$CSC258\ Lab\ 2$

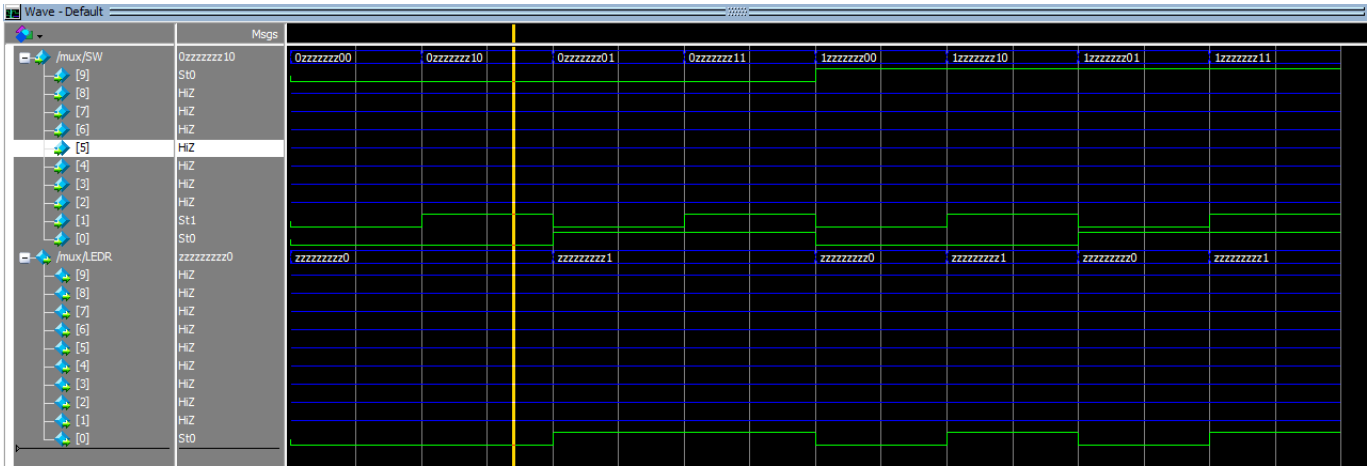
$Pre-Lab$

$Shantanu\ Singh$ 1005218514

$Part\ I$

1. $We\ can\ find\ the\ generated\ waveform\ below\ simulation\ below\ and\ comapring\ the\ output\ with$

$2-to-1\ multiplexer's\ Truth\ Table, we\ can\ verify\ that\ the\ test\ cases\ work\ as\ we\ expect.$



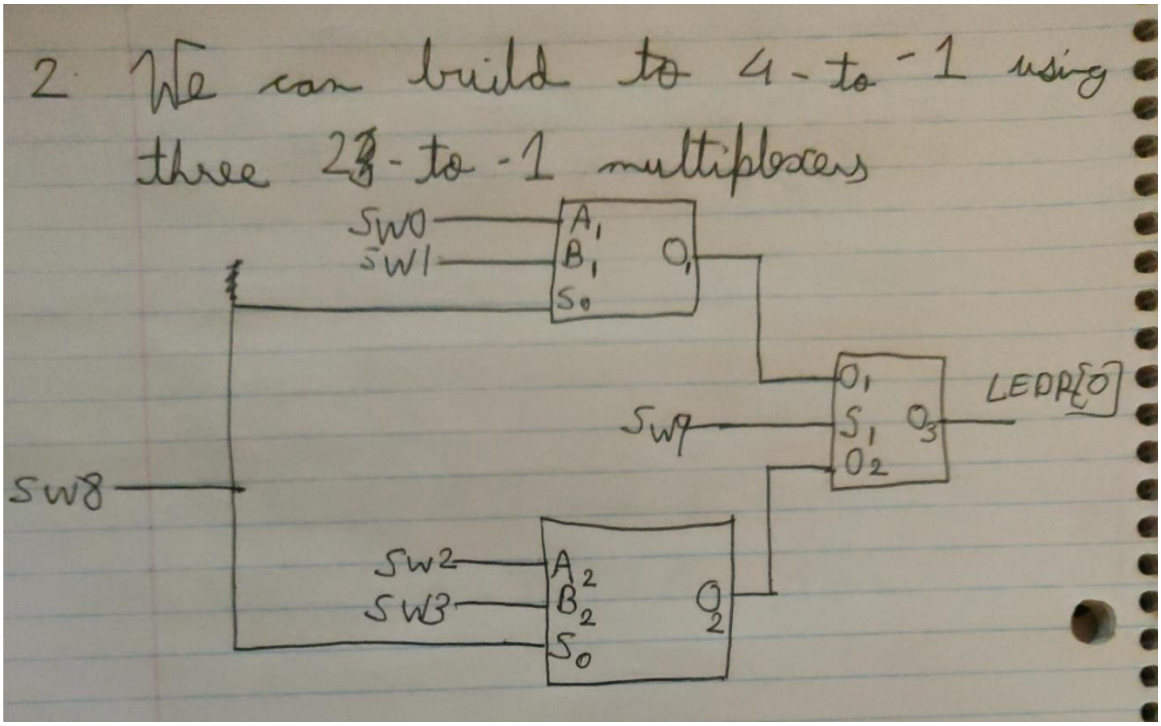
$The\ output\ is\ as\ expected, The\ LEDR\ [0]\ lights\ up\ when\ s = 0\ implying\ y = 1\ which\ is\ the\ case.$

$Similarly\ when\ s = 1, which\ means\ LEDR[0]\ lights\ up\ when\ x = 1\ which\ is\ the\ case.$

$Part\ II$

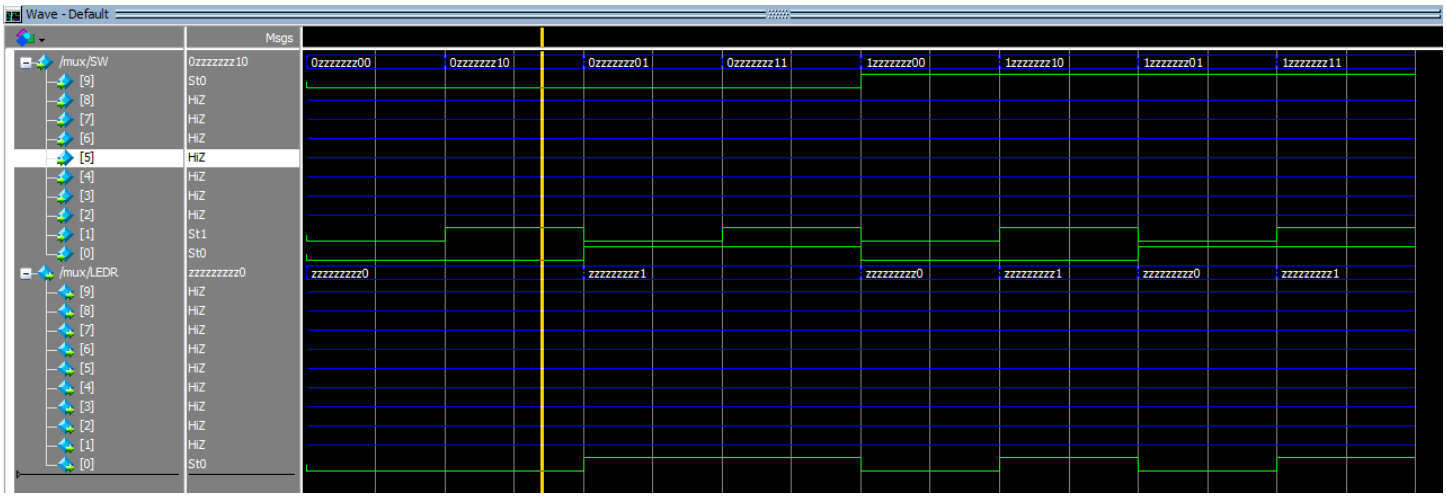
1. $A\ 4-to-1\ multiplexer\ has\ 6\ total\ inputs\ therefore\ with\ 2\ possible\ values\ (0\ or\ 1),$

$therefore\ it\ will\ have\ 2^6 = 64\ inputs.$

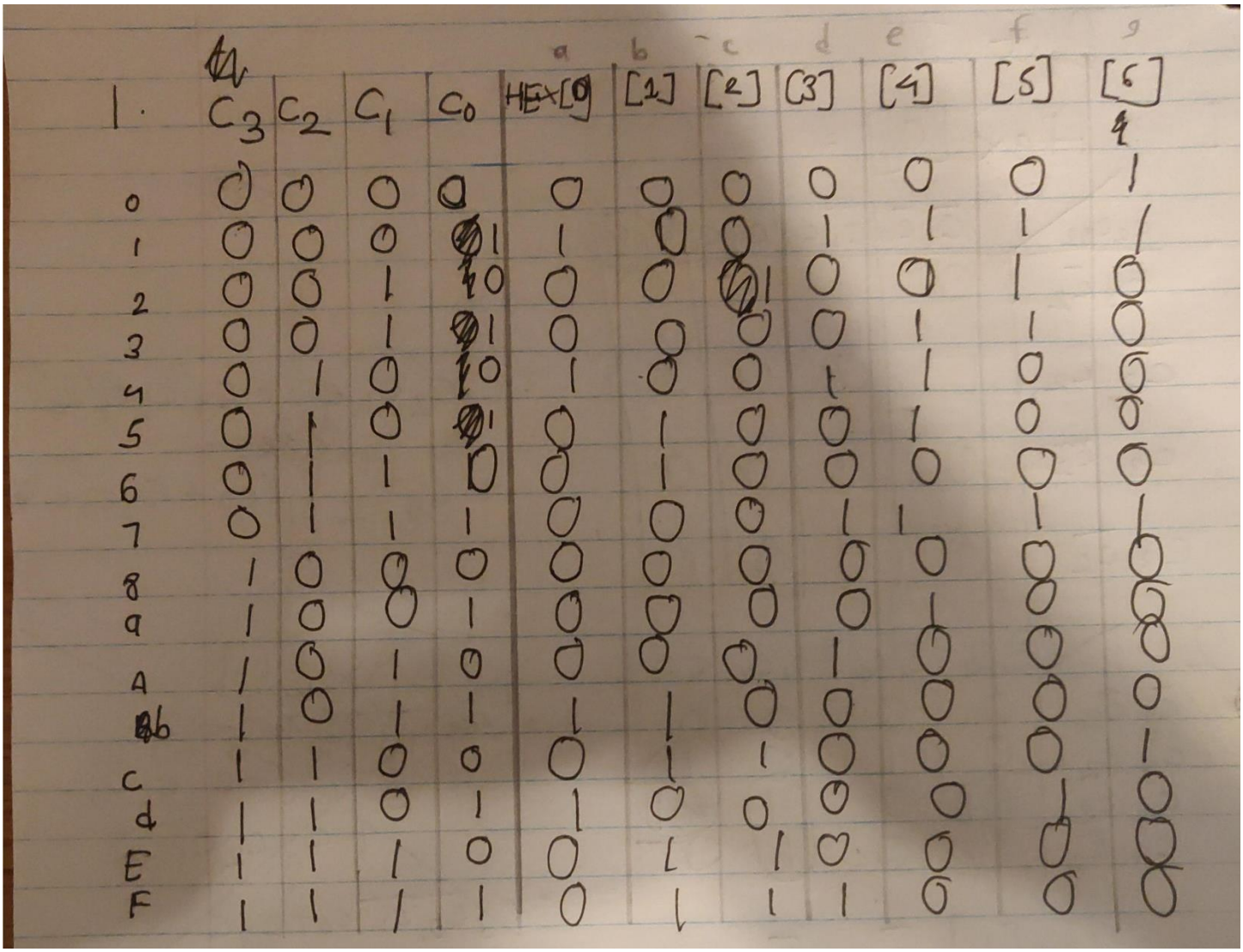


Q3. Write the Verilog Code – Please refer to Four_To_One.v

Q5. Please find attached the Four_To_One.do *file that was simulated in ModelSim. Here is an attached screenshot of the same.*



PART III



	C_3	C_2	C_1	C_0	HEX	a [0]	b [1]	c [2]	d [3]	e [4]	f [5]	g [6]
0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	0	1	1	1	1
2	0	0	1	0	2	0	0	1	0	0	1	0
3	0	0	1	1	3	0	0	0	0	1	1	0
4	0	1	0	0	4	1	0	0	1	1	0	0
5	0	1	0	1	5	0	1	0	0	1	0	0
6	0	1	1	0	6	0	1	0	0	0	0	0
7	0	1	1	1	7	0	0	0	1	1	1	1
8	1	0	0	0	8	0	0	0	0	0	0	0
9	1	0	0	1	9	0	0	0	0	1	0	0
A	1	0	1	0	A	0	0	0	1	0	0	0
b	1	0	1	1	b	1	1	0	0	0	0	1
C	1	1	0	0	C	0	1	1	0	0	0	1
d	1	1	0	1	d	1	0	0	0	0	1	0
E	1	1	1	0	E	0	1	1	0	0	0	0
F	1	1	1	1	F	0	1	1	1	0	0	0

Part III

1. Hex [0] =

C_3C_2 \ C_1C_0	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	C_1C_0	$C_1\bar{C}_0$
$\bar{C}_3\bar{C}_2$	0	1	0	0
$\bar{C}_3C_2$	1	0	0	0
C_3C_2	0	1	0	0
$C_3\bar{C}_2$	0	0	1	0

$= C_3'C_2'C_1'C_0 + C_3'C_2C_1'C_0$
$+ C_1'C_0C_3$
$+ C_3C_2C_1'C_0 + C_3C_2'C_1$

2.

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	C_1C_0	$C_1\bar{C}_0$
$\bar{C}_3\bar{C}_2$	0	0	0	0
$\bar{C}_3C_2$	0	1	0	1
C_3C_2	1	0	1	1
$C_3\bar{C}_2$	0	0	1	0

Hex [1]
$= C_3C_2C_1C_0 + C_3C_2C_1C_0$
$+ C_3C_1C_0 + C_2C_1\bar{C}_0$
$+ C_3C_2\bar{C}_1C_0$
$+ C_3C_2C_1C_0 + C_3C$

Hex[1] $= \bar{C}_3C_2\bar{C}_1C_0 + C_3C_1C_0 + C_2C_1\bar{C}_0 + C_3C_2\bar{C}$

3.

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	C_1C_0	$C_1\bar{C}_0$
$\bar{C}_3\bar{C}_2$	0	0	0	1
$\bar{C}_3C_2$	0	0	0	0
C_3C_2	1	0	1	1
$C_3\bar{C}_2$	0	0	0	0

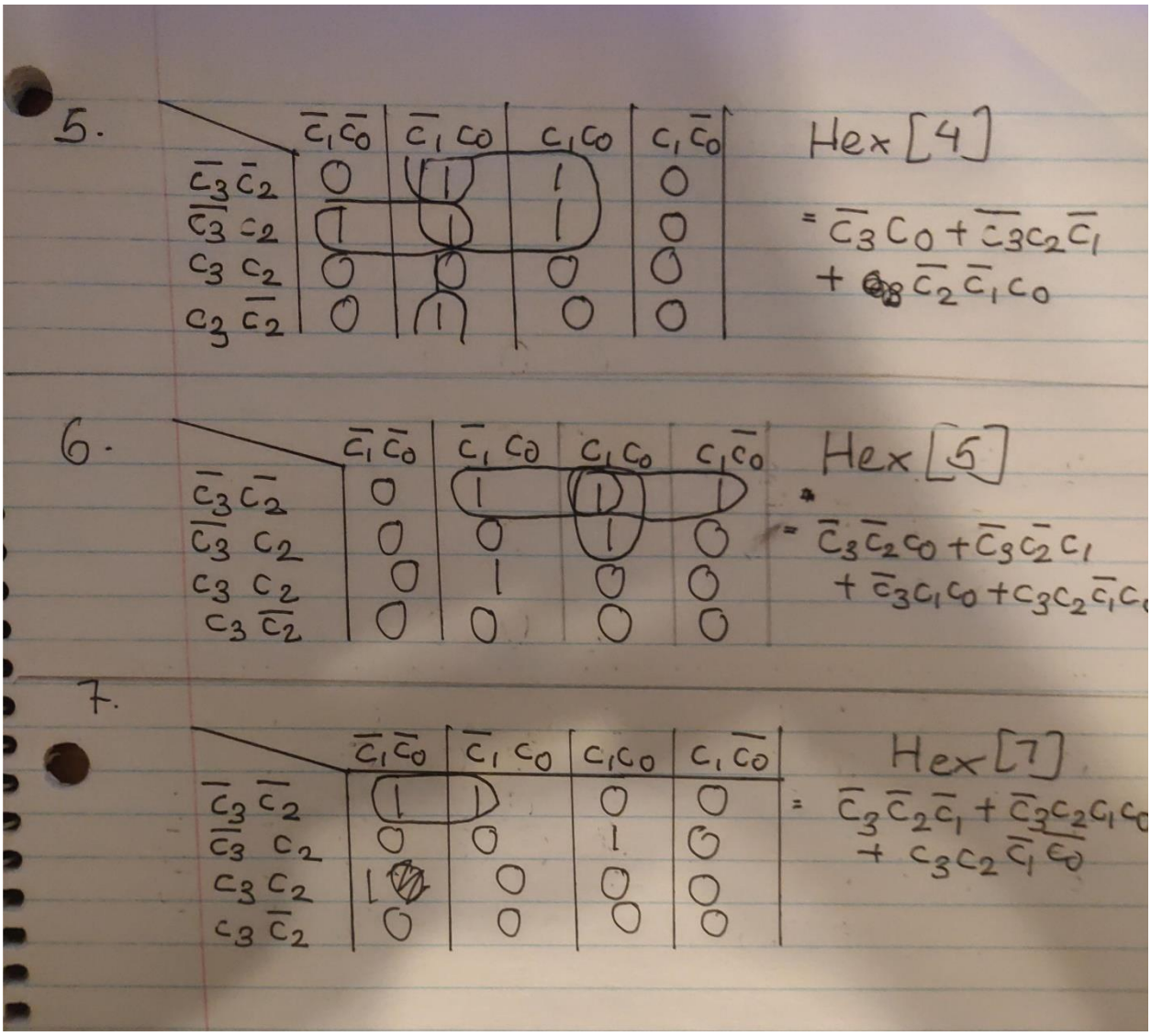
Hex [2]
$= C_3C_2\bar{C}_1\bar{C}_0 + \overline{C_3C_2}C_1\bar{C}_0$
$+ C_3C_2C_1$

4.

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	C_1C_0	$C_1\bar{C}_0$
$\bar{C}_3\bar{C}_2$	0	1	0	0
$\bar{C}_3C_2$	1	0	1	0
C_3C_2	0	0	1	0
$C_3\bar{C}_2$	0	0	0	1

Hex [3]
$= \bar{C}_3C_2\bar{C}_1C_0 + \overline{C_3C_2C_1}$
$+ C_2C_1C_0 + C_3\bar{C}_2C_1\bar{C}$

Hilroy



Q2. Write the Verilog Module – Please refer to SevenHex.v

Q3. My Room is BA3155. Please check SevenHex.do. Screenshot of the same attached below.