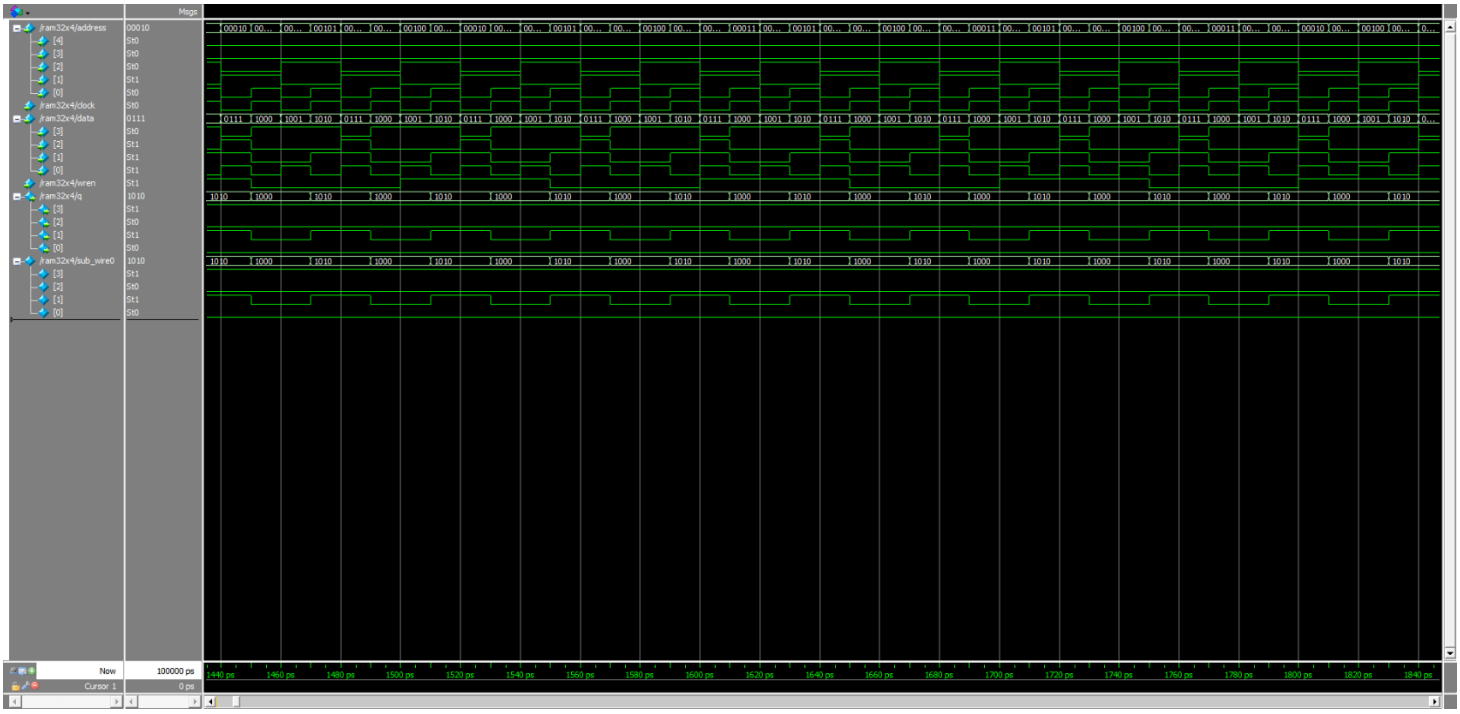
CSC258 Pre – Lab 7

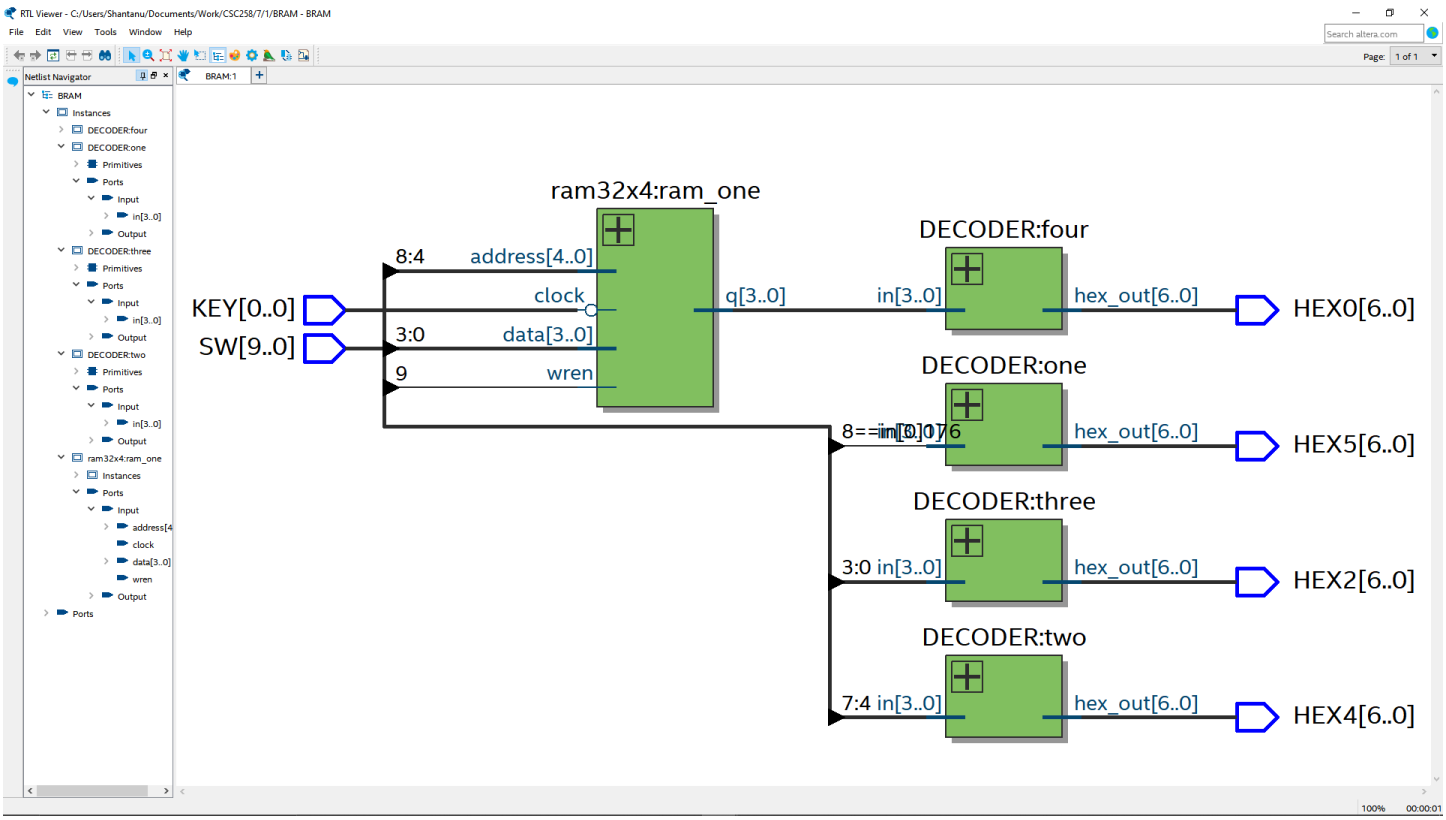
Part 1

9. *Attach screenshot of ram32x4.v simulations*



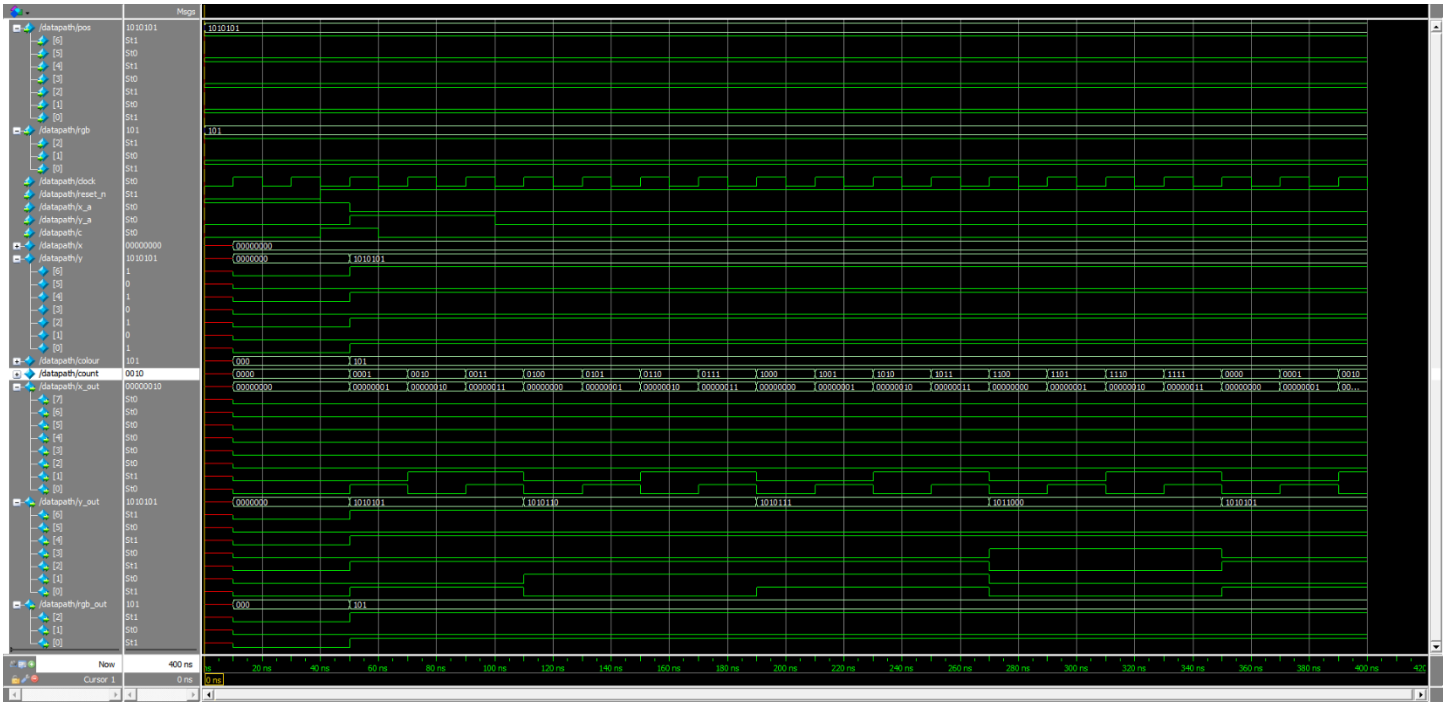
10. *Instantiate ram32x4.v to a top – level verilog module – Please check BRAM.v*

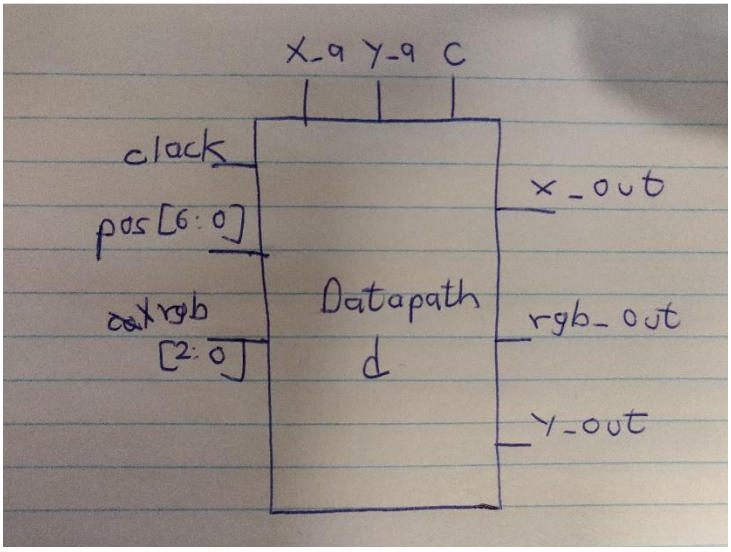
11. *Draw a schematic –*



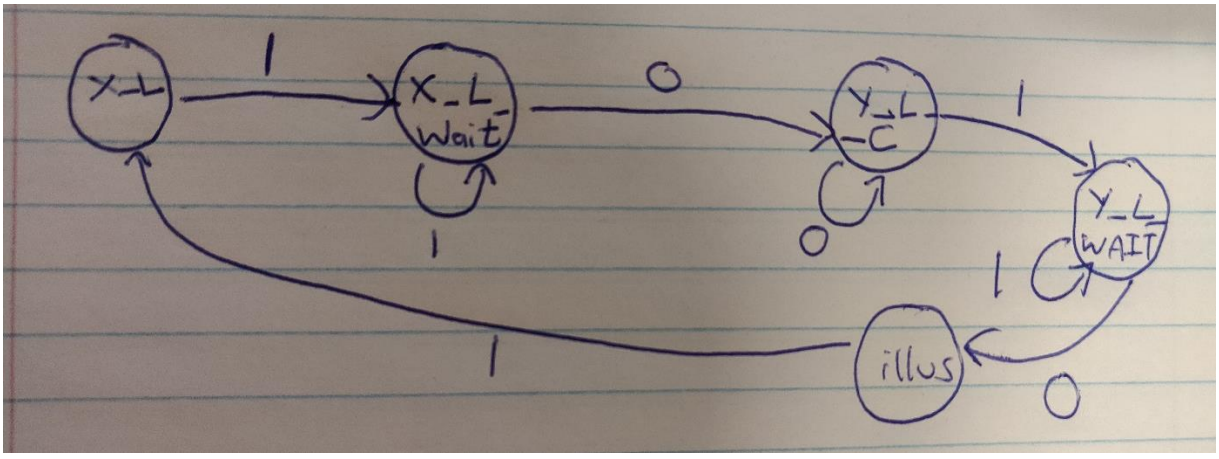
Part 2

1. *Draw the Schematics and Post Screenshots – Please see module datapath of part2.v*

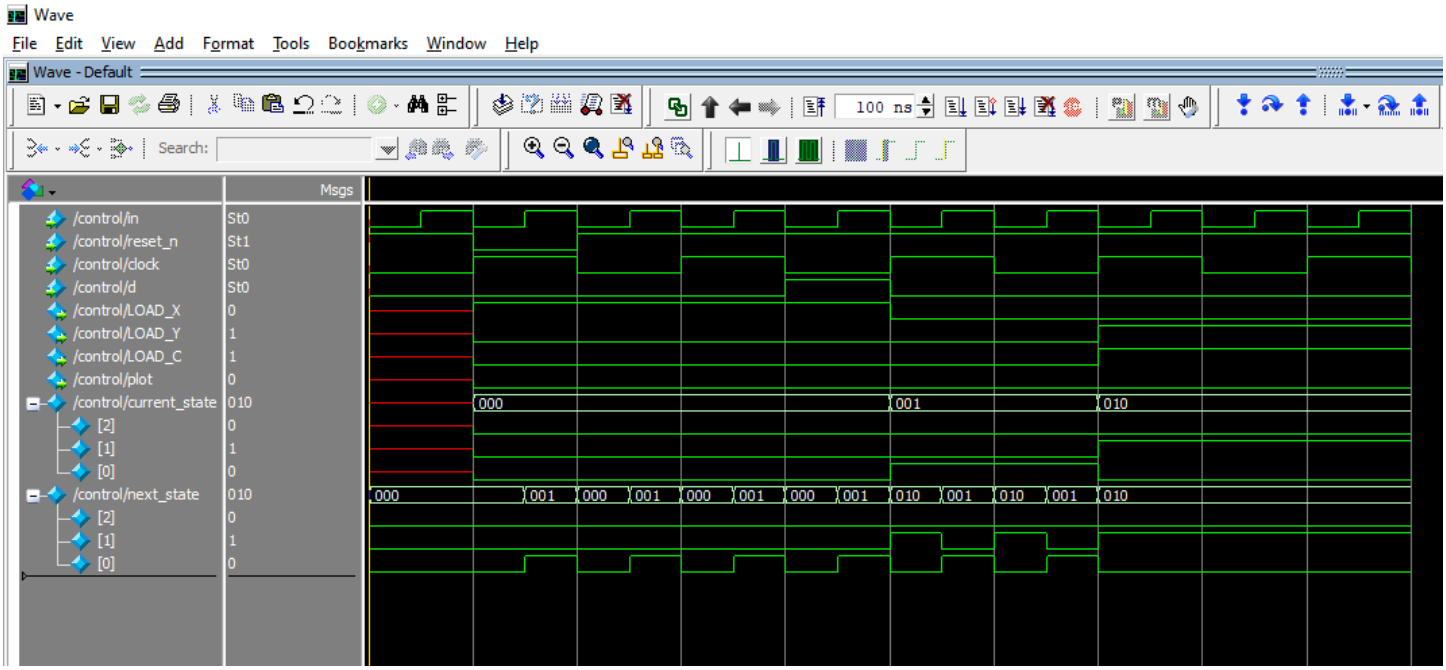




2. *Design the FSM and simulate it and Post Screenshots – Please see module control of part2.v*



State	LOAD_X	LOAD_Y	LOAD_C	plot
X_L	1	0	0	0
Y_L_C	1	1	1	0
d	1	1	1	1



3. *Simulate and Post Screenshots – Please see module joined of part2.v*