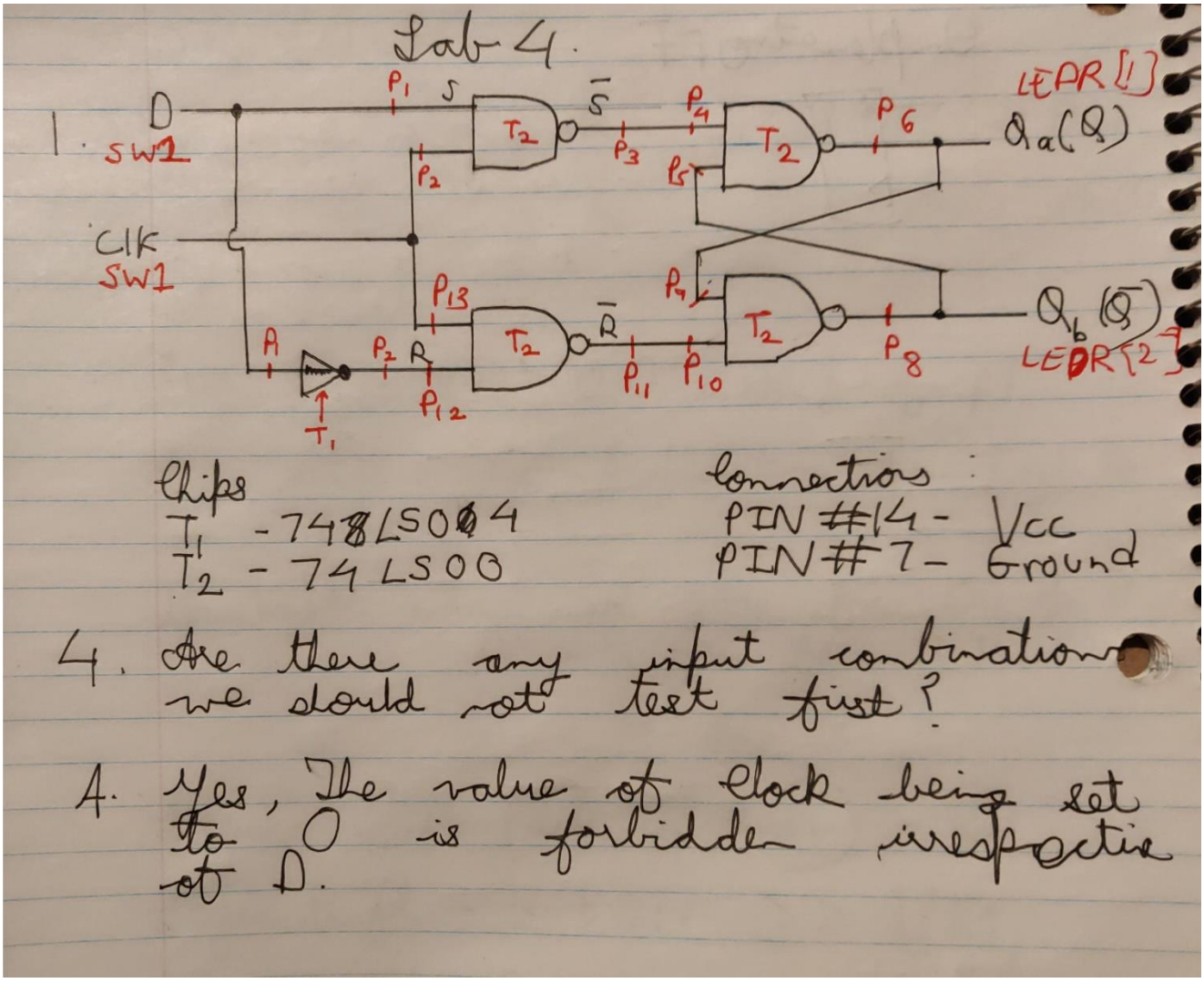
Lab 4

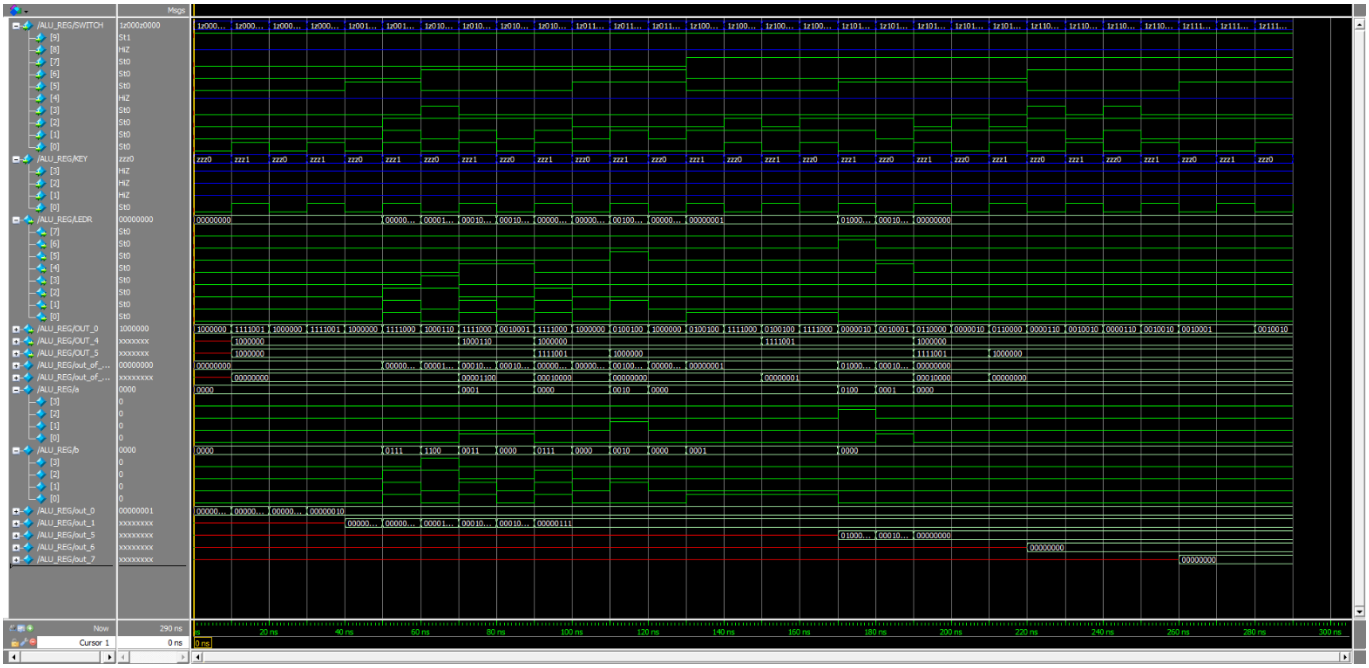
Part I


Lab 4.
D
SW2
CLK
SW1
S
$\bar{S}$
R
$\bar{R}$
T_1
T_2
P_1
P_2
P_3
P_4
P_5
P_6
P_7
P_8
P_{10}
P_{11}
P_{12}
P_{13}
A
LEDR[1]
LEDR[2]
$Q_a(Q)$
$Q_b(\bar{Q})$
Chips
T_1 - 74LS04
T_2 - 74LS00
Connections:
PIN #14 - Vcc
PIN #7 - Ground
4. Are there any input combinations we should not test first?
A. Yes, The value of clock being set to 0 is forbidden irrespective of D.

Part II

1. *Create a Verilog Module – Please refer to ALU_REG.v*

2. *Run the simulation and Show Screenshots – Please refer to the screenshots below and ALU_REG.do if required.*



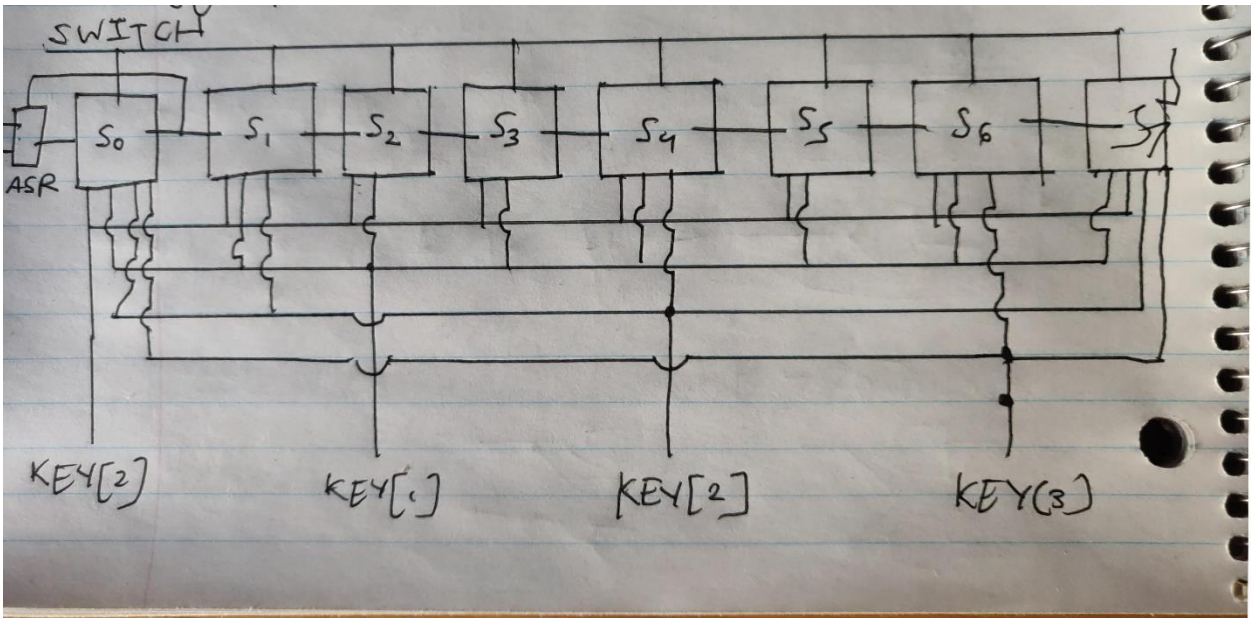
Part III

1. *What is the behaviour of the* 8 − *bit shift register shown in Figure* 6?

Ans − *The Multiplexer only decides the input of D and the value of the register is unchanged.*

Load and ShiftRight are connect to the MUX which is connected to D so Register is constant.

2. *Draw a Schematic*



3 & 4. *Please refer to SHIFT_REG.v*

5. *Compile and Sim and attach Screenshots of the output.*