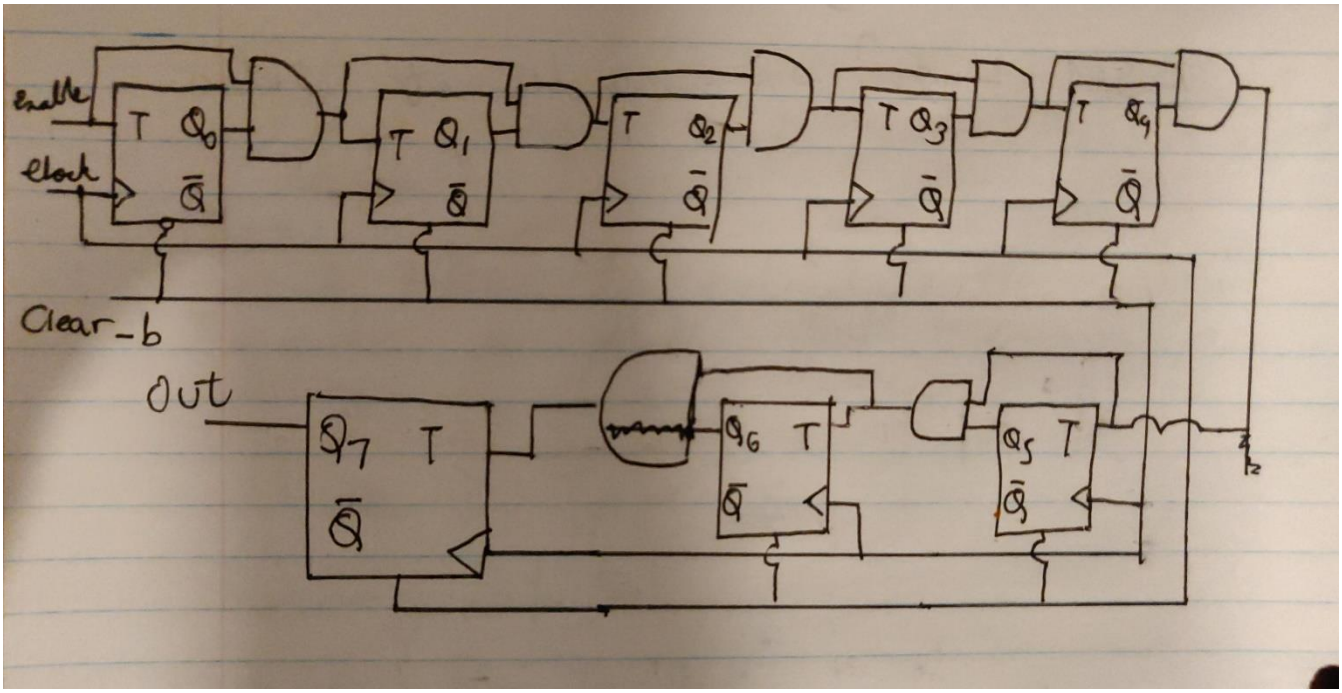
LAB 5

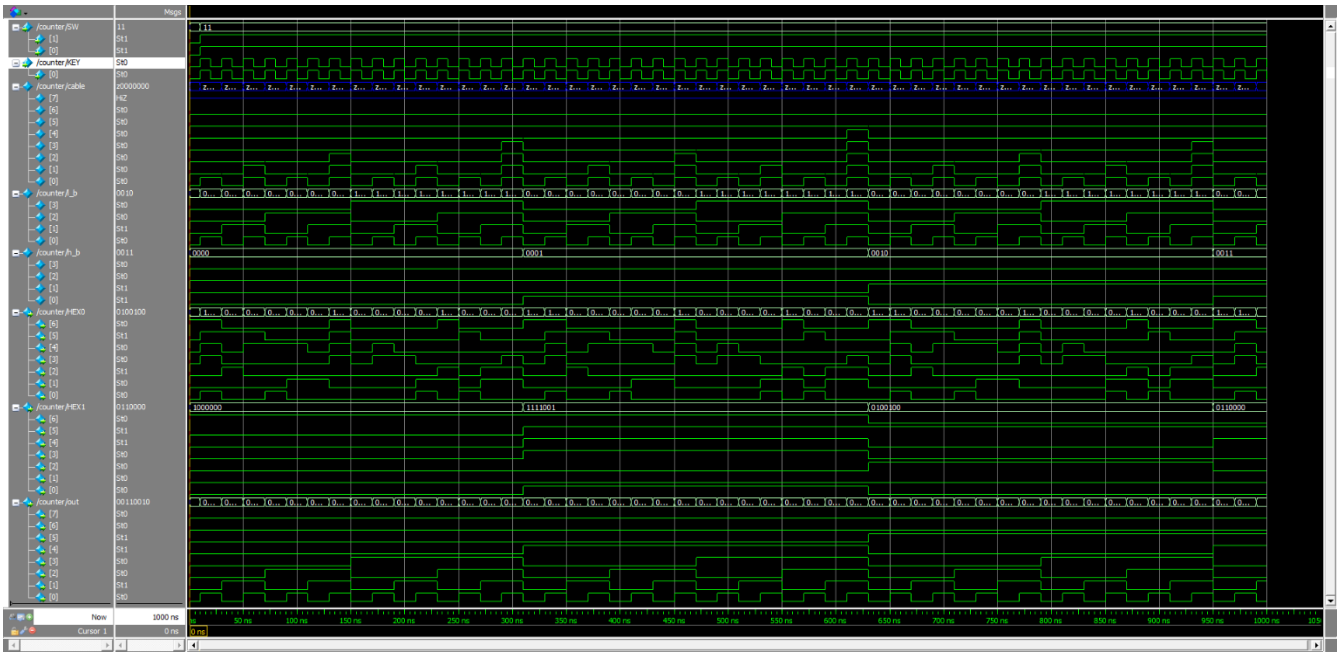
Part I

1 & 2

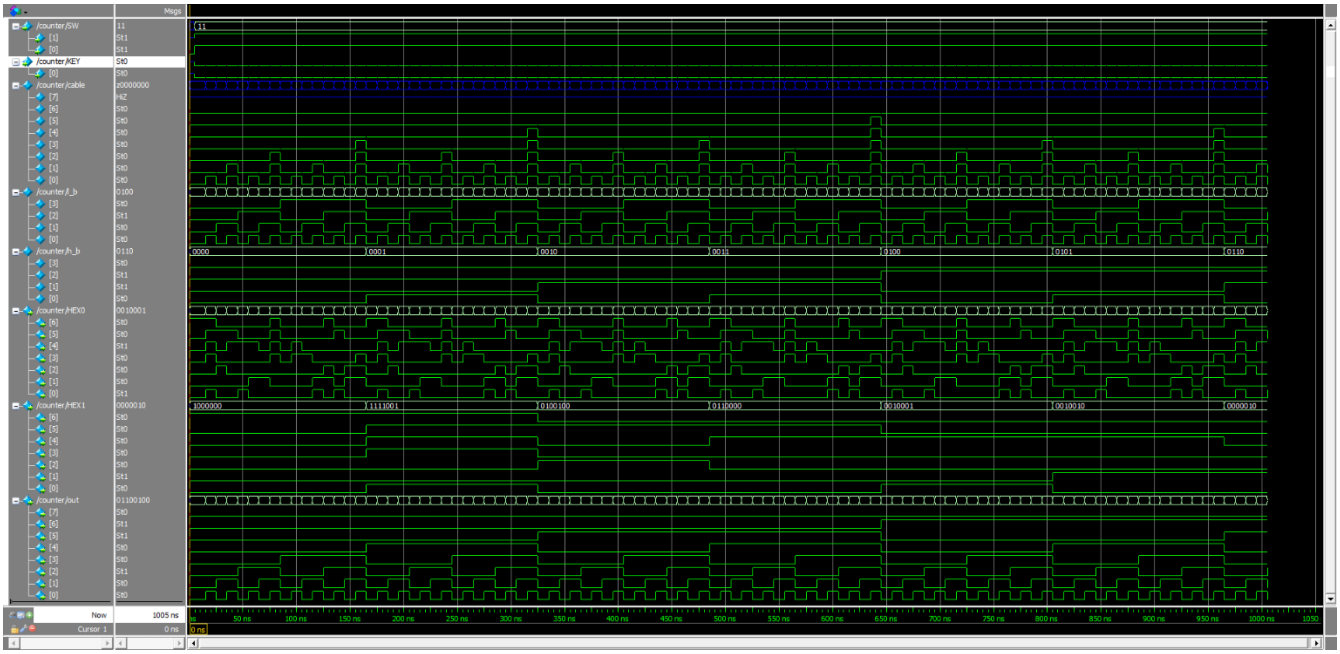


3. *Verilog Code – Please check counter.v*

4. *Simulate the circuit –*



5. *Simulate the circuit again –*



6. *Create a new Quartus Project –*

A.

Logic utilization (in ALMs)	13 / 32,070 (< 1 %)
Total registers	8

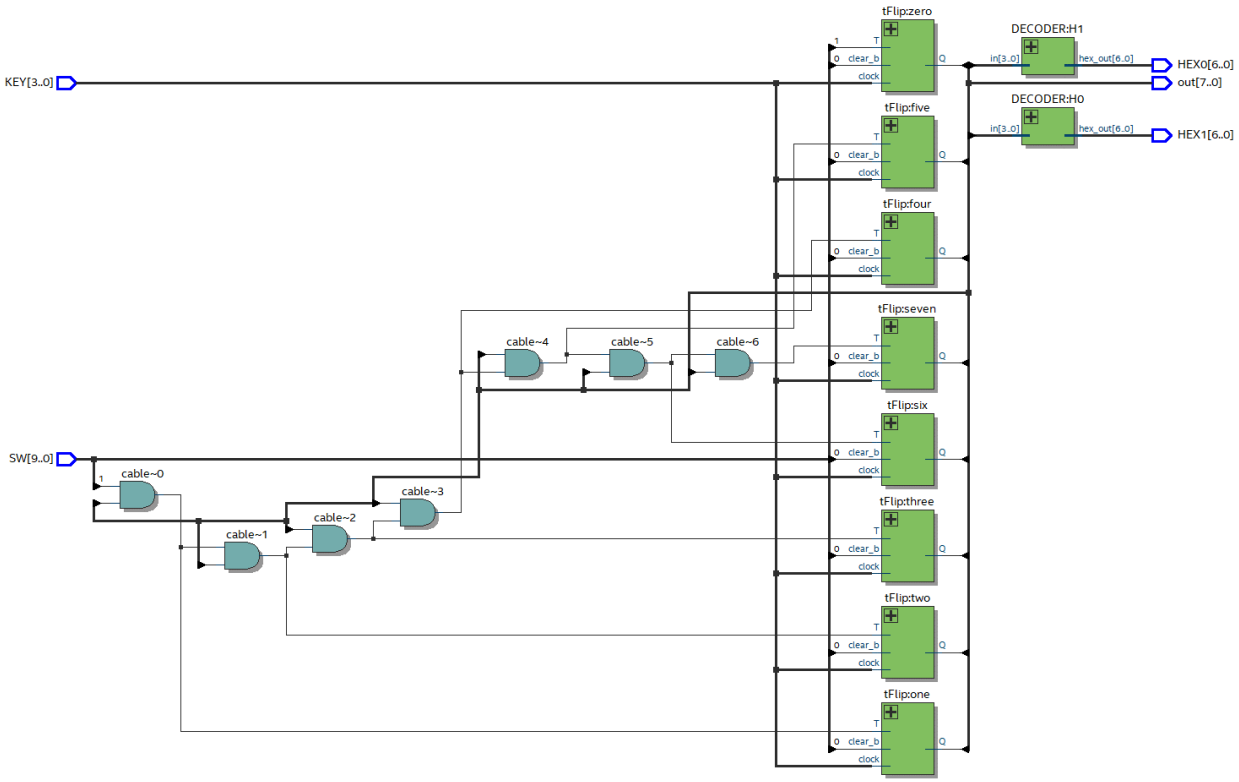
B.

Slow 1100mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	666.67 MHz	621.89 MHz	KEY[0]	limit due to low minimum pulse width violation (tcl)

7. *View the Synthesized Circuit.*



Part II

A1. Since it is 4 bits only, adding 1 to 1111 will make it 0000 and we are back to the default postion.

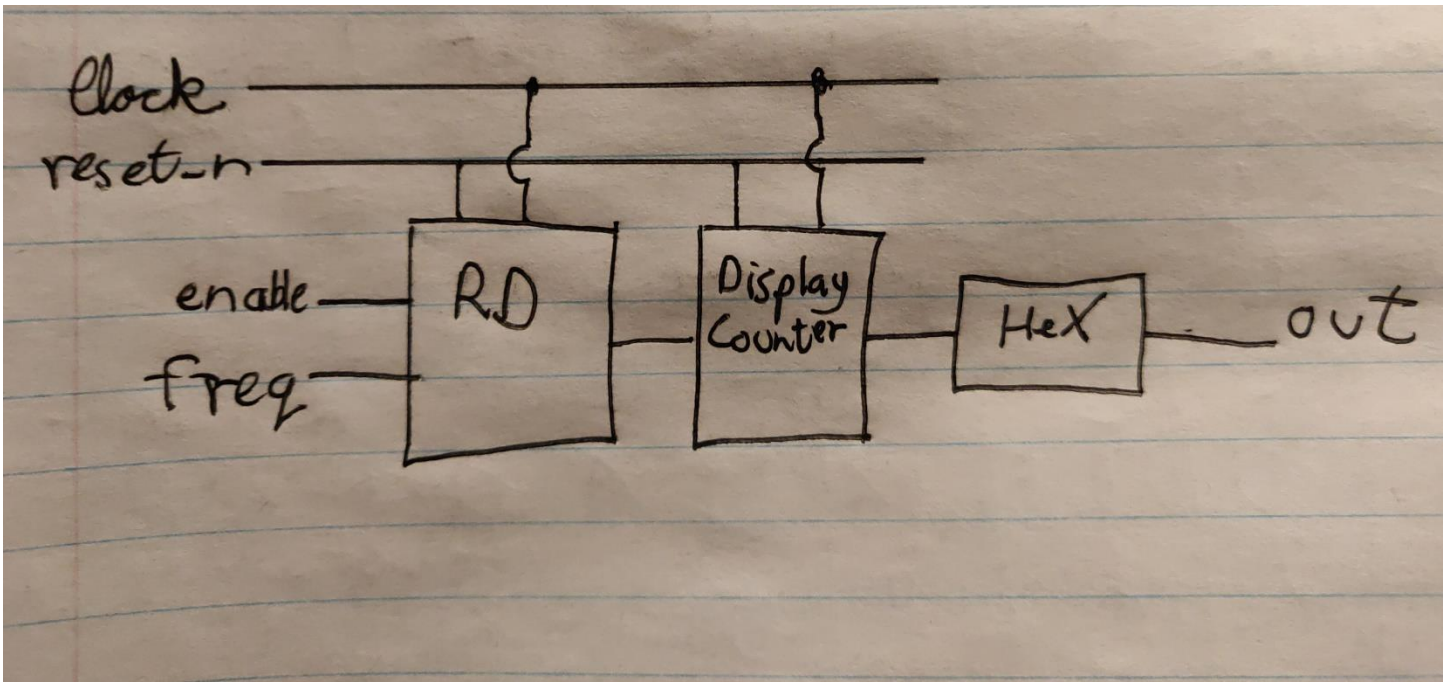
A2. Since 9 is 1001 in binary, we change `if ( q == 4'b1111 )` *to* `if ( q == 4'b1001 )`

A3. At this speed we will see all the numbers flashing 50 Million times a second. Due to our persistence of vision, being 10 Hz we will see 8

A4. We should require not more than 2 counters

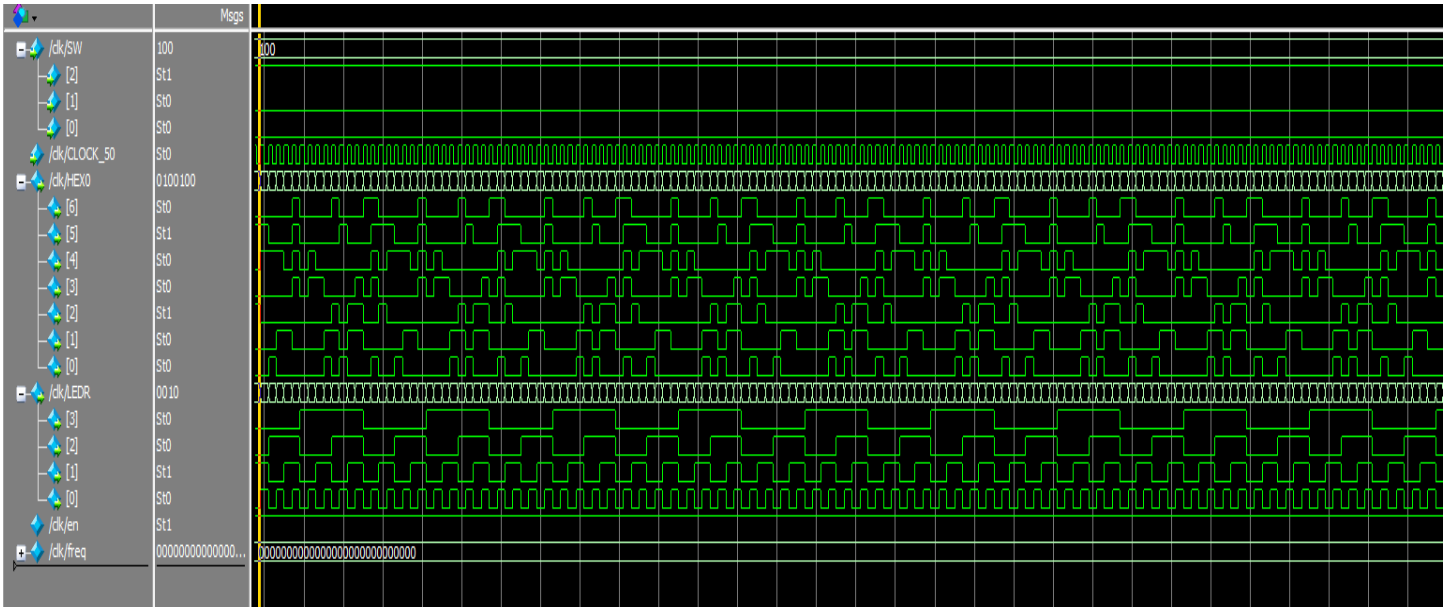
A5. Since $2^{26} = 67108864$*, it will require* $26 - bits\ minimum$

1.



2. *Verilog Code – Please check clk.v*

3. *Simulate the circuit –*

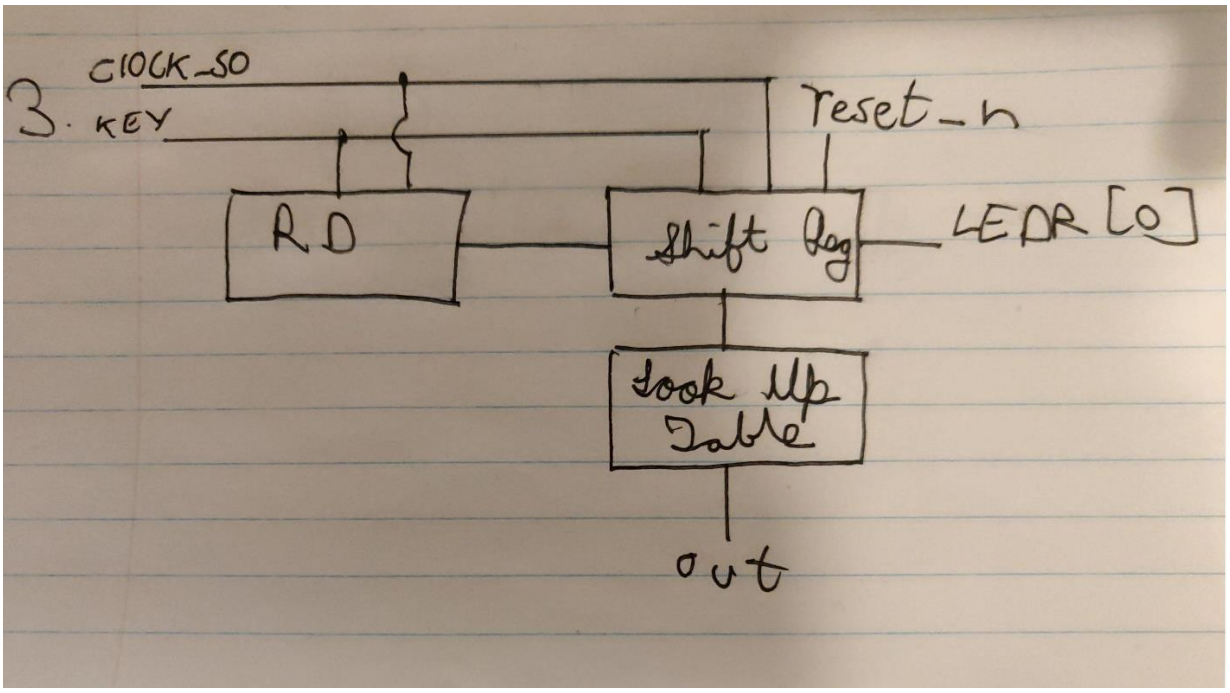


Part III

1.

Letter	Morse Code	Pattern Representation (pattern length is 14 bits)
S	• • •	10101 000 000 000
T	—	11100000000000
U	• • —	10101110000000
V	• • • —	10101011100000
W	• — —	10111011100000
X	— • • —	111010101110
Y	— • — —	11101011101110
Z	— — • •	11101110101000

2.



3. *Verilog Code – Please check morse.v*

4. *Screenshot of the Simulations –*