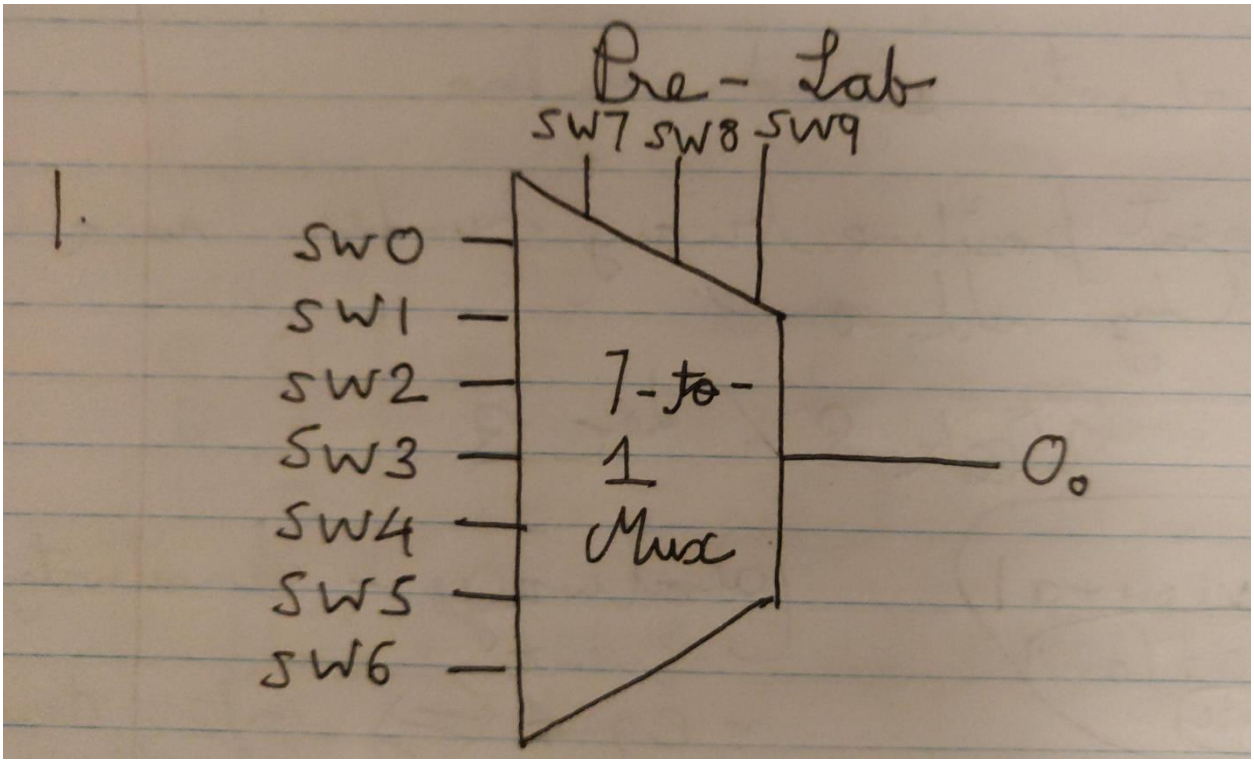
LAB 3

Shantanu Singh – 1005218514

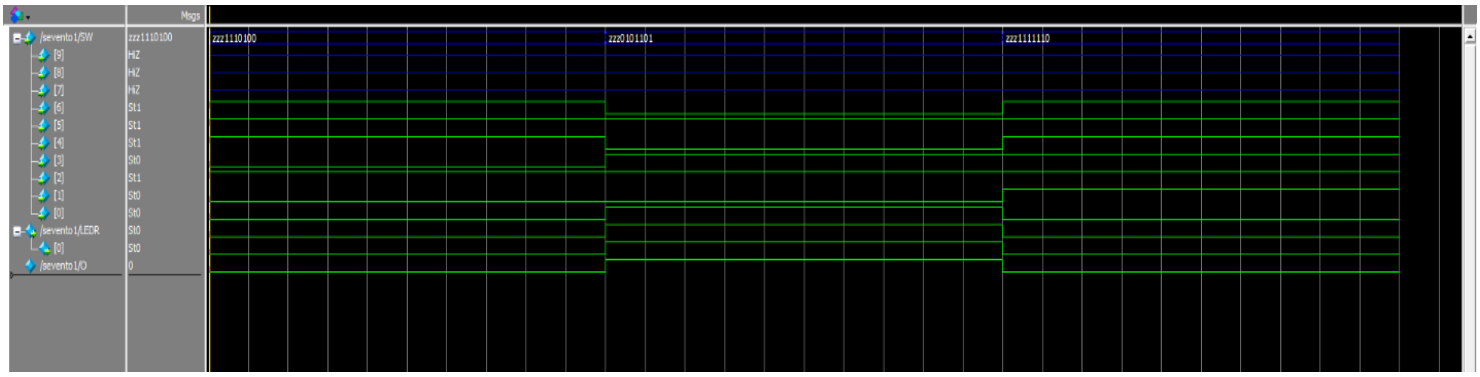
Part I



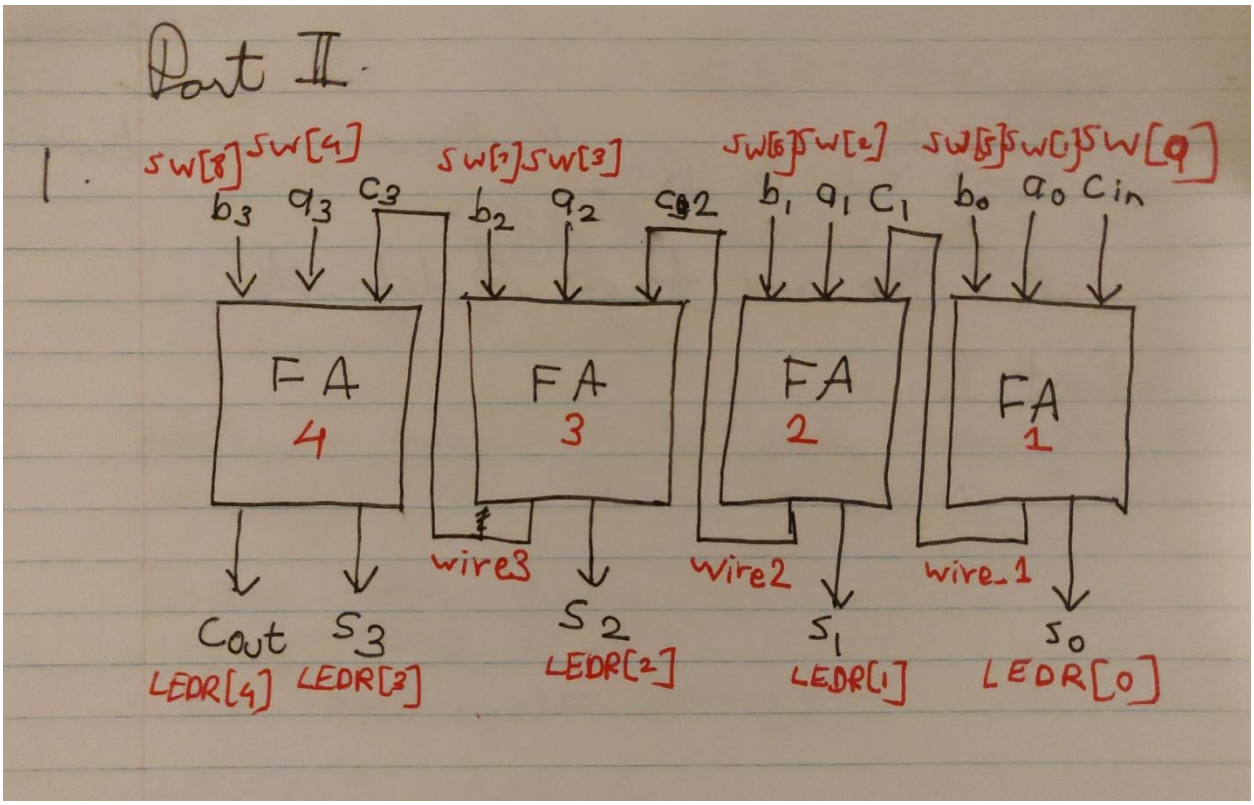
2. *Write the Verilog Code for the* 7 – *to* – 1 *MUX*.

*Ans – Please check the sevento*1.*v file attached with this file*

3. *Attach a screenshot of the simulation*



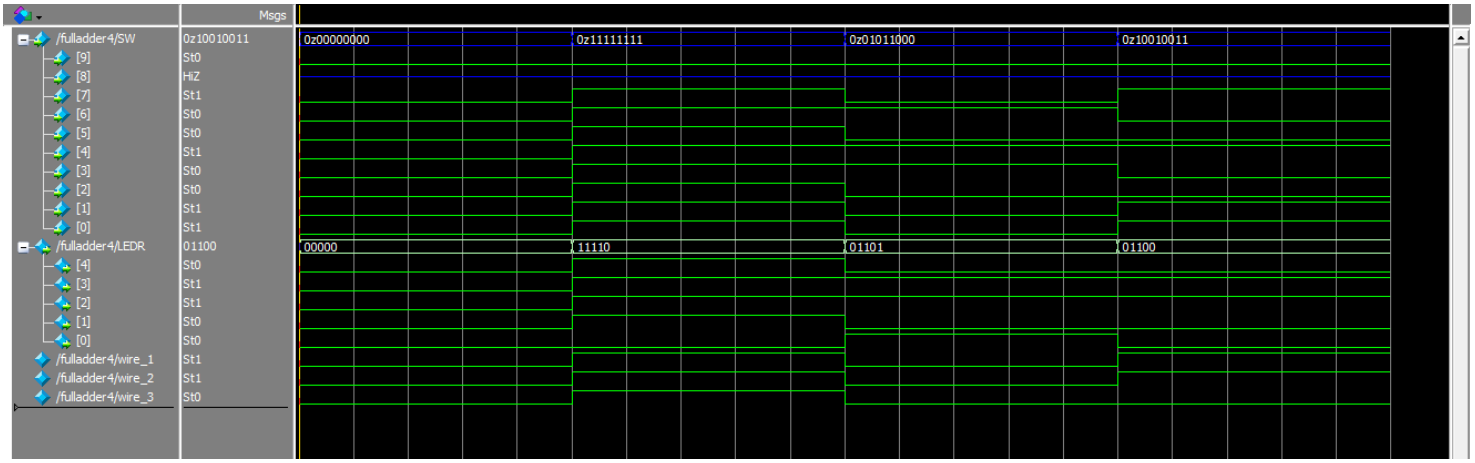
Part II



2. *Write the Verilog Code for Full − Adder.*

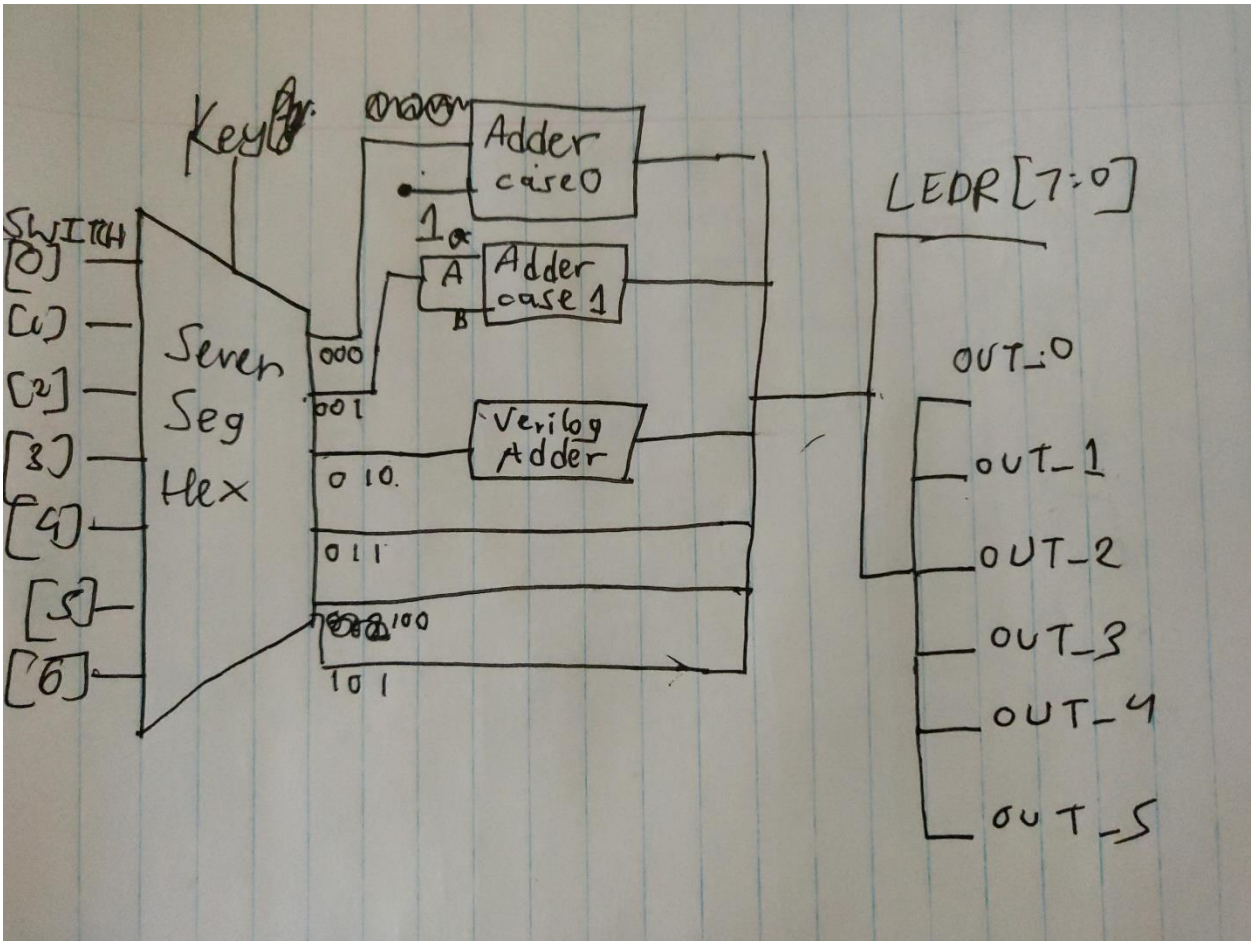
Ans − Please check the fulladder4.v file uploaded with this.

3. *Attach a screenshot of the simulation*



Part III

1.



2. *Write the Verilog Code for the ALU*

Ans – Please check ALU.v attached with this file

3. *Attach a screenshot of the simulation*