

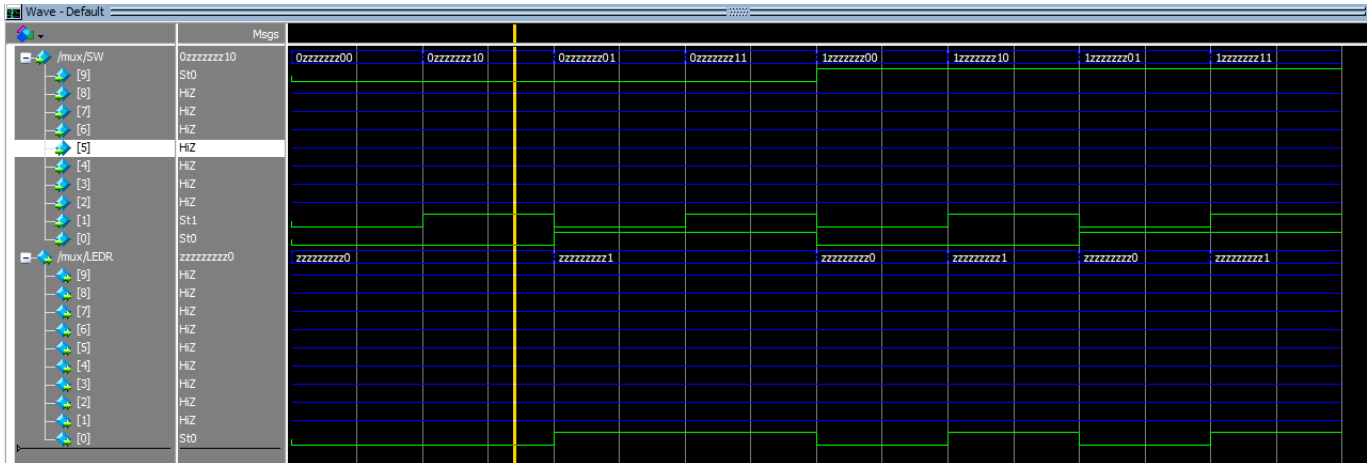
CSC258 Lab 2

Pre – Lab

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Part I

1. We can find the generated waveform below simulation below and comparing the output with 2 – to – 1 multiplexer's Truth Table, we can verify that the test cases work as we expect.

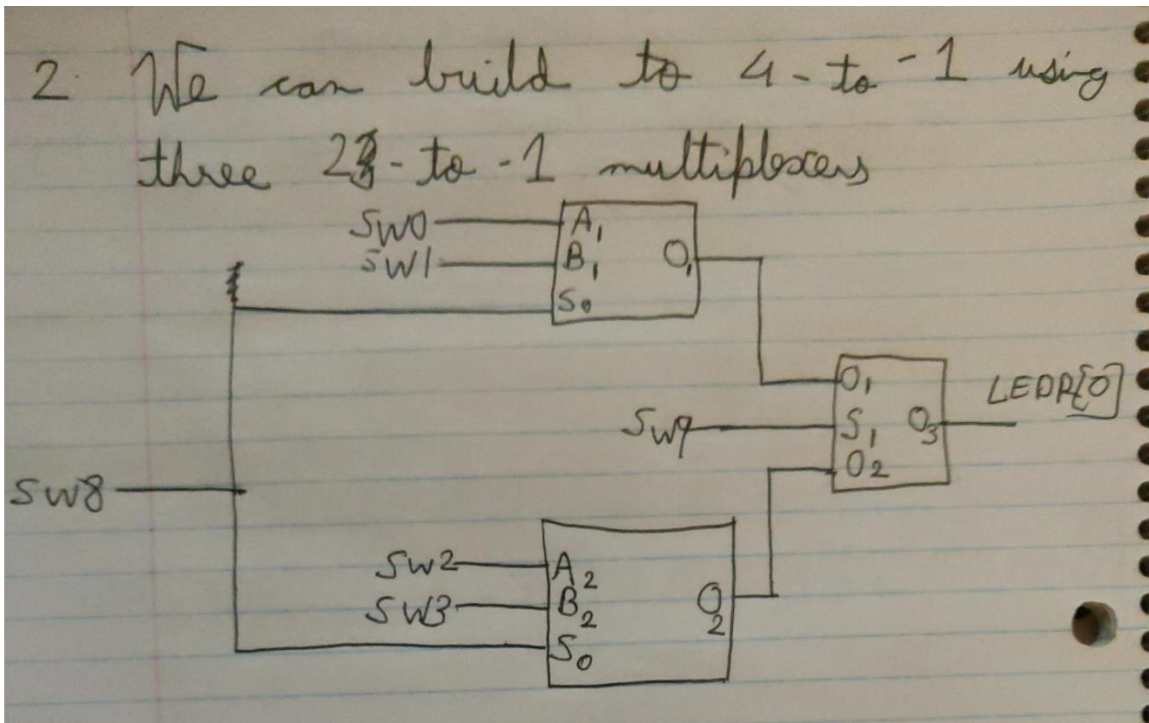


The output is as expected, The LEDR [0] lights up when $s = 0$ implying $y = 1$ which is the case.

Similarly when $s = 1$, which means LEDR[0] lights up when $x = 1$ which is the case.

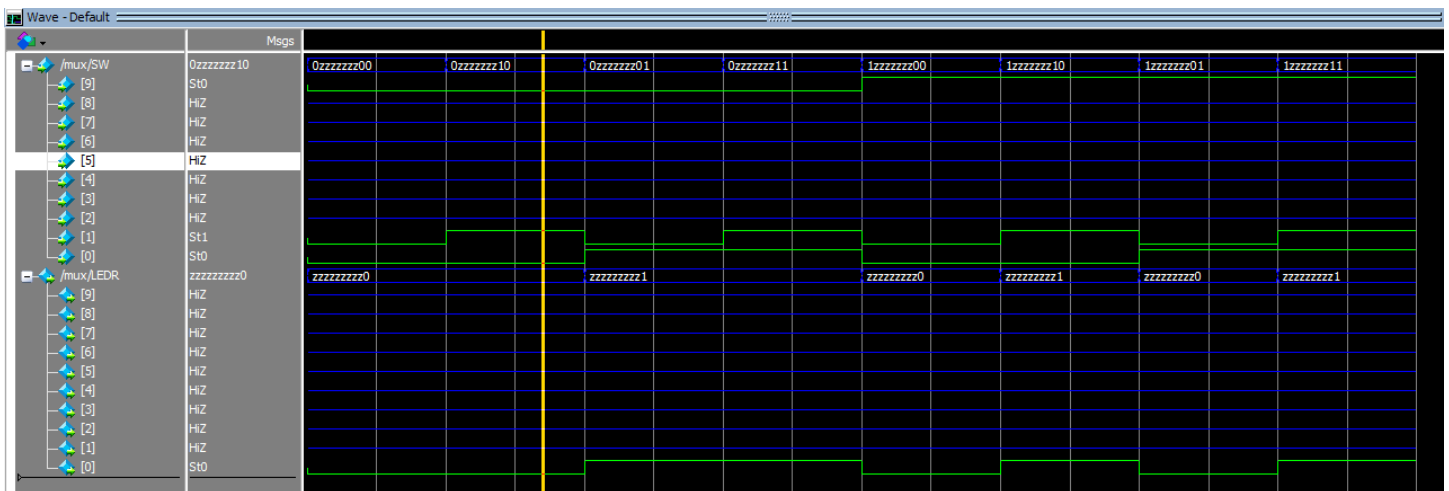
Part II

1. A 4 – to – 1 multiplexer has 6 total inputs therefore with 2 possible values (0 or 1), therefore it will have $2^6 = 64$ inputs.



Q3. Write the Verilog Code – Please refer to Four_To_One.v

Q5. Please find attached the Four_To_One.do file that was simulated in ModelSim. Here is an attached screenshot of the same.



PART III

	A C ₃	C ₂	C ₁	C ₀	HEX [0]	a [1]	b [2]	c [3]	d [4]	e [5]	f [6]	g
0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	1	0
3	0	0	1	1	0	0	0	0	1	1	1	0
4	0	1	0	0	1	0	0	0	1	0	0	0
5	0	1	0	1	0	1	0	0	1	0	0	0
6	0	1	1	0	0	1	0	0	0	0	0	0
7	0	1	1	1	0	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	0	0	0	0
A	1	0	1	0	0	0	0	1	0	0	0	0
B	1	0	1	1	1	1	0	0	0	0	0	0
C	1	1	0	0	0	1	1	0	0	0	0	1
D	1	1	0	1	1	0	0	0	0	0	0	0
E	1	1	1	0	0	1	1	0	0	0	0	0
F	1	1	1	1	0	1	1	1	0	0	0	0

Part III.

1. Hex [0] =

$c_3 c_2$ \ $c_1 c_0$	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 \bar{c}_0$	$c_1 c_0$
$\bar{c}_3 \bar{c}_2$	0	1	0	0
$\bar{c}_3 c_2$	1	0	0	0
$c_3 \bar{c}_2$	0	1	0	0
$c_3 c_2$	0	0	1	0

$$= \bar{c}_3 \bar{c}_2 c_1 c_0 + \bar{c}_3 c_2 c_1 c_0 + c_3 \bar{c}_2 c_1 c_0 + c_3 c_2 c_1 c_0$$

2.

$c_3 c_2$ \ $c_1 c_0$	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 \bar{c}_0$	$c_1 c_0$
$\bar{c}_3 \bar{c}_2$	0	0	0	0
$\bar{c}_3 c_2$	0	1	0	1
$c_3 \bar{c}_2$	1	0	1	1
$c_3 c_2$	0	0	1	0

~~Hex [1]~~

$$= \bar{c}_3 \bar{c}_2 c_1 c_0 + \bar{c}_3 c_2 c_1 c_0 + c_3 \bar{c}_2 c_1 c_0 + c_3 c_2 c_1 c_0$$

$$\text{Hex}[1] = \bar{c}_3 c_2 \bar{c}_1 c_0 + c_3 c_1 c_0 + c_2 c_1 c_0 + c_3 c_2 c_1$$

3.

$c_3 c_2$ \ $c_1 c_0$	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 \bar{c}_0$	$c_1 c_0$
$\bar{c}_3 \bar{c}_2$	0	0	0	1
$\bar{c}_3 c_2$	0	0	0	0
$c_3 \bar{c}_2$	1	0	1	1
$c_3 c_2$	0	0	0	0

Hex [2]

$$= c_3 c_2 \bar{c}_1 c_0 + c_3 c_2 c_1 c_0 + c_3 c_2 c_1$$

4.

$c_3 c_2$ \ $c_1 c_0$	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 \bar{c}_0$	$c_1 c_0$
$\bar{c}_3 \bar{c}_2$	0	1	0	0
$\bar{c}_3 c_2$	1	0	1	0
$c_3 \bar{c}_2$	0	0	1	0
$c_3 c_2$	0	0	0	1

Hex [3]

$$= \bar{c}_3 c_2 \bar{c}_1 c_0 + \bar{c}_3 c_2 c_1 c_0 + c_2 c_1 c_0 + c_3 \bar{c}_2 c_1 c_0$$

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5.

	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 c_0$	$c_1 \bar{c}_0$
$\bar{c}_3 \bar{c}_2$	0	1	1	0
$\bar{c}_3 c_2$	1	1	1	0
$c_3 c_2$	0	0	0	0
$c_3 \bar{c}_2$	0	1	0	0

Hex [4]

$$= \bar{c}_3 c_0 + \bar{c}_3 c_2 \bar{c}_1 + c_3 \bar{c}_2 \bar{c}_1 c_0$$

6.

	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 c_0$	$c_1 \bar{c}_0$
$\bar{c}_3 \bar{c}_2$	0	1	1	1
$\bar{c}_3 c_2$	0	0	1	0
$c_3 c_2$	0	1	0	0
$c_3 \bar{c}_2$	0	0	0	0

Hex [5]

$$= \bar{c}_3 \bar{c}_2 c_0 + \bar{c}_3 c_2 c_1 + \bar{c}_3 c_1 c_0 + c_3 c_2 \bar{c}_1 c_0$$

7.

	$\bar{c}_1 \bar{c}_0$	$\bar{c}_1 c_0$	$c_1 c_0$	$c_1 \bar{c}_0$
$\bar{c}_3 \bar{c}_2$	1	1	0	0
$\bar{c}_3 c_2$	0	0	1	0
$c_3 c_2$	1	0	0	0
$c_3 \bar{c}_2$	0	0	0	0

Hex [7]

$$= \bar{c}_3 \bar{c}_2 \bar{c}_1 + \bar{c}_3 c_2 c_1 c_0 + c_3 c_2 \bar{c}_1 c_0$$

Q2. Write the Verilog Module – Please refer to SevenHex.v

Q3. My Room is BA3155. Please check SevenHex.do. Screenshot of the same attached below.

File	Line	Code
/SevenHex/SW	1011	1011
St1	1010	1010
St0	0010	0010
St1	0001	0001
St1	0101	0101
/SevenHex/HEN0	0000011	0000011
St0	0001000	0001000
St0	0100100	0100100
St0	1111001	1111001
St0	0010010	0010010
St0		
St0		
St0		
St0		
St1		
St1		