CSEN2011	COMPUTER ORGANIZATION AND ARCHITECTURE	L	T	P	S	J	C
		2	1	0	0	0	3
Pre-requisite	Digital Logic Circuits						
Co-requisite	**None**						
Preferable exposure	**None**						

Course Description:

Computer Architecture and Organization provides a comprehensive knowledge on the structure and behaviour of computer hardware architecture and application of the design concepts. The basicconcepts of this course can have a view as to how a computer system works. This course enables the students to learn the basics of hardware components from basic gates to memory and I/O devices and instruction set architectures.

Course Educational Objectives:

- Attain the knowledge of fundamental circuit components and techniques for designing the circuits
- Describe and understand the processor memory hierarchy
- Understand the concepts of interrupts and I/O devices
- Attain the general knowledge of advances in microprogramming and Their implementation in computer design
- Experience the design process in the context of a reasonable size hardware system

UNIT 1 Register Transfer and Micro operations: **8 hours**

Register transfer language, register transfer, bus and memory transfers, arithmetic micro-operations, logic micro-operations, shift micro-operations, arithmetic logic shift unit

UNIT 2 Basic Computer Organization and Design 11 hours

Basic Computer Organization and Design Instruction codes, computer registers, computer instructions, timing and control, instruction cycle, memory-references instructions, input-output and interrupt, complete computer description. Design ofthe basic computer, Design of accumulator logic. Micro programmed Control: Control memory, address sequencing, micro program example, Design of control unit.

UNIT 3 Central Processing Unit 10 hours

Central Processing Unit: Introduction, general register organization, stack organization, instruction formats, addressing modes, data transfer and manipulation, program control.

Pipeline and Parallel Processing: Parallel processing, pipelining, arithmetic pipeline, instruction pipeline.

Computer Arithmetic: Introduction, addition and subtraction, decimal arithmetic unit, Booth's multiplication algorithm.

UNIT 4 Input-Output Organization 8 hours

Peripheral devices, I/O Interface, Asynchronous Data Transfer,Modes of Transfer, Priority Interrupt, DMA, I/O Processor, Serial Communication.

UNIT 5 Memory Organization 8 hours

Memory Hierarchy, Main Memory, Auxiliary Memory, AssociativeMemories, Cache Memory, Virtual Memories, Memory Management Hardware

TextBooks:

1. M. Morris Mano, Computer System Architecture, 3/e, Pearson education, 2008

References:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization,5/e, McGraw Hill,2001
2. John P. Hayes, Computer Architecture and Organization, 3/e, McGraw Hill, 1998.
3. William Stallings, Computer Organization and Architecture, 6/e, Pearson PHI, 2012.

Course Outcomes:

After successful completion of the course the student will be able to:

1. Classify the machine's instruction set architecture (ISA) including basic instruction fetchand execute cycles, instruction formats, control flow, and operand addressing modes
2. Build the design and functioning of a machines central processing unit (CPU) includingthe data path components (ALU, register file) and the control unit
3. Understand the basic input/output functioning including program controlled I/O andinterrupt I/O
4. Analyze the organization of different types of memories
5. Analyze the performance of processors and cache

CO-PO Mapping:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	1	2									1	2	2
CO2	2	2	2	2		2			2				1	2	2
CO3	1	2	1	2					2				2	2	2
CO4	1	1	1	2									2	2	2
CO5	1	1	2	2									2	2	2

Note: 1 - Low Correlation 2 - Medium Correlation 3 - High Correlation

APPROVED IN:

BOS : 06-09-2021 **ACADEMIC COUNCIL: 01-04-2022**

SDG No. & Statement:

SDG Justification: