SPECIALISED THIRD YEAR LABORATORY (SKEE3742)

LAB REPORT

VLSI SYSTEM DESIGN LABORATORY

DESIGN OF 4-BIT COUNTER

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Design of a 4-bit Counter

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***Abstract*— This study was to design the 4 bit counter. The 4 bit counter must had the counting sequence which included 9 digits, which was starting from 0 until 8 and back to 0 again. The 4 bit counter was designed from the transistor level of the gates and flip flop until the layout of 4 bit counter formed. The software, Cadence 6.1 EDA was used to the design of 4 bit counter. In summary, the 4 bit counter able to count from 0, 1, 2, 3, 4, 5, 6, 7, 8 and back to 0 again once 8 reached.**

I. INTRODUCTION

VLSI transistor layout design is a crucial and fundamental knowledge that every VLSI designer should know. This project requires us to design and layout a 4-bit counter using Cadence 6.1 EDA tools software. The objectives include simulating the schematic diagram design using Quartus II Tools, designing its schematic and layout design in Cadence 6.1 EDA tools software, testing the Design Rules Check (DRC) and Layout Versus Schematic (LVS), extracting each layout and simulating the netlist to verify its correct functionality and characterizing the performance (delay, power, critical path and area).

II. PROCEDURES

1. The state diagram was constructed with the sequence of 0, 1, 2, 3, 4, 5, 6, 7, 8 and reverse to 0 again once 8 reached.
2. The schematic diagram of the 4 bit counter was designed and verified by the Quartus II.
3. The transistor level of inverter, NAND gates, NOR gates, transmission gates and D flip flop was designed using Cadence 6.1 EDA.
4. The schematic diagram of XOR gates was constructed by schematic of transmission gates and NOT gates.
5. Then, T flip flop was constructed using the cell view of XOR gates and D flip flop.
6. The 4 bit counter was constructed using the schematic of T flip flop, NAND gates and NOR gates.
7. The schematic diagram was verified through simulation process.
8. After that, the layout of inverter was draw out and verified using DRC and LVS process.
9. The step 8 was repeated until all the component layout formed and verified sing DRC and LVS.

III. QUARTUS SIMULATION

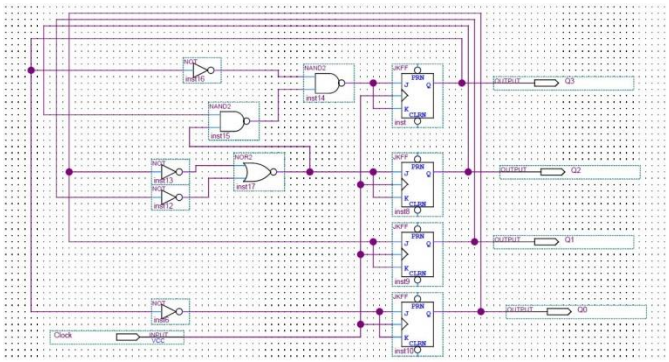

Fig 1. Gate-level Schematics

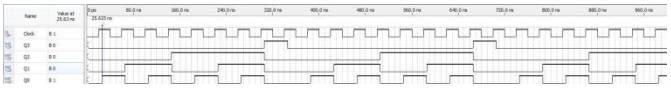

Fig 2. Quartus Simulation Waveform

From the timing waveform, the output propagation delay is 5.625ns as counted from the input.

IV. STICK DIAGRAM DESIGN

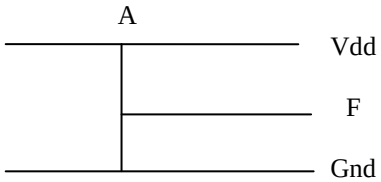

Fig 3. NOT stick diagram

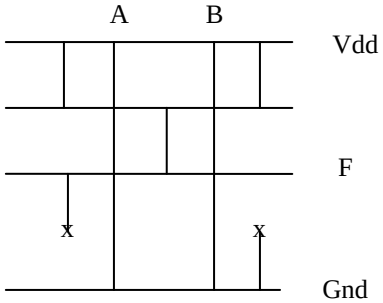

Fig 4. NAND gate

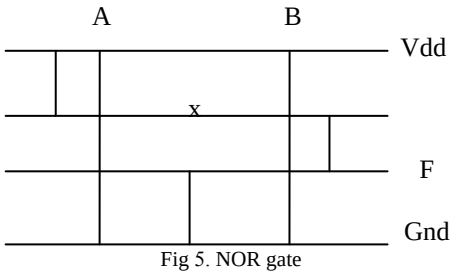

Fig 5. NOR gate

V. DATA AND RESULTS

1. The counter is designed using 4 T flip flop, a NOR gate and two NAND gates. For the entire circuit, it is built using 96 transistors. The figure below shows the top level transistor schematics. For lower level schematics, refer to Appendix.

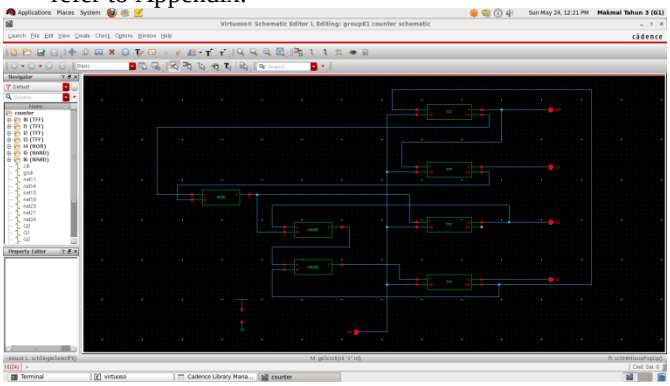
Fig 6. Counter Transistor Schematics

2. The counter circuit is simulated and the results of the simulations are as shown below:

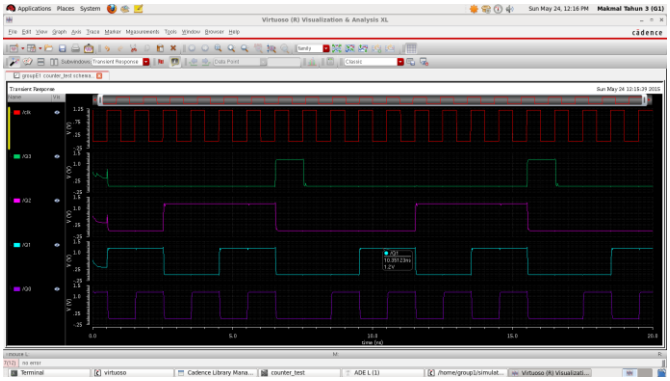
Fig 7. Simulation before Extraction

3. The layout of the circuit is generated after the schematics are completely drawn and other lower level layouts are drawn.

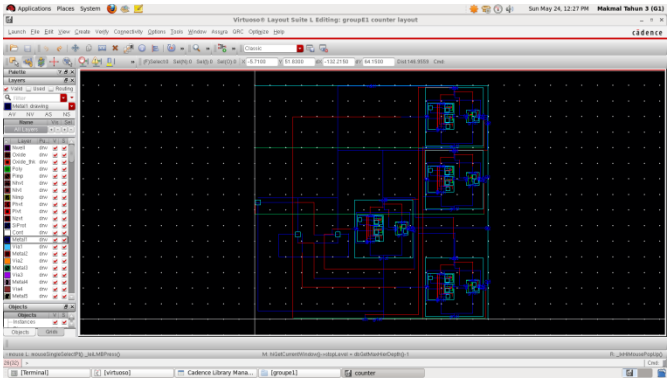
Fig 8. Layout of Counter Circuit

4. DRC and LVS test are run on the top level layout and their verifications are shown below:

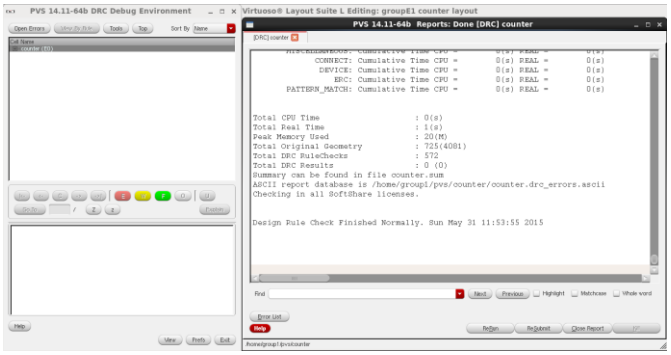
Fig 9. DRC verification

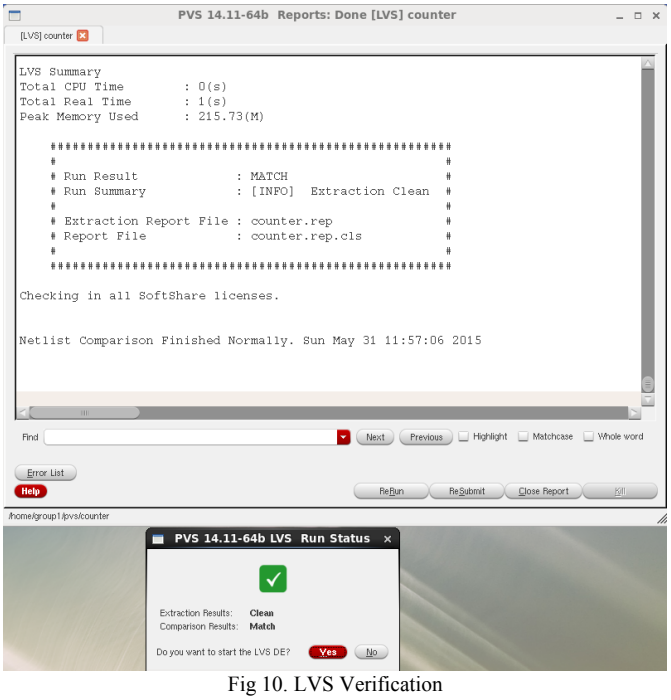

Fig 10. LVS Verification

5. After running the LVS test, the parasitic capacitance and resistance is been extracted as shown below:

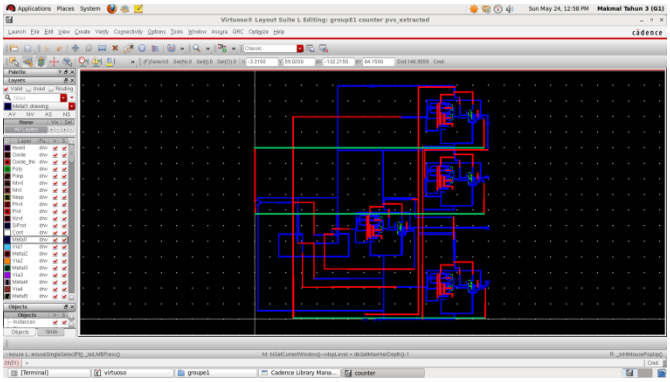

Fig 11. PVS extracted layout

6. After extracting the parasitic capacitance and resistance, the counter circuit is simulated and the results of the simulations are as shown below:

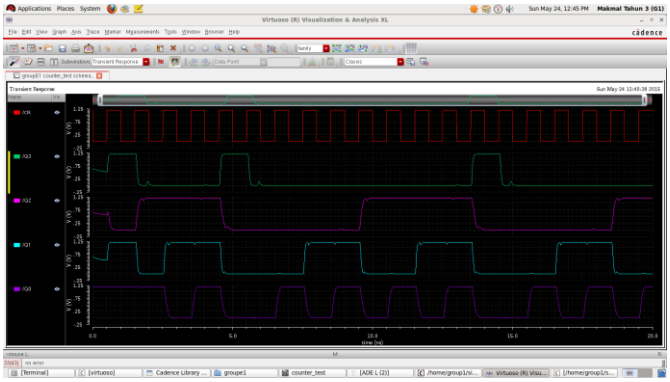

Fig 12. Simulation after extraction

7. From the figure above, it can be clearly seen that the counter circuit functionality is still correct even after extracting parasitic capacitance and resistance.
8. The propagation delay of the counter circuit is calculated and tabulated in the table below:

TABLE I. PROPAGATION DELAY OF COUNTER CIRCUIT

Transition	Maximum propagation delay (ns)		
	t_{pLH}	t_{pHL}	t_p
1	0.093143	-	0.093143
2	0.060885	0.125248	0.0930665
3	0.093054	-	0.093054
4	0.092197	0.126464	0.1093305
5	0.09314	-	0.09314
6	0.06085	0.12523	0.09304
7	0.09296	-	0.09296
8	0.06104	0.12671	0.093875
9	-	0.08444	0.08444

9. From the table above, the transition that has the worst propagation delay is transition 4 which is from 0011(3) to 0100(4). The transition that has the best propagation delay is transition 9 which is from 1000(8) to 0000(0).

VI. DISCUSSION

1. This 4 bit counter was implemented by 4 basic combinational logic circuits (inverter, NAND gate, NOR gate and transmission gate) and a sequential logic circuit which was D-flipflop. The XOR gate was built by using transmission gates and inverters whereas the T-flipflop was implemented by combining the output from the XOR gate to the input of the D-flipflop.
2. While designing the D-flipflop, gate level design was avoided in order to prevent large fan-in effect that will cause long delay in the output. Thus, D-flipflop was designed in transistor level.
3. From the simulation output waveforms of the extracted 4 bit counter, it can be seen that there was slope at the edge of the output waveforms and some peaks and ditches in the waveforms. All these were caused by resistors and capacitors added in to the 4 bit counter circuit. The capacitors needed time to charge and discharge which result in slope at the edge of the waveform.
4. By comparing the input and output waveform, notice that there are certain time delay in between them. Each different output transition will have different time delay because different transitions for example 0⇢1 will passed through different number of transistors inside the circuit. The greater number of transistors passed through will result in longer time delay.
5. At the first positive edge clock cycle, the output wave form did not start at 0. This is because on power-up, the counter could be any possible states. This is due some build up charges that are not discharged completely during starting. Hence, it will start from a random state. However, eventually the counter enters a valid value such that the sequence remains correct and circuit behaves as designed.

VII. CONCLUSION

A simple 4 bit counter can be designed and implemented by using combinational logic gates and sequential logic gate together. To obtain 4 bit counter with better performance in term of time delay, the sequential logic circuit must be designed in transistor level instead of gate level to reduce the fan-in effect. Different transition output will have different time delay compared to input signal depends on the number of transistor passed through in the circuit.

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