FAKULTI KEJURUTERAAN ELEKTRIK

UNIVERSITI TEKNOLOGI MALAYSIA

KAMPUS SKUDAI

JOHOR

SKEL 3742
VLSI SYSTEM DESIGN LAB

Lab Project 2: Traffic Light System

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Project Introduction

The traffic light at a junction between a main road and a small road is controlled by two motion sensors as shown in Figure 1 below. The two main traffic lights, SA and SB take turns to change to green every 12 seconds once. However, if there is a car detected by motion sensors, M1 or M2, then after the current main traffic light changes to red, SC or SD are changed to green for 12 seconds followed by the resumed process of change between SA and SB. If both motion sensors are activated at the same time, SC is given priority to become green for 12 seconds followed by SD for 12 seconds.
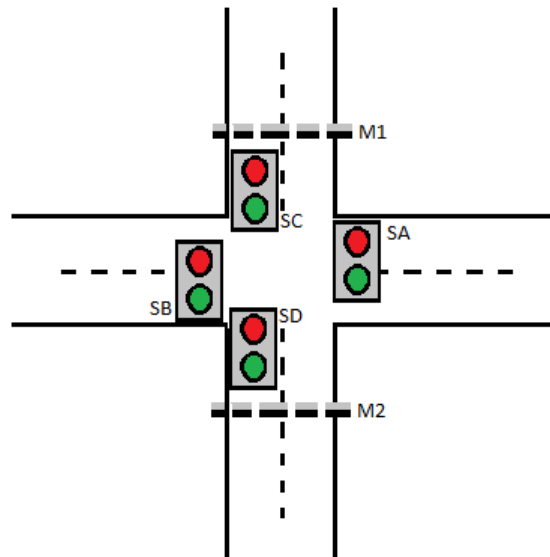

Figure 1: Traffic Light System

The objectives of this project are:

1. To construct truth table based on project specifications and design the traffic light system using combinational and sequential logic design.

2. To draw the combinational and sequential logic circuit of the traffic light system using schematic design entry/hardware design language (HDL) coding and verify its function using Altera Quartus II Tools software.

3. To prototype and demonstrate the design of the system using Altera FPGA DE2 board.

Project Task

Design the traffic light system using Quartus II schematic entry/HDL coding. Write a report with the well-presented design steps, simulation results and FPGA prototyping methodology are expected to be produced at the end of the project after the third session of the lab.

Some design guidelines:

1. Design a circuit for the traffic light using multiplexers, counters, adders and similar logic blocks.
2. For your design, use appropriate gates, components and mega functions from the Quartus II system library.
3. Use a mod-12 counter to do countdown for the traffic light change.
4. Use registers or flip-flops to for storage.
5. The motion sensor inputs will eventually be connected to the toggle switches on the DE2 board.
6. The countdown for the traffic light will eventually be displayed on the 7-segment displays on the DE2 board.

     Identify input and output of your system, encoding method, circuit topology and suitable algorithm to be used. Design the system using combinational and sequential logic gates and verify the design using Quartus II CAD Tool. Final task is to prototype and demonstrate your system using FPGA DE2 board. Refer to Quartus II and FPGA tutorial to help you to implement this project.

Week 1:

Design the traffic light system including a block diagram for the datapath and a state machine diagram for the control unit. Below is a sample datapath unit for your reference. Use this as an example to design your datapath.
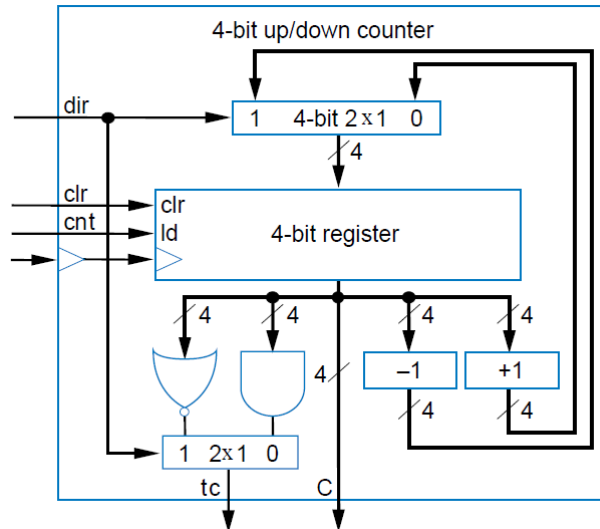

Figure 2: Up/Down Counter (F. Vahid, Chapter 4, Digital Design, 2006)

Week 2:

Design the datapath and control unit using schematic entry or Verilog HDL. Verify your design by using simulation waveform to check design correctness.

Week 3:

Implement the completed traffic light on the Altera DE2 FPGA board. Use the toggle switches for input and 7-segment display as well as LEDs for output.