Branch : CSE & IT Batch : Hinglish

WEEKLY TEST – 06

Subject : Operating System

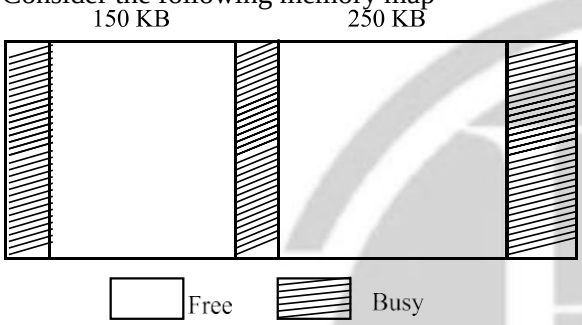
Topic : Memory Management

Maximum Marks 19

Q.1 to 5 Carry ONE Mark Each

[MSQ]

1. Consider the following memory map



The successive request of the processes are 50 KB, 200 KB, 50 KB and 100 KB.

Which of the following variable partitioning scheme satisfies the given process request?

(a) Best fit (b) Worst fit

(c) first fit (d) Next fit

[MSQ]

2. Assume, a system is suffering from thrashing which of the following factor(s) will help in recovery the system from thrashing?

(a) Install faster CPU

(b) Decrease the degree of multiprogramming

(c) Install more main memory

(d) Install more disk space

[NAT]

3. Consider an inverted paging architecture that supports logical address and physical address of sizes 30 bits and 24 bits respectively. The system is characterized with 8KB page size. If the memory is byte addressable, the difference in the conventional and inverted page table size is_____(in kilobits)

(Page table entry size in the conventional and inverted page table is 4 bytes.)

[NAT]

4. Consider a segmented paging architecture which supports 8GB logical and physical address spaces. The segment number requires 19 bits to represent all the segments in the logical address space. The maximum size of a page of the segment such that the page table of the segment fits into a memory frame is _____(in bytes)

(Assume the page table entry size of the segmented page table is 4 bytes)

[MCQ]

5. Consider the following statements:

S_1: Paging is a continuous memory management scheme.

S_2: In fixed partition scheme, all the partitions are of same size.

Which of the given statement(s) is/are CORRECT?

(a) S1 only

(b) S_2 only

(c) Both S_1 and S_2

(d) Neither S_1 nor S_2

Q.6 to 12 Carry TWO Mark Each

[MSQ]

6. Consider a demand paging architecture that is characterized with page fault rate 'P' and page fault service time is given as $3t^2 - 2t + 24$. The optimal value of the page hit rate such that the effective main memory access time is minimized is-

(Assume, the time required to access a frame in main memory is t)

(a) $\frac{1}{3-6t}$ (b) $\frac{1}{6(1-t)}$

(c) $\frac{5-t6}{6-t}$ (d) $\frac{2-6t}{3(1-2t)}$

[MCQ]

7. Consider the virtual page reference string
2021, 2022, 2023, 2024, 2022, 2021, 2025, 2023, 2022, 2024, 2026

Assume there are three-page frames which are initially empty. Let LRU, FIFO and Optimal denote the number of page faults under the corresponding page replacement policy. Which of the following statement(s) is/are CORRECT?

(a) Optimal<LRU<FIFO

(b) Optimal<LRU=FIFO

(c) Optimal = LRU

(d) Optimal = FIFO

[MCQ]

8. Consider a multi-level paging architecture having logical address of 48 bits and physical address of 32 bits. The operating system uses 3-level paging for logical to physical address translation. Assume, memory is byte addressable and page table entry size is 128 bits. What should be the optimal page size such that the first level page table fits in a memory frame?

(a) 4 KB (b) 16 KB

(c) 32 KB (d) 8 KB

[NAT]

9. consider a system with paging hardware in which a regular memory access takes 200 nanosecond and servicing a page fault takes 10 MS.

The TLB hit ratio is 80% and the page fault rate is one in every 5000 instructions. The effective average instruction execution time is_____nanosecond. (Assume TLB access time is 50 ns.) (Upto 3 decimal places)

[MSQ]

10. Let a memory have four free blocks-

P = 4K, Q = 8K, R = 10K, S = 2K

These blocks are allocated using best-fit strategy. The allocation request of the processes are given as-

Arrival time	Requesting Process	Requested size	Usage Time
0	A	2K	3
1	B	9K	6
2	C	2K	3
3	D	4K	2
4	E	4K	4
5	F	9K	3

Which of the following statements is/are CORRECT?

(a) At t = 10, all the process finish execution

(b) The process F has to wait for 3 units of time

(c) The process C, D and E are allocated Block P.

(d) D is allocated block Q.

[MCQ]

11. Consider a system using with TLB.

What is hit ratio is required to reduce the effective memory access time from 'E' ns to 'P' ns using TLB? (Assume that TLB access time is 'T' ns).

(a) $\frac{2P + 2PT + 2E}{E}$ (b) $\frac{(P + T + E)2}{(2T + E)}$

(c) $\frac{2[T + E - P]}{E}$ (d) None of these

[MCQ]

12. Consider a logical address of 32 Bit and page size of 8 KB. The page table is in hardware with one 32 Bit word per entry.

When a process starts the page table is copied to hardware from memory at one word every 100 ns. If each process rans for 100msec. (including the time to load the page table). What fraction of CPU time is devoted to loading the page tables?

(a) 20% (b) 52%

(c) 30% (d) None of these

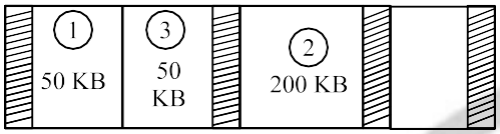
Answer Key

1. **(a, b)**
2. **(b, c)**
3. **(4032)**
4. **(256)**
5. **(d)**
6. **(d)**
7. **(b)**
8. **(c)**
9. **(253.992)**
10. **(a, d)**
11. **(c)**
12. **(b)**

Hints and Solutions

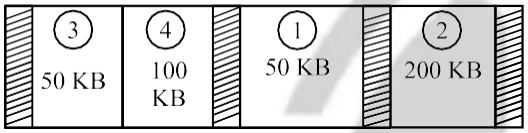
1. (a, b)

First fit



100 KB request cannot be satisfied

Worst fit



Next fit works after last allocation point.

(50KB, 200KB, 50KB) can be serviced but 100 KB can't be.

2. (b, c)

The system can recover from thrashing by-

- decreasing the degree of multiprogramming
- Installing more main memory /allocating more frames to process undergoing thrashing.

3. (4032)

Conventical page table size $= \frac{2^{30}}{2^{13}} \times 2^2$ B

$= 2^{19}$ B $= 2^9$ KB

$= 2^{12}$ K bits

Inverted page table size $= \frac{2^{24}}{2^{13}} \times 2^2$ B

$= 2^{13}$ B $= 2^3$ KB

$= 2^6$ K bits

Difference in K Bits $= 2^{12} - 2^6$

$= 4032$

4. (256)

Logical address $= \log_2 = 8$ G

Segment size $= (33 - 19)$ bits

$= 14$ bits

Let the page size of the segmented page table be $2x$.

Page table size $= \frac{2^{14}}{2^x} \times 4$ bytes

$= 2^{16-x}$ bytes

Segmented page table size = frame size

$2^{16-x} = 2^x$

$16 - x = x$

$2x = 16$

$x = 8$

$\therefore$ Page size of the segment $= 2^8 = 256$ Bytes

5. (d)

S_1: INCORRECT. Paging is non-contiguous memory management scheme.

S_2: INCORRECT. In fixed partitioning, the number of the partitions are fixed. Partitions may vary in size.

6. (d)

Effective Main memory $= P \times S + (1 - P) \times M$

Access time (EMAT)

P: Page fault rate

S: Page fault server time

M: Main memory access time

EMAT $= P \times (3t^2 - 2t + 24) + (1 - P) \times t$

$\frac{d}{dt}(\text{EMAT}) = \frac{d}{dt}[P \times (3t^2 - 2t + 24) + (1-P) \times t]$

$\frac{d}{dt}(\text{EMAT}) = P \times (6t - 2) + (1 - P)$

For minimizing EMAT-

$P \times (6t - 2) + (1 - P) = 0$

$P \times (6t - 2 - 1) + 1 = 0$

$P \times (6t - 3) = -1$

$P = \frac{1}{3 - 6t}$

Page hit rate = $1 - P = 1 - \frac{1}{3-6t} = \frac{3-6t-1}{3-6t} = \frac{2-6t}{3-6t}$

7. (b)

LRU

2024	2022	2021	2025	2023	2022	2024	2026
~~2021~~	2024	2024	~~2024~~	2025	2025	~~2025~~	2024	2024
2022	2022	2022	2022	~~2022~~	2022	2023	~~2023~~	2026
2023	2023	~~2023~~	2021	2021	~~2021~~	2021	2022	2022

Number of page faults = 3 + 7 = 10

FIFO

~~2021~~	2024	2024	2024	~~2024~~	2023	2023	~~2023~~	2026
2022	2022	~~2022~~	2021	2021	~~2021~~	2022	2022	2022
2023	2023	2023	~~2023~~	2025	2025	~~2025~~	2024	2024

Number of page faults = 3 + 7 = 10

Optimal –

2021	~~2021~~	~~2025~~	2023
2022	2022	2022	
~~2023~~			

Number of page faults = 3 + 4 = 7

8. (c)

Let page size be 'x' by xs

First time paging –

Page table size = $\frac{2^{48}}{x} \times 16$ B

$= \frac{2^{52}}{x}$ B

2nd Time paging–

Page table size = $\frac{2^{52}}{x} \times 16$ B

$= \frac{2^{56}}{x^2}$ B

3rd time paging–

Page table size = $\frac{2^{56}}{x} \times 16$ B

$= \frac{2^{60}}{x^3}$ B

$\Rightarrow \frac{2^{60}}{x^3} = x$

$= 2^{60}$ B $= x^4$

$= x = 2^{15}$ bytes = 32 KB

9. (253.992)

EMAT $\Rightarrow$ x (C + M) + (1– x) [P × S+ (1 – P) × M + C]

Where X = TLB = hit rate

C = TLB access time

M = Main memory access time

P = Page fault rate

S = Page fault service time

$\Rightarrow$ EMAT = $0.8 (50 + 200) + 0.2 \left\lceil \frac{1}{5000} \times 10,000 + \frac{4999}{5000} \times 200 + 50 \right\rceil$

$\Rightarrow$ 253.992 nanoseconds

10. (a, d)

	0	1	2	3	4	5	6	7	8	9	10
4K			C	C	C	E	E	E	E		
8K				D	D						
10K		B	B	B	B	B	B	F	F	F	
2K	A	A	A								

(F has to wait till t = 7)

E has to wait for 1 unit as its request size is 4k

11. (c)

Without TLB:

EMAT = 2 × M

E = 2M

$M = \frac{E}{2}$

With TLB:

EMAT = x (C + M) + (1 – x) (C + 2M)

$P = x\left(T + \frac{E}{2}\right) + (1-x)\left(T + 2 \times \frac{E}{2}\right)$

$P = x\left(T + \frac{E}{2}\right) + (1-x)(T + E)$

$P = x\left(T + \frac{E}{2}\right) + T + E - Tx - Ex$

$P - T - E = x\left(T + \frac{E}{2}\right) - x(T + E)$

$P - T - E = x\left(T + \frac{E}{2} - T - E\right)$

$P - T - E = x\left(-\frac{E}{2}\right)$

$x = \frac{2(T + E - P)}{E}$

12. (b)

Logical address = 32 bits

Page size = 8 kb

Number of Entries in page table = $\frac{2^{32}}{2^{13}}$

= 219 entries

= 512 k entries

- For 1 word copied from memory to hardware = 100 ns
- For 1 entry time to copied from memory to hardware = 100 ns
- Total CPU time to load the entries = 100 × 512 k ns

Total time = 100ms

$= \frac{\%\ \text{CPU time}}{\text{loading of page table}}$

$= \frac{512\ k \times 100\ ns}{100\ \text{ms}}$

$= \frac{512 \times 1024 \times 10^{-9} \times 10^{3}}{100}$

$= \frac{512 \times 1024}{100} \times 10^{-6}$

$= 512 \times 1024 \times 10^{-6}$

$= 524288 \times 10^{-6}$

$= .5242 \times 100$

$\cong 52\%$

Hence, option (b) is correct.