CS & IT — Batch : Hinglish

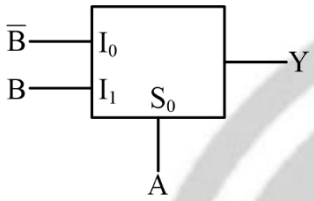
Weekly Test - 03
Digital Logic
Combinational Circuit

Time Duration - 50 Min **Maximum Marks –** 20

Note : Negative Marking - 1/3, NAT no negative marking
{For MSQs no part marking no negative marking(from week onwards)}

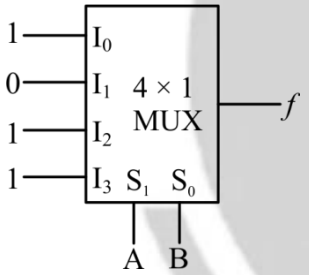
Part A : 1 to 6 questions each will carry 1 marks (MCQs + NAT)

1. The logic gate of given multiplexer circuit is



(a) AND (b) X-OR
(c) XNOR (d) NAND

2. The logic function implemented by 4 × 1 mux, is



(a) A + B (b) $A + \overline{B}$
(c) $\overline{A} + B$ (d) $\overline{A} + \overline{B}$

3. How many AND gates are required for a 1 × 8 Demux ?

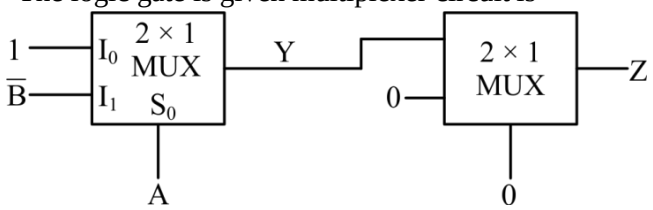
4. A multiplexer with a 4-bit data select input is a
(a) 4 × 1 mux (b) 16 × 1 mux
(c) 8 × 1 mux (d) 2 × 1 mux

5. A designer has multiplexer units of size 2 × 1 and multiplexer of size 16 × 1 is to be realized. The number of units of 2 × 1 mux is required will be _____.

6. How many OR gates are required for an octal to binary encoder?
(a) 3 (b) 2
(c) 8 (d) 10

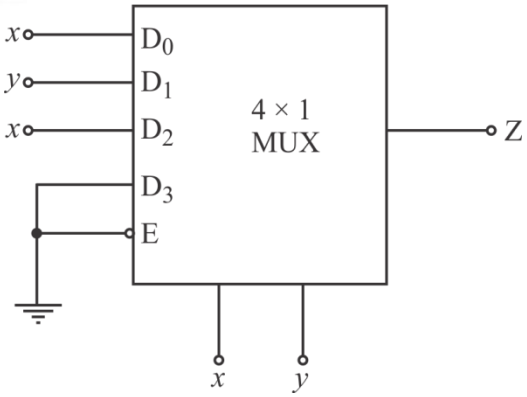
Part A : 7 to 13 questions each will carry 2 marks (MCQs + NAT)

7. The logic gate is given multiplexer circuit is



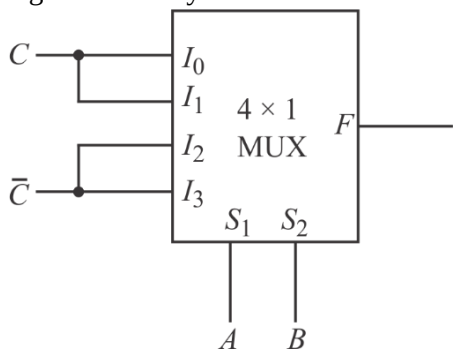
(a) AND (b) XOR
(c) NAND (d) NOR

8. The logic function implemented by 4 × 1 MUX, is



(a) $Z = xy$ (b) $Z = x + y$
(c) $Z = \overline{x + y}$ (d) $x \oplus y$

9. The logic realized by the circuit shown in figure is



(a) $F = A \odot C$ (b) $F = A \oplus C$

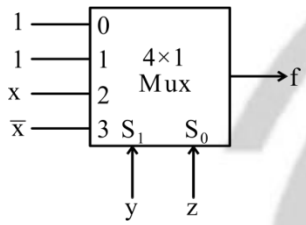
(c) $F = B \odot C$ (d) $F = B \oplus C$

10. Which one of the following circuits implements the Boolean function given below?

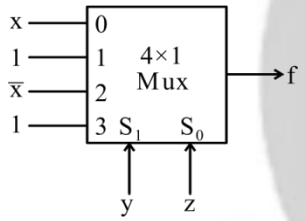
$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6$

where m_i is the i^{th} minterm.

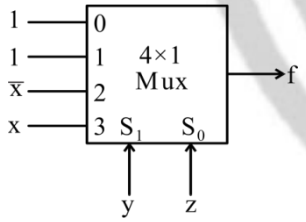
(a)



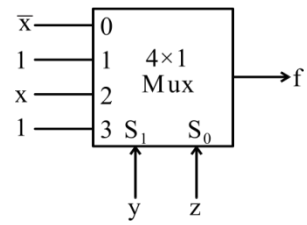
(b)



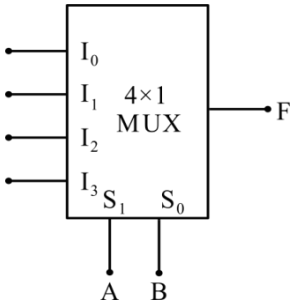
(c)



(d)



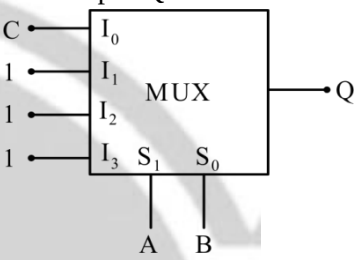
11. In the 4 × 1 multiplexer, the output F is given by F = A ⊕ B. Find the required input $I_3I_2I_1I_0$.



(a) 1010 (b) 0110

(c) 1000 (d) 1110

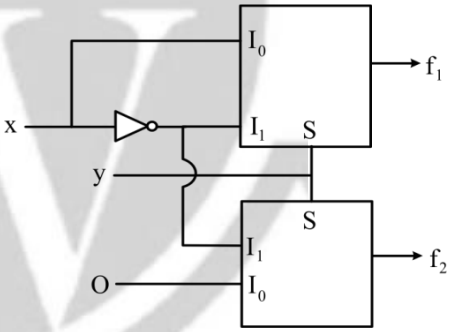
12. The combinational logic circuit shown in the given figure has an output Q which is



(a) ABC (b) A + B + C

(c) A ⊕ B ⊕ C (d) A . B + C

13. Minimum number of NAND gates required to implement following combinational circuit are_____.



Answer Key

1. **(c)**
2. **(b)**
3. **(8)**
4. **(b)**
5. **(15)**
6. **(a)**
7. **(c)**
8. **(d)**
9. **(b)**
10. **(a)**
11. **(b)**
12. **(b)**
13. **(5)**

Hints and solutions

1. **(c)**

$Y = \bar{S}_0 I_0 + S_0 I_1$

$Y = \bar{A}\bar{B} + AB$

$Y = A \odot B$

2. **(b)**

$f = 1.\bar{A}\bar{B} + 0.\bar{A}B + 1.A\bar{B} + AB.1$

$f = \bar{A}\bar{B} + A\bar{B} + AB$

$f = \bar{B} + AB = (\bar{B} + B)(\bar{B} + A)$

$f = A + \bar{B}$

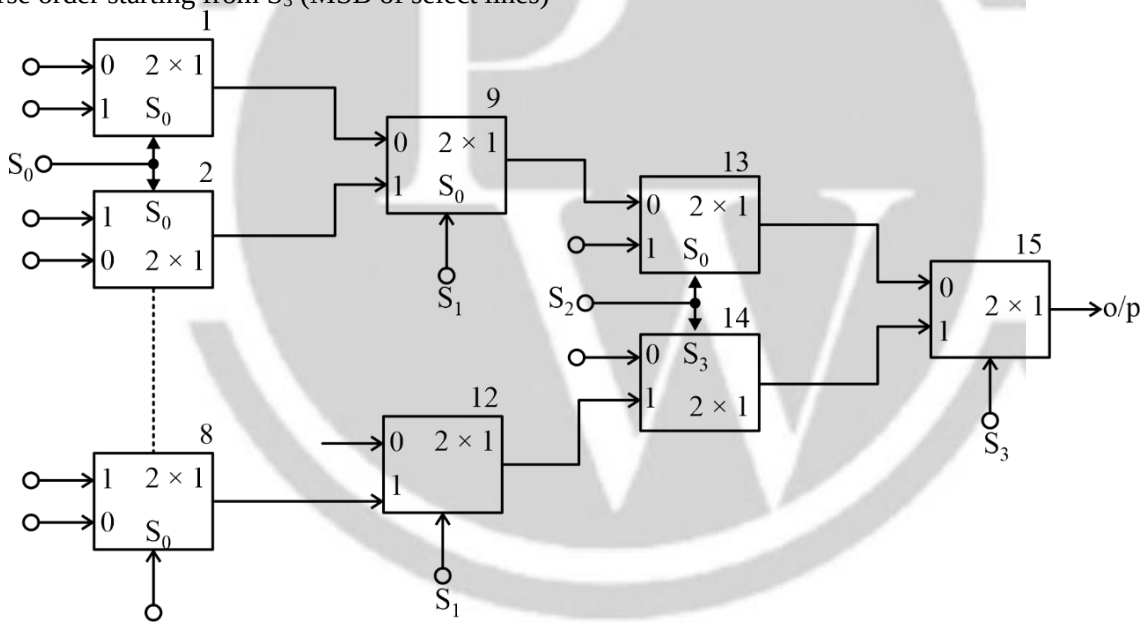
3. **(8)**

Number of AND gates = Number of output in DEMUX

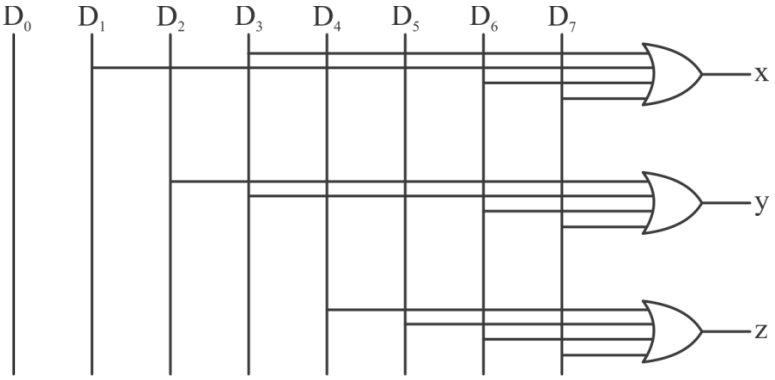
4. **(b)**

16 × 1 mux is implemented with 4-bit data select input.

5. Number of units of 2 × 1 MUXs required = 8 + 4 + 2 + 1 = 15 as demonstrated below. Select lines are assigned in reverse order starting from S_3 (MSB of select lines)



6. **(a)**



7. **(c)**

$Y = \bar{A} + \bar{A}B = \bar{A} + B$

$Z = \bar{O}.Y + O.O$

$Z = Y = \bar{A} + \bar{B}$

$Z = \overline{AB}$

NAND Gate

8. **(d)**

$z = \bar{x}\,y\,x + \bar{x}\,y\,y + x\bar{y}\,x + x\,y \cdot 0$

$z = \bar{x}\,y + x\bar{y}\,x$

$z = \bar{x}\,y + x\bar{y}$

$z = x \oplus y$

9. **(b)**

$F = \bar{A}\bar{B}C + \bar{A}BC + AB\bar{C} + ABC$

$F = \bar{A}C(B + \bar{B}) + A\bar{C}(B + \bar{B})$

$F = \bar{A}C + A\bar{C}$

$F = A \oplus C$

10. **(a)**

$f = \bar{y}\,\bar{z} \cdot 1 + \bar{y}z \cdot 1 + y\,\bar{z} \cdot x + y\,z\,\bar{x}$

$f = x\,\bar{y}\,\bar{z} + \bar{x}\,\bar{y}\,\bar{z} + x\,\bar{y}\,z + \bar{x}\,\bar{y}\,z + x\,y\,\bar{z} + \bar{x}\,y\,z$

$f = \bar{x}\,\bar{y}\,\bar{z} + \bar{x}\,\bar{y}\,z + \bar{x}\,y\,z + x\,\bar{y}\,\bar{z} + x\,\bar{y}\,z + x\,y\,\bar{z}$

$f(x, y, z) = (m_0, m_1, m_3, m_4, m_5, m_6)$

11. **(b)**

$F = \bar{A}\bar{B}\,I_0 + \bar{A}B\,I_1 + AB\bar{I}_2 + AB\,I_3$

Put $I_0 = 0$, $I_1 = 1$, $I_2 = 1$, $I_3 = 0$

$F = \bar{A}B + AB\bar{}$

$F = A \oplus B$

12. **(b)**

$Q = \bar{A}\bar{B}C + \bar{A}\bar{B} + AB\bar{} + AB$

$Q = \bar{A}\,(\bar{B}C + B) + A(\bar{B} + B)$

$Q = \bar{A}\,(\bar{B} + B)(B + C) + A\,Q$

$= A\,(\bar{B} + C) + A$

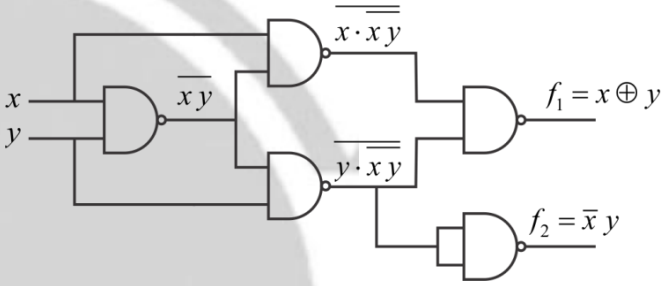
$Q = (\bar{A} + A)(A + B + C)$

$Q = A + B + C$

13. **(5)**

$f_1 = x\,\bar{y} + \bar{x}\,y = x \oplus y$

$f_2 = \bar{x}\,y$



Hence 5 NAND gate required.