CS & IT — Batch : Hinglish

Weekly Test - 05
Subject : Digital Logic
Topic : Sequential Circuit

Time Duration - 50 Min **Maximum Marks –** 20

Note : Negative Marking - 1/3, NAT no negative marking
{For MSQs no part marking no negative marking(from week onwards)}

Part A : 1 to 6 questions each will carry 1 marks (MCQs + NAT)

1. If the 5-bit ripple counter and 5-bit synchronous counter are having flip-flops with a propagation delay of 40 ns, then the total sum (x + y) of maximum delay in the ripple counter (x) and synchronous counter (y) will be_____(in ns)

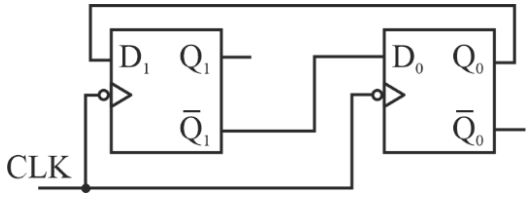
2. If the J-input of a J-K flip-flop is treated as input and an inverter is connected between J and K inputs, the J-K flip-flop becomes

(a) D Latch (b) D Flip Flop
(c) T Flip Flop (d) JK Flip Flop

3. Determine f_{max} for the 4-bit parallel carry synchronous counter, if t_{pd} for each flip-flop is 40ns and t_{pd} for each AND gate is 10ns

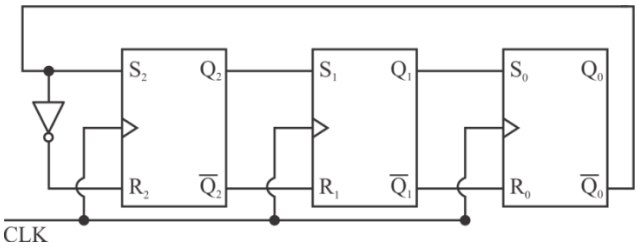
(a) 2 MHz (b) 0.2 MHz
(c) 20 MHz (d) 25 MHz

4. The two negative edge trigged D flip flops are interconnected as shown below. Assume initially Q_1Q_0=00. The outputs Q_1Q_0 of the circuit, will be

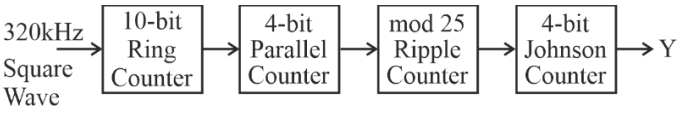


(a) 00, 01, 10, 11, 00
(b) 00, 01, 11, 10, 00
(c) 00, 11, 10, 01, 00
(d) 00, 10, 11, 01, 00

5. How many different output states the following circuit is having?



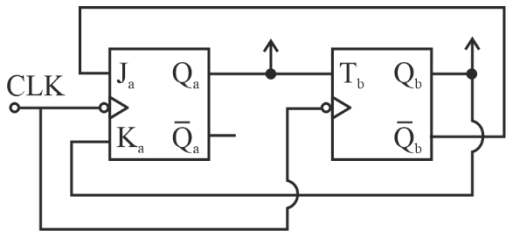
6. Various types of counters are cascaded as shown below. The signal available at output Y will have the frequency.



(a) 20Hz (b) 10Hz
(c) 320Hz (d) 160Hz

Part B: 7 to 13 questions each will carry 2 marks (MCQs + NAT)

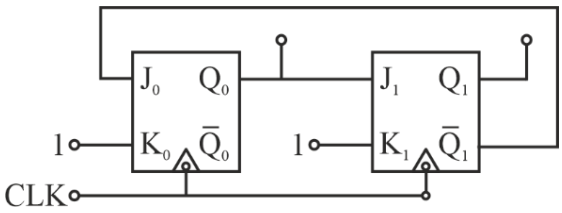
7. If the Q_a Q_b of counter shown below at clock time t_n is 10, then the state Q_a Q_b of counter at t_{n+3} (after 3 clock cycles) will be



(a) 00 (b) 01

(c) 10 (d) 11

8. Figure shows a mod-K counter, Here K is equal to



(a) 1 (b) 2

(c) 3 (d) 4

9. Consider the following conditions:

1. $t_p < \Delta t$ 2. $\Delta t < T$ 3. $t_p > \Delta t$ 4. $\Delta t < T$

Consider the following conditions:

Where t_p = pulse width, Δt = propagation delay of flip-flop and T = clock period. The race around condition in the flip-flop can be avoided if conditions_____

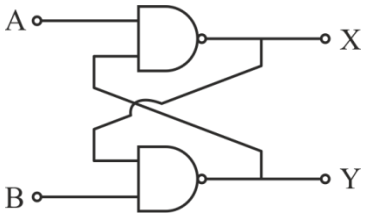
(a) 1 and 2 are correct

(b) 1, 3 and 4 are correct

(c) 2 and 3 are correct

(d) 2, 3 and 4 are correct

10. In the NAND latch shown below, initially A = B = 1 and then B is replaced by a sequence 10 10 10 ….., the outputs X and Y will be (assume initially X = 0 and Y = 1)



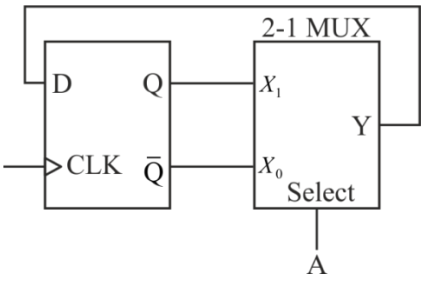
(a) fixed at 0 and 1 respectively

(b) fixed at 1 and 0 respectively

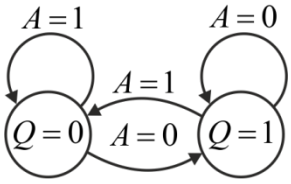
(c) X = 1010…. and Y = 0101

(d) X = 0101…. and Y = 1010

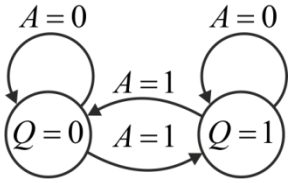
11. The state transition diagram for the logic circuit shown is



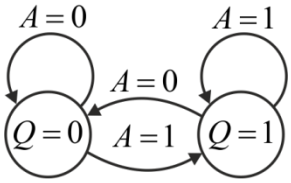
(a)



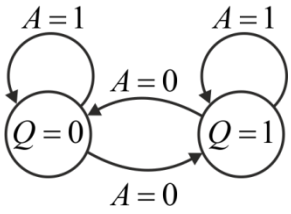
(b)



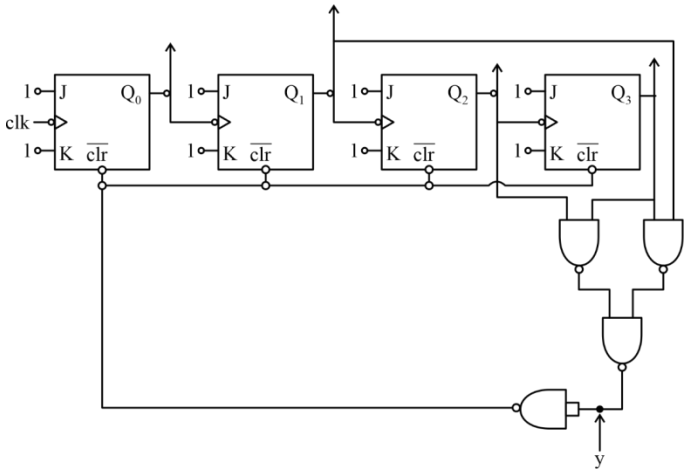
(c)



(d)



12. A circuit for truncated ripple counter together with a reset function labelled *y*, is shown below.



Then the reset function y can be expressed as

(a) $y = Q_3(Q_2 + Q_1)$

(b) $y = Q_3 + Q_2Q_1$

(c) $y = \overline{Q_3(Q_2 + Q_1)}$

(d) $y = \overline{Q_3 + Q_2Q_1}$

13. A 6 bit counter is designed with a switch *S*. Function of switch S is to switch the counter from up counter to down counter and vice-versa after MOD-no. of clock pulses irrespective of starting state of counter. Counter started with state $(101100)_2$ in up-counter mode then after how many clock-pulses it will be at $(110010)_2$ in down-mode condition of the switch _____.

Answer Key

1. (240)
2. (b)
3. (c)
4. (b)
5. (6)
6. (b)
7. (c)
8. (c)
9. (a)
10. (a)
11. (d)
12. (a)
13. (122)