Branch : CS & IT Batch : Hinglish

Weekly Test - 04
Digital Logic

Time Duration - 50 Min **Maximum Marks –** 20

Note : Negative Marking - 1/3, NAT no negative marking
{For MSQs no part marking no negative marking(from week onwards)}

Part A : 1 to 6 questions each will carry 1 marks (MCQs + NAT)

1. [NAT]

We have two types of digital units available:

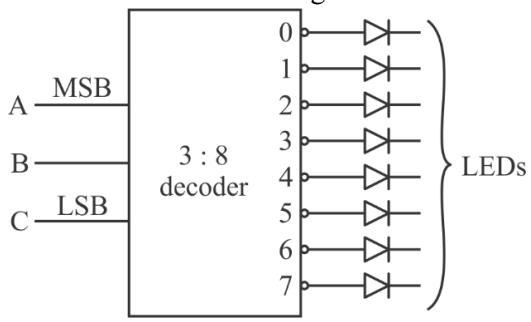
2 : 1 MUX $\rightarrow$ Cost 2 unit each

NOT gate $\rightarrow$ Cost 1 unit each

We have to implement half subtractor circuit then the minimum costing required to implement the circuit is _____ unit.

2. [NAT]

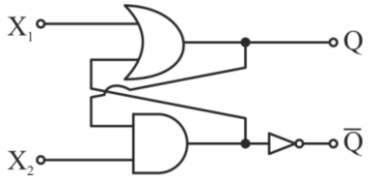
A 3 : 8 decoder circuit is as given below :



When applied input is ABC = $(110)_2$ then the sum of output pin numbers which will glow will be $(\_\_\_\_\_)_{10}$.

[MCQ]

3. The latching action of a latch shown below, is controlled by two inputs X_1, X_2. The invalid input combinational X_1, X_2 will be



(a) $X_1 = 1, X_2 = 0$ (b) $X_1 = 0, X_2 = 1$

(c) $X_1 = X_2 = 0$ (d) $X_1 = X_2 = 1$

4. [NAT]

Two numbers A & B are 2-bit numbers i.e. $A = a_1, a_0$ & $B = b_1b_0$. If we perform operation (A – B) using parallel subtractor with minimum no. of possible gates XOR, AND, OR, NOT etc. then minimum number of 2-input XOR gate required will be _____.

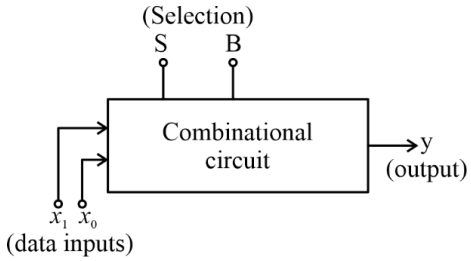
5. [MCQ]

The design of a combinational circuit is attempted as demonstrated below.

(i) For S = 0, y = 0 regardless of status of B

(ii) For S = 1 and B = 0, $y = x_1$

(iii) For S = 1 and B = 1, $y = x_0$



The minimum number count of 3-input NAND gates required to complete the design, will be

(a) 3 (b) 2

(c) 4 (d) 1

6. [NAT]

How many don't care inputs are there in a BCD adder?

Part B: 7 to 13 questions each will carry 2 marks (MCQs + NAT)

7. **[MCQ]**

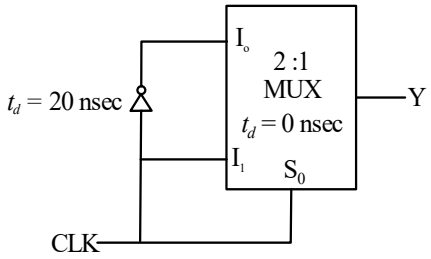
In a 4-bit carry look ahead adder, the X-OR and AND/OR gate has delay of 5ns each. The sum will appear after delay of

(a) 10 ns (b) 20 ns

(c) 15 ns (d) 40 ns

8. **[NAT]**

A MUX circuit is as shown below:

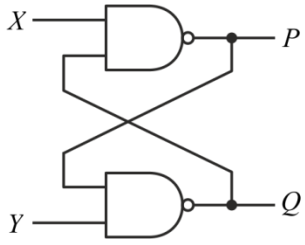


Clock input has frequency of 10 MHz, then duty cycle of the output waveform at output Y will be_____. (**up to two decimal places**).

9. The following binary values were applied to the *X* and *Y* inputs of the NAND latch shown in the figure in the sequence indicated below :

$X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1$

The corresponding stable *P*, *Q* outputs will be



(a) $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$ or $P = 1, Q = 1$

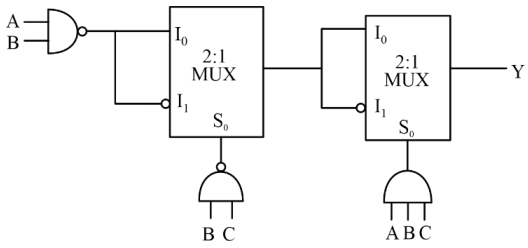
(b) $P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$ $P = 0, Q = 1$

(c) $P = 1, Q = 0; P = 1, Q = 1;\ P = 1, Q = 0$ or $P = 0, Q = 1$

(d) $P = 1, Q = 0; P = 1, Q = 1;\ P = 1, Q = 1$

10. **[MCQ]**

A MUX circuit is designed as shown below:



What is the output Y of above combinational circuit?

(a) AB + BC + CA

(b) B (A + C)

(c) A ⊕ B ⊕ C

(d) Borrow output of full adder

11. **[NAT]**

A 16-bit parallel adder is designed using 16, 1-bit full adders. Each 1-bit full adder is designed using X-OR, AND and OR gates. The delay contributed by X-OR gate is 20ns while that contributed by AND/OR gate is 5ns. The number of additions per second that a 16-bit parallel adder can perform reliably, will be _____ $\times 10^6$

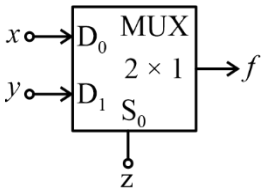
12. **[NAT]**

A designer has sufficient number of units of decoder with enable input of size 4×2^4 and a decoder of size 8×2^8 is to be realized. The number of units of 4×2^4 decoders, required will be

13. [MCQ]

Consider the configuration of a 2 × 1 MUX as shown below.

It is required to implement two variable Boolean function f = P + Q. Then



(a) x = Q, y = 1 and z = P

(b) x = Q, y = 0 and z = P

(c) x = P, y = Q and z = 0

(d) x = P, y = 0 and z = Q

Answer Key

1. (5)
2. (22)
3. (a)
4. (3)
5. (c)
6. (312)
7. (b)
8. (0.80) [Range 0.75 to 0.82]
9. (c)
10. (b)
11. (5.26) (Range 5.1 to 5.3)
12. (17)
13. (a)