Branch : CSE & IT

Hinglish

WEEKLY TEST – 02

Computer Organization and Architecture

Maximum Marks 15

Q.1 to 5 Carry ONE Mark Each

[MCQ]

1. In which address mode, the effective address of the operand is generated by adding a constant value to the content of a register?

(a) Absolute mode
(b) Indirect mode
(c) Immediate mode
(d) Index mode

[MCQ]

2. Consider 4 byte long jump instruction stored in the memory with a starting address of $(200)_{10}$. Address filed of an instruction contain (–24), base register contain 400. Calculate the branch address when the instruction is designed using PC relative addressing mode?

(a) 180 (b) 80
(c) 204 (d) 24

[MSQ]

3. Which of the following address modes is/are the transfer of control addressing modes (AM^S).

(a) Indexed Address modes (AM^S)
(b) Relative /PC-relative AM^S
(c) Based/Based register AM^S
(d) Indirect Addressing modes (AM^S)

[MSQ]

4. Which of the following cannot be a valid instruction for an accumulator based computer system?
X, Y = Addresses, r_1, r_2 = Registers.

(a) Load X
(b) Push Y
(c) Add Y
(d) POP X

[NAT]

5. A 16 bit instruction is present in memory location starting at 250. The instruction is divided into two fields opcode and address of 8 bit each, where address field contains the value 232. What will be the effective address using direct addressing mode.
Consider the memory is byte addressable.

Q.6 to 10 Carry TWO Mark Each

[NAT]

6. Consider 500 MHZ clock frequency processor uses different operand accessing mode below.

Operand Accessing Modes	Frequencies %
Immediate	20
Register	20
Direct	20
Indirect	20
Register Indirect	10

Indexed	10

Also consider 4 cycles consumed for memory references 2 cycles consumed for ALU operation, 0 cycle consumed when the data is present in register and instruction itself. Calculate the average execution time up to one decimal place to fetch the operand?

[MCQ]

7. Which of the following statement(s) is true.

(a) Indexed addressing mode is used for branch instruction.

(b) If current running or branch instruction memory address is 456 and the PC-relative address field is 44.The current running instruction branch to 500 after its execution.

(c) Indirect addressing mode and base register addressing modes permits relocation without any change in code.

(d) For an indirect addressing mode, the address field in the instruction is the address of the effective address of the actual operand.

[NAT]

8. A CPU has 19 registers and uses 10 addressing modes. RAM is 8K × 32 and the instruction is of size 32 bits. What is the maximum size of the op-code field (in bits) if the instruction has a register operand and a memory address operand?

[MSQ]

9. In a computer, a memory unit is of size 256 KW, where W stands for word. Word size is 32 bits and instruction size is one word. Instruction sports 3 types of addressing modes (direct, indirect and registers AM^s)

The instruction has four parts:

Addressing mode, operation code, register code, and address part. An addressing mode part is used to specify one of the 64 registers.

Which of following given statements is/are true?

(a) Addressing mode part takes 2 bits.

(b) Register code takes 6 bits.

(c) Address part takes 18 bits.

(d) opcode part takes 6 bits.

[NAT]

10. Only instructions with zero, one and two addresses are supported by some CPUs, The size of an op-code field is of 8 bits, the instruction size is of 16 bits whereas the size of an address is 4 bits what is the maximum number of two address instructions?

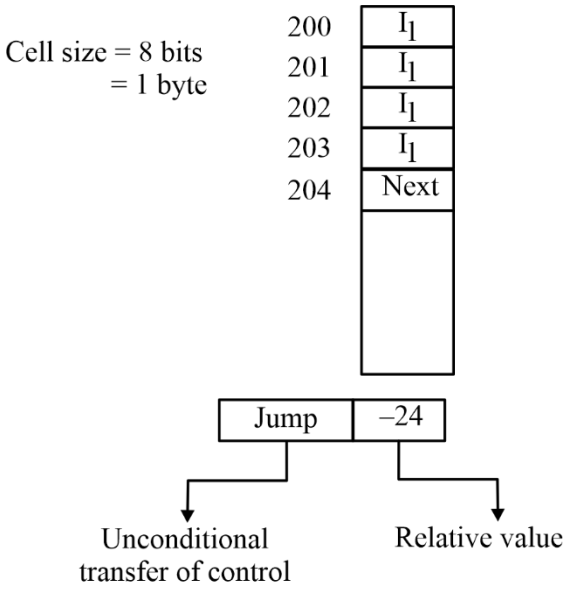
Answer Key

1. **(d)**
2. **(a)**
3. **(b,c)**
4. **(b, d)**
5. **(232)**
6. **(6.8 to 6.8)**
7. **(d)**
8. **(10 to 10)**
9. **(a, b, c, d)**
10. **(256 to 256)**

Hints and Solutions

1. (d)
In Index addressing mode, the content of a given Index register gets added to an instructions address part so as to obtain effective address.

2. (a)
By default memory is byte addressable.



PC- relative Addressing mode

Effective address = PC + relative value
= 204 – 24
= 180

PC : ~~204~~ 180

3. (b,c)
Addressing modes

(i) Sequential control flow AM^S
(ii) Transfer of control flow AM^S

Sequential control flow AM^S

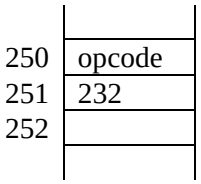
(i) Implied AM^S
(ii) Immediate AM^S
(iii) Direct AM^S
(iv) Indirect AM^S
(v) Indexed AM^S
(vi) Auto Indexed AM^S

Transfer of control flow AM^S

(i) Relative/PC-relative AM^S
(ii) Based /Based register AM^S

4. (b, d)
In single accumulator CPU organization, the first ALU operand is always stored into the accumulator and the second operand is present either in registers or in the memory.
Hence, Push B and POP are not a valid accumulator based instructions.

5. (232 to 232)
In direct addressing mode, the value at the address field is considered as the actual address of data.



Effective address = 232

6. (Range 6.8 to 6.8)

$$\text{Cycle time} = \frac{1}{\text{Frequency}}$$

$$= \frac{1}{500\ \text{MHZ}} = .002\times 10^{-6}$$

= 2 nsec.

Immediate → 0 cycle

Register → 0 cycle

Direct → 1 memory Reference (MR) → 4 cycles

Indirect → 2 MR → 4 ×2 → 8 cycles

Register Indirect → 1MR→ 4 cycles

Indexed → IMR + IALU = 4+2 = cycles

Average execution time = [0.2 × 0 + 0.2×0+0.2×4 + 0.2 ×8 + 0.1 × 4 + 0.1 ×6] × 2nsec.

= [0.8 + 1.6 + 0.4 + 0.6] ×2nsec.

= 3.4 × 2 nsec.

= 6.8 n sec.

7. (d)

For example.

Add A, @500 ⇒ A ← A + m [m[500]]

500	625
	⋮
625	400

Since 500 gives effective address (EA) of 400,

Hence, option (d) is true.

8. (10 to 10)

Number of registers = 19

Number of bits for register field = $\lceil \log_2 19 \rceil$

= 5

Addressing modes = 10

Number of bits for a addressing mode = $\lceil \log_2 10 \rceil$

= 4

RAM size = 8k × 32

= $2^{13} \times 2^5$

Address lines required = 13

Instruction size = 32 bits

Addressing Mode	Opcode Field	Registers	Memory address field
← 4 bits →	← x bits →	← 5 bits →	← 13 bits →

4 + x + 5 + 13 = 32

x = 32 – 22

= 10

9. (a, b, c, d)

Memory unit = 256 KW

= 2^{18} W

1 word = 32 bits = 4B

Addressing mode = 2 bits for direct, indirect and registers.

Register code = $\lceil \log_2 64 \rceil$ = 6 bits

Address lines in memory = 18 bits

Operation mode (op-code) = 32 – (1 + 6 + 18)

= 32 – 25

Opcode = 7 bits

10. (256 to 256)

The given data,

The CPU supports instruction size = 16 bits

Op-code field = 8 bits

Address size = 4 bits

← 16 bits →		
Op-code	Add_2	Add_1

We have two operands

so it requires the 2 × 4 bits = 8 bits

And remaining 16 – 8 bits can be used for two address instructions

Maximum number of two address instructions

= 2^8 = 256