Branch : CSE & IT Batch : Hinglish

WEEKLY TEST – 01

Subject : Computer Organization and Architecture

Topic : Introduction to COA

Maximum Marks 15

Q.1 to 5 Carry ONE Mark Each

[MCQ]

1. A microprocessor has a data bus with 64 lines and an address bus with 32 lines. The maximum number of bits that can be stored in memory is_____.

(a) 32×2^{12} (b) 32×2^{64}

(c) 64×2^{32} (d) 64×2^{64}

[MCQ]

2. Various storage device used by an operating system can be arranged as follows in increasing order of accessing speed.

(a) Secondary memory → main memory → cache memory → Register

(b) Main memory →Secondary memory→cache memory→Register

(c) Secondary memory →cache memory → main memory →Register

(d) Main memory → secondary memory→ Register → cache memory

[MCQ]

3. In the Big-Endian system, the computer stores.

(a) MSB of data in the lowest memory address of data unit.

(b) LSB of data in the lowest memory address of data unit.

(c) MSB of data in highest memory address of data unit.

(d) LSB of data in the highest memory address of data unit.

[MCQ]

4. Consider 32 bits stack CPU supports 1W opcode and 4GB RAM.

Following statement is executed in the system:

X = (A*B) (C+D)

How many machine instructions required for the given statement.

(a) 6 (b) 7

(c) 8 (d) None

[NAT]

5. Consider 32 bits hypothetical CPU which supports 1-word long instruction with 7 bits opcode, register operand field value 5 bits and a memory operand field. Then calculate the total memory size in MB.

Q.6 to 10 Carry TWO Mark Each

[NAT]

6. Consider a hypothetical CPU which supports instruction with 2 register operands and 1 memory operands. CPU supports 120 instructions, 24 register and 512 KB memory space. How many bits are required to encode the instructions.

[NAT]

7. Consider 32 bits CPU which supports 1 words instruction with 3 Register operands and immediate operands fields. Processer supports 7 bits opcode and 24 Register with register size of 32 bits. Instruction is placed in a 256KW memory. What is the largest unsigned constant possible in the instruction?

[NAT]

8. Consider 20 bits hypothetical CPU which supports 1 word instruction placed in a 8KW memory space. If there exits 126 one address instruction and a^b zero address instruction then calculate the value of a + b.

[MCQ]

9. Consider a hypothetical CPU which supports 84 instructions. Instruction format contain two registers operand, one memory operand and 13 bits immediate constant field. CPU supports 34 registers 256KB memory space. A process contains 100 instructions. How much storage space is required in bytes to store the process.

(a) 625 bytes (b) 700 bytes
(c) 600 bytes (d) 725 bytes

[NAT]

10. Consider 64 bits hypothetical CPU which supports one word instruction program is stored in the memory with a starting address of 1000 in decimal. Consider a processes P and 4 instructions. What will be the program counter (PC) value of during the execution of 3^{rd} instruction?

Answer Key

1. **(c)**
2. **(a)**
3. **(a,d)**
4. **(c)**
5. **(4 to 4)**
6. **(36 to 36)**
7. **(1023 to 1023)**
8. **(16 to 16)**
9. **(b)**
10. **(1024 to 1024)**

Hints and Solutions

1. (c)

Data lines = 64 bits

Address lines = 32 bits

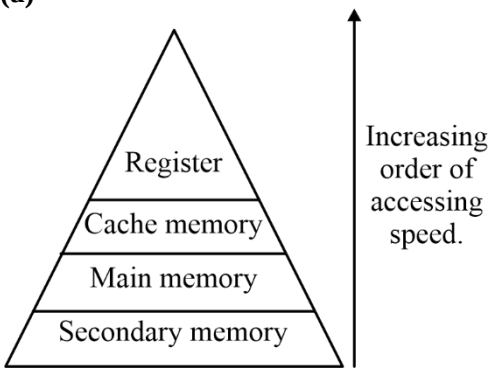
Number of memory location = 2^{32}

Block size = 64 bits.

Maximum number of bits stored in memory

= $2^{32} \times 64$ bit

2. (a)



3. (a,d)

In Big Endian, lower address contains higher byte and higher address contain lower bytes.

4. (c)

X = (A*B) (C+D)

I_1: PUSH A

I_2: PUSH B

I_3: ADD

I_4: PUSH C

I_5: PUSH D

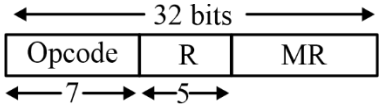
I_6: ADD

I_7: MUL

I_8: POP X

Total number of instructions required in stack CPU is 8.

5. (Range 4 to 4)



MR field = 32 – 12

= 20

Number of cells in memory = 2^{20}

Cell size = 7 + 5 + 20

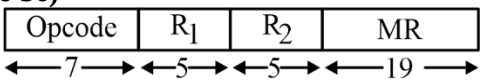
= 4 bytes

Memory size = $2^{20} \times 4$ bytes

= 4 MB

6. (Range 36 to 36)

Instruction format:



Number of registers = 24

Number of bits required to locate register = $\lceil \log_2 24 \rceil$

= 5

Number of Instruction = 120

Opcode = $\lceil \log_2 120 \rceil = 7$

Memory space = 512 KB

Bits required to address memory cells = $\log_2$ 512 K

= $\log_2 2^{19}$

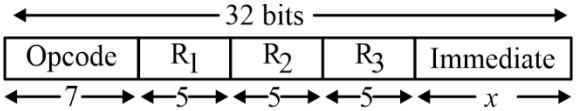
= 19

Instruction size = 7 + 5 + 5 + 19

= 36

7. (Rang 1023 to 1023)

Instruction size = 32 bits



Number of registers = 24

Bits required to represent a register = $\lceil \log_2 24 \rceil = 5$

Opcode = 7 bits

Immediate field value = 32 – (7 + 5 + 5 + 5)

x = 32 – 22

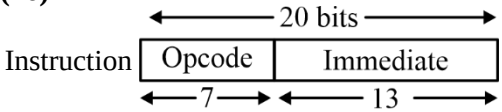
x = 10

The maximum unsigned constant value possible

$= 2^{10} - 1$

$= 1023$

8. (16)



Memory space = 8 KW

Memory address space $= \log_2 8K$

$= \log_2 2^{13}$

$= 13$

Total number of instructions $= 2^7$

$= 128$

Number of one address instruction = 126

Then number of zero address instruction

$= (128 - 126) \times 2^{13}$

$= 2 \times 2^{13}$

$= 2^{14}$

Answer = 2 + 14 = 16

9. (b)

Number of instructions = 84

Opcode = $\lceil \log_2 (84) \rceil = 7$ bits

Number of registers = 34

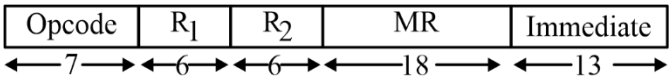
Number of bits required to locate a register = $\log_2 34$

= 6

Memory space = 256 KB

Address space = $\log_2 2^{18}$

= 18 bits



One instruction size = 7 +6 + 6 + 18 + 13

= 50 bits

≅ 7 bytes

Note:- 50 bits ⇒ 6 bytes + 2 bits

By default, memory is byte addressable so 7 cell will be used for one instructions.

Process size =100 instruction

= 100× 7 cells

= 100 × 7 bytes

= 700 bytes

10. (Range 1024 to 1024)

Word size = 64 bits

= 8 bytes

Initial PC value = 1000

I_1 – 1000 – 1007

I_2 – 1008 – 1015

I_3 – 1016 – 1023

I_4 – 1024 – 1031

During the execution of I_3 instruction PC will store the address of next instruction.

$\boxed{PC \rightarrow 1024}$