Branch : CSE & IT Batch : Hinglish

WEEKLY TEST – 04

Computer Organization and Architecture

ALU and Control Unit

Maximum Marks 15

Q.1 to 5 Carry ONE Mark Each

[MCQ]

1. How many 256 × 8 memory modules are required to build 1G × 16 memory system_____?

(a) 2^{24} (b) 2^{23}

(c) 2^{22} (d) 2^{21}

[MCQ]

2. Consider the following statements

S_1: Control unit directs the system and elevates the instruction entered by the user. It coordinates most of the operations in the computer.

S_2: ALU performs arithmetic, comparison and other operations. It executes all tasks to complete all those instructions.

(a) Only S_1 is true.

(b) Only S_2 is true.

(c) Both S_1 and S_2 are true.

(d) Neither S_1 and S_2 is true.

[MCQ]

3. Assume an instruction set architecture of a general propose machine has a total of 126 control signals. Then number of bits required in control word for horizonal and vertical micro-instruction encoding are?

(a) 7 in vertical and 126 in horizontal

(b) 126 in vertical and 7 in horizontal

(c) 128 in vertical and 7 in horizontal

(d) 7 in vertical and 128 in horizontal

[MCQ]

4. Consider the following sequence of micro-instructions.

I_1: MAR← PC

I_2: MBR← memory, PC← PC + 1

I_3: IR← (MBR)

I_4: MAR ←IR[Address field]

I_5: MBR ← (memory)

I_6: R1← R1 + (MBR)

What is the functionality of above instruction?

(a) Adding the number NUM to register R1.

(b) Adding the contents of memory location NUM to register R1

(c) Adding contents of the memory location whose address is at memory location NUM to register R1

(d) None of the above.

[MSQ]

5. Choose the correct statements form the following statements about horizontal and vertical micro programming.

(a) Horizontal micro programing is faster than vertical micro-programming

(b) In vertical programming, Additional hardware is required to generate control signals

(c) Vertical micro programming supports shorter control word and horizontal micro programming supports wider (longer) control word.

(d) Horizontal micro programming allows higher degree of parallelism than vertical micro programming.

Q.6 to 10 Carry TWO Mark Each

[NAT]

6. Consider a system with 6 register and 64 address and two types of 16– bit instruction. Type-1 instruction has three register operands and type-2 instruction has 1 address and 2 register operands. Both instructions exists and the encoding space is completely utilized then what is the total number of instructions can be possible in this system_____.

[MCQ]

7. Consider the following values are in memory and register R_1 is the index register and is stored with 200.

Address	400	500	600	700	800
Data	600	400	100	800	700

Let assume value loaded into the accumulator with instruction "load 500", is P if addressing mode considered to be immediate, if addressing mode considered to be direct addressing then the value of accumulator is q and with indirect addressing r is loaded into accumulator then the value of $x + y + z$ is_____.

(a) 1000 (b) 7000
(c) 1500 (d) 3000

[MCQ]

8. Consider the following code fragment

```
ADD R1, R0, #1          //R1←R0 + 1 and R0 = 0
ADD R2, R0, R0          //R2←R0 + R0
ADD R3, R0, #128        //R3←R0 + 128
Loop: MUL R1, R2, #2    //R1←R1 × 2
ADD R2, R2, #1          //R2←R2 + 1
BNE R2, R3, loop        // if R2 = R3 then exit
```

How many instructions are executed dynamically to complete the above code?

(a) 385 (b) 386
(c) 387 (d) None of the above

[MCQ]

9. Assume a control unit in which the control signals can be divided into the following mutually exclusive types?

Type-1: 23 control signals to activate gates that transfer data from register to the internal bus to the register.

Type-2: 20 control signals to activate gates that transfer data from register to the internal bus to the register.

Type-3: 32 control signals to specify ALU operations.

Type-4: 8 control signals to specify ALU operations.

Then, how many bits of control word can be optimized by using vertical and horizontal micro programming_____.

(a) 60 (b) 61
(c) 64 (d) 65

10. [MCQ]

Assume a micro programmed control unit which supports 260 instructions, each instruction takes 10 micro-operations. 15 flags are supported and 62 control signal vertical micro programmed is used the what is the size of 4 control words? (in bytes)

(a) 8 (b) 9
(c) 10 (d) 11

Answer Key

1. **(b)**
2. **(c)**
3. **(a)**
4. **(b)**
5. **(a, b, c, d)**
6. **(121)**
7. **(c)**
8. **(c)**
9. **(d)**
10. **(d)**

Hints and Solutions

1. (b)

$$\frac{2^{30}\times 16}{256\times 8}=\frac{2^{30}\times 2}{2^{8}}=2^{23}$$

Hence, option (b) is correct.

2. (c)

S_1 (True) : Control unit direct the system and elevates the instruction entered by the user. It coordinates most of the operations in the computer.

S_2 (True) : ALU performs arithmetic, comparison and other operations. It executes all tasks to complete all those instructions.

3. (a)

In horizontal encoding 1 bit is used for each control signal hence it will require 126 control signals and in vertical encoding, 126 control signals can be encoded in $\lceil \log_2 126 \rceil = 7$ bits.

4. (b)

Micro instruction I_1, I_2 and I_3 are used to fetch the instruction Microinstruction I_4, I_5 and I_6 are used to execute the instruction

$$\left.\begin{array}{l} I_1 : MAR \leftarrow (PC) \\ I_2 : MBR \leftarrow (Memory)\, PC \leftarrow (PC)+1 \\ I_3 : IR \leftarrow (MBR) \end{array}\right\} \text{fetch cyle}$$

I_4 : MAR ←IR (address field)

I_5 : MAR ←(memory)//address field of IR updated from the MBR so the reference memory location is read.

I_6 : $R_1 \leftarrow R_1$ +(MRR)// The contents of R and MBR are added by the ALU.

∴ This is executing instruction ADD R1, x.

5. (a, b, c, d)

Type-1: 23 control signals to activate gates that transfer data from register to the internal bus to the register.

Type-2: 20 control signals to activate gates that transfer data from register to the internal bus to the register.

Type-3: 32 control signals to specify ALU operations.

Type-4: 8 control signals to specify ALU operations.

6. (121)

Bits for register = 2^3 = 3 bits

Bits for register = 2^6 = 6 bits

Type 1 → 7 bits	3 bits	3 bits	3 bits
	Opcode	R1	R2	R3
Type 2 → 4 bits	6 bits	3 bits	3 bits
	Opcode	Add	R1	R2

In order to have maximum instruction, we gave 1 instruction to type A so 15 instruction are with type-2 and type- 2 opcode is of only 4 bits and that type-1 is of 7 bits we have 3 extra bits.

So, $15 \times 2^3 + 1 = 121$ instructions

7. (c)

- When immediate addressing is used then the value of p in accumulator is 500.
- If direct addressing is used the value of q in accumulator is m [500] = 400
- If indirect addressing is used the value of r accumulator is @ [500] = 600.

∴ = 500

8. (c)

RO = 0

R1 = 0 + 1 , R1 = 1

R2 = 0 + 0 , R2 = 0

R3 = 0 + 128 = 128

R1 = 1 × 2 = 2

R2 = 0 + 1 = 1

R2 ≠ R3

1 ≠ 128 So, go to loop section and this loop runs 128 times for first time all 6 instructions are executed and after 6th time only 3 instructions are executed.

6 + 3 × 127 = 387

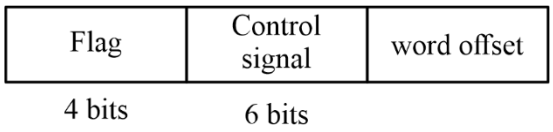
∴ Total number of instructions executed is 387.

9. (d)

Type-1: 23 control signals present So, 5 bits are enough.
Type-2: 20 control signals So, 5 bits are enough
Type-3: 32 control signals So, 5 bits are enough
Type-4: 8 control signals So, 3 bits are enough

Vertical microprograming:
In this we require = 5 + 5 + 5 + 3 = 18 bits
Horizontal microprograming:
23 + 20 + 32 + 8 = 83 bits
∴ By using vertical microprograming over horizontal microprograming 83 – 18 = 65 bits can be saved or optimized.

10. (d)



Number of bits for flag = $\lceil \log_2 15 \rceil$ = 4 bits number of bits for control signal = $\lceil \log_2 62 \rceil$ = 6 bits length of control word = flag + control signal + address.

Also, number of operations for 260 instructions

= 260×10 = 2600

So. Address field = $\lceil \log_2 2600 \rceil$ = 12 bits

∴ Size of 1 control word = 12 + 4 + 6 = 22 bits

for 4 control words = 4× 22 bits = 88 bits

$\Rightarrow \frac{88}{8}$ = 11 bytes.