CONESTOGA
Connect Life and Learning

DIGITAL DESIGN PRINCIPLES

LAB 3 – Parking Indicator

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INTRODUCTION

The project has been created to simulate a real time issue. Consider a parking space indicator fort he customers who are looking for free space for their car. Lets imagine indicators in front of the main entrance, so the customers can see if the parking area is filled or it is still free space. Green indicator shows that there is still free space and red indicator shows there is not enough free space. Simulation has been created in both environment VHDL and Verilog.

VHDL & VERILOG CODE

```
----------------------------------------------------------------------------------
-- PROJECT NAME : LAB3 - Parking Indicator                                      -
-- PROJECT DESCRIPTION : 6 inputs and 2 output, inputs represent the switches -
-- for the spaces inside the parking area. 2 outputs reperesent if there is   -
-- space. Green is on when there is space, red is on when there is no space.  -
----------------------------------------------------------------------------------
-- PROJECT CREATOR : Sinan KARACA                                               -
-- STUDENT ID : 873013                                                          -
----------------------------------------------------------------------------------

--Library Declerations
library IEEE;
use IEEE.std_logic_1164.all;


-- Entity Declerations
entity skaraca_lab3 is
port(sw1 : in std_logic;
     sw2 : in std_logic;
     sw3 : in std_logic;
     sw4 : in std_logic;
     sw5 : in std_logic;
     sw6 : in std_logic;
     LEDR : inout std_logic;
     LEDG : out std_logic);
end skaraca_lab3;

architecture andLogic of skaraca_lab3 is

begin

-- LEDR is showing if all the spaces are occupied
   LEDR <= sw1 AND sw2 AND sw3 AND sw4 AND sw5 AND sw6;

--LEDG is showing if any of the spaces are free
   LEDG <= not LEDR;

end andLogic;
```

- The project is created to implement only second stage of the project.
- In VHDL code, LEDR has been chosen as “inout”, due to use not of LEDG.
- 6 inputs and 2 output, inputs represent the switches for the spaces inside the parking area. 2 outputs reperesent if there is space. Green is on when there is space, red is on when there is no space.

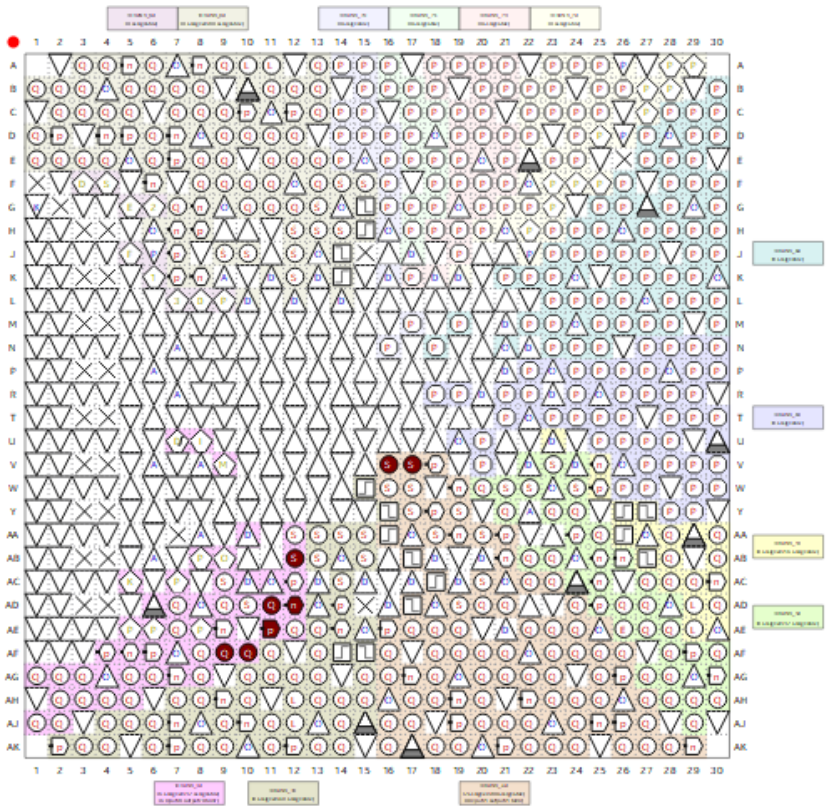
```
module skaracaLab3 (sw1,sw2,sw3,sw4,sw5,sw6,LedG,LedR);
input sw1,sw2,sw3,sw4,sw5,sw6;
output LedG,LedR;

assign LedR = sw1 & sw2 & sw3 & sw4 & sw5 & sw6;
assign LedG = !(LedR);
endmodule
```

- The algorithms of VHDL and Verilog codes are same with each other.

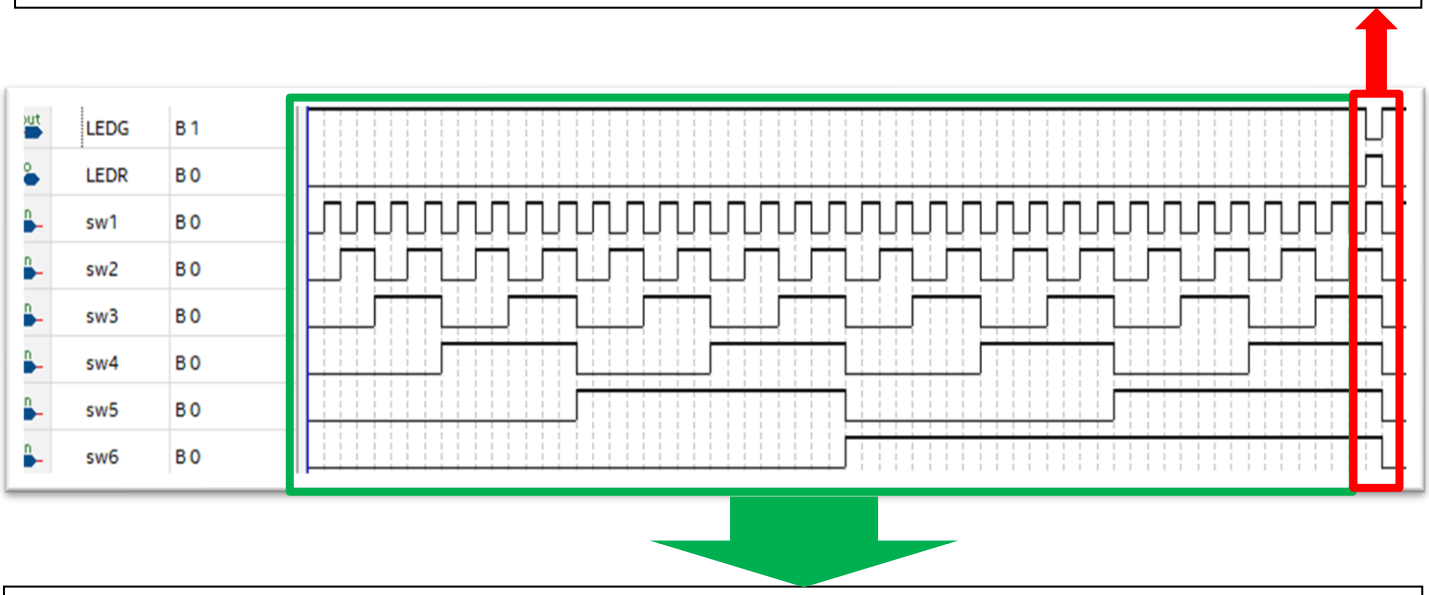
PIN PLANNER

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	er Analog Setting:
out LEDG	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)		
io LEDR	Bidir	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)		
in sw1	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA (default)			
in sw2	Input	PIN_AF9	3A	B3A_N0	PIN_AF9	2.5 V		12mA (default)			
in sw3	Input	PIN_AF10	3A	B3A_N0	PIN_AF10	2.5 V		12mA (default)			
in sw4	Input	PIN_AD11	3A	B3A_N0	PIN_AD11	2.5 V		12mA (default)			
in sw5	Input	PIN_AD12	3A	B3A_N0	PIN_AD12	2.5 V		12mA (default)			
in sw6	Input	PIN_AE11	3A	B3A_N0	PIN_AE11	2.5 V		12mA (default)			
<<new node>>											



SIMULATION WAVE FORM

This is stage that green led is off and red led is on, as it can be seen down below. All of the switches are on, it means all of the spaces are occupied.



If the parking space is occupied, correspounding switch goes high. Even if, one switch is on it means general green led is off, red led is on and vice versa.

CONCLUSION

Input switches simulated on/off with the given time period. For example, sw1 20ns On-20ns Off, sw2 40ns On – 40 ns Off, sw3 80 ns On – 80 ns Off ….. etc. This gives the chance to see all the different combination of input switches to see the behaviour of leds. Because of the lack of FPGA, the code couldnt uploaded to board. However, in this work , all the configuration is done to work with FPGA.