CONESTOGA
Connect Life and Learning

DIGITAL DESIGN PRINCIPLES

LAB 5 – MAGNITUDE COMPARATOR

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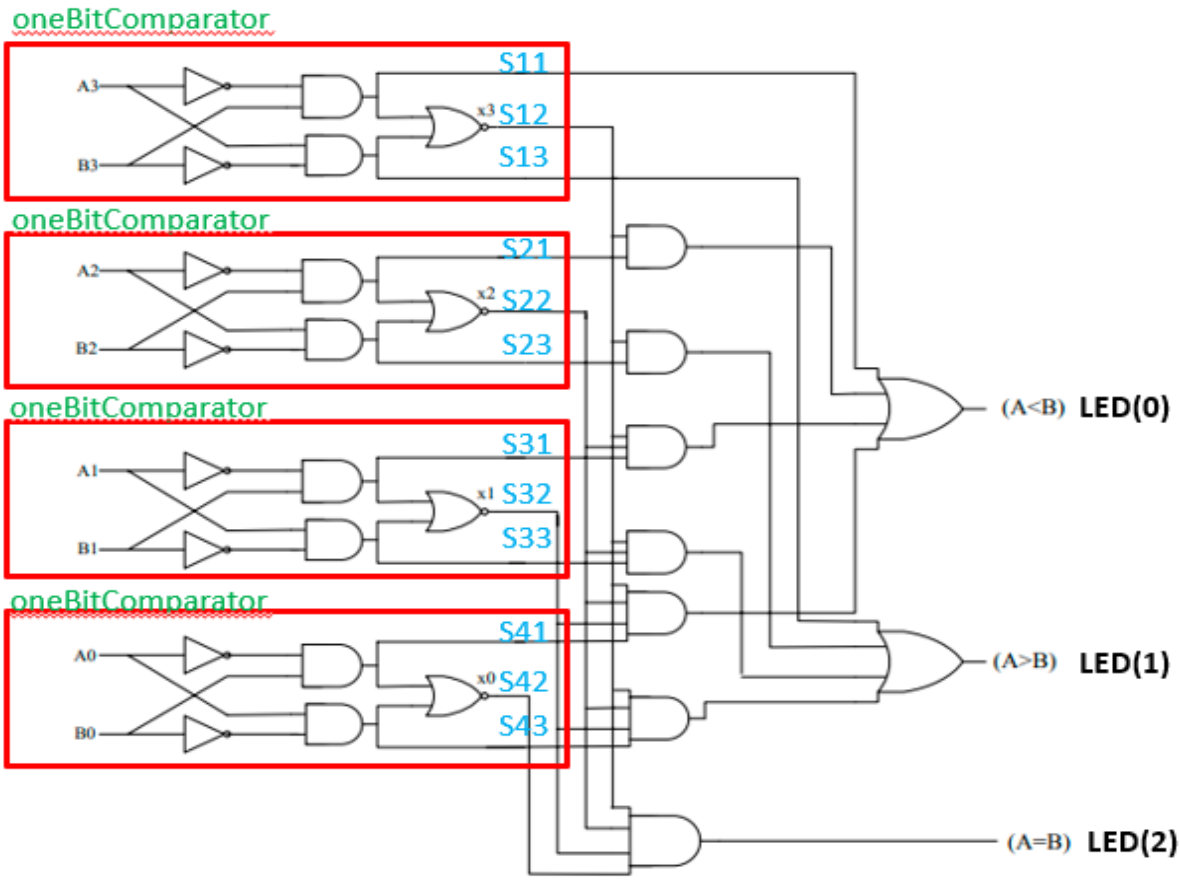
INTRODUCTION

The purpose of the lab experiment is to design 4 bit magnitude comperator with 8 bit input and indicate if they are equal with 3 bit output leds.

WORKING PRINCIPLE



The design consist of 4 oneBitComparator components, the logic circuit above has been designed with truth table of 4 bit magnitude comparator.

VHDL CODE

```
----------------------------------------
----------------------------------------
-- Project Name  : Magnitude Comparator
-- File          : skaraca_lab5
-- Creator       : Sinan KARACA
-- Student number: 8743013
-- Date          : 08.07.2021
----------------------------------------
----------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity skaraca_lab5 is
   port(
      SW : in STD_LOGIC_VECTOR(7 downto 0);
      LED : out STD_LOGIC_VECTOR(2 downto 0));
   end skaraca_lab4;


architecture magnitudeComparator of skaraca_lab5 is


component oneBitComparator is
   port(
      A  : in STD_LOGIC;
      B  : in STD_LOGIC;
      O1 : out STD_LOGIC;
      O2 : out STD_LOGIC;
      O3 : out STD_LOGIC);
   end component oneBitComparator;

signal s11,s12,s13,s21,s22,s23,s31,s32,s33,s41,s42,s43 : STD_LOGIC;


begin

   D1: oneBitComparator port map (SW(7), SW(3), s11, s12, s13);
   D2: oneBitComparator port map (SW(6), SW(2), s21, s22, s23);
   D3: oneBitComparator port map (SW(5), SW(1), s31, s32, s33);
   D4: oneBitComparator port map (SW(4), SW(0), s41, s42, s43);

   -- A < B
   LED(2) <= s11 or (s12 and s21) or (s22 and s12 and s31) or (s12 and s22 and s32 and s41) ;


   -- A > B
   LED(1) <= s13 or (s12 and s23) or (s12 and s22 and s33) or  (s12 and s22 and s32 and s43);

   -- A = B
   LED(0) <= s12 and s22 and s32 and s42;


end magnitudeComparator;
```

VHDL COMPONENT CODE

```
----------------------------------------
----------------------------------------
-- Project Name  : 3to 8 Octal Decoder
-- File          : oneBitComparator
-- Creator       : Sinan KARACA
-- Student number: 8743013
-- Date          : 08.07.2021
----------------------------------------
----------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity oneBitComparator is

      -- 1 bit outputs A , B
      -- o1 ---> A < B
      -- o2 ---> A = B
      -- o3 ---> A > B

   port(
      A   : in STD_LOGIC;
      B   : in STD_LOGIC;
      O1  : out STD_LOGIC;
      O2  : out STD_LOGIC;
      O3  : out STD_LOGIC);

   end oneBitComparator;


architecture Behavioral of oneBitComparator is

   begin
            O2 <= not(((not A) and B) or (A and (not B)));
            O1 <= (not A) and B;
            O3 <= A and not B ;

end Behavioral;
```

VERILOG CODE

```
//////////////////////////////////////////
//////////////////////////////////////////
// Project Name  : Magnitude Comparator
// File          : oneToTwodecoder
// Creator       : Sinan KARACA
// Student number: 8743013
// Date          : 08.07.2021
//////////////////////////////////////////
//////////////////////////////////////////

module skaraca_lab4(SW, LED);
   input  [7:0]SW;
   output [2:0]LED;

   wire s11,s12,s13,s21,s22,s23,s31,s32,s33,s41,s42,s43;

   oneBitComparator(SW[4], SW[0],  s11, s12, s13);
   oneBitComparator(SW[5], SW[1],  s21, s22, s23);
   oneBitComparator(SW[6], SW[2],  s31, s32, s33);
   oneBitComparator(SW[7], SW[3],  s41, s42, s43);

   // A > B
   assign LED[1] = s11 | (s12 & s21) | (s22 & s12 & s31) | (s12 & s22 & s32 & s41) ;

   // A < B
   assign LED[0] = s13 | (s12 & s23) | (s12 & s22 & s33) | (s12 & s22 & s32 & s43);

   // A = B
   assign LED[2] = s12 & s22 & s32 & s42 ;

endmodule
```

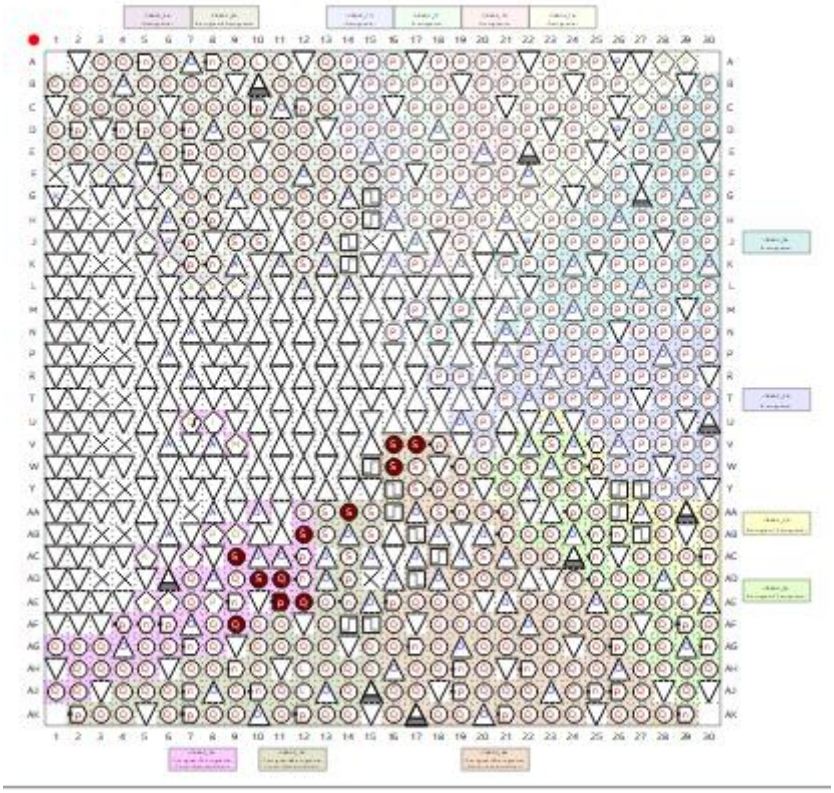
VERILOG COMPONENT CODE

```
//////////////////////////////////////////////////
//////////////////////////////////////////////////
// Project Name  : Magnitude Comparator
// File          : oneBitComparator
// Creator       : Sinan KARACA
// Student number: 8743013
// Date          : 17.06.2021
//////////////////////////////////////////////////
//////////////////////////////////////////////////

module oneBitComparator(A, B, o1, o2, o3);

    // 1 Bit inputs
    input  A, B;

    // 1 bit outputs
    // o1 ---> A < B
    // o2 ---> A = B
    // o3 ---> A > B
    output o1,o2,o3;

    assign o2 = ~((~A & B) | (A & ~B));
    assign o1 = ~A & B;
    assign o3 = A & !B;

endmodule
```

PIN ASSIGNMENT

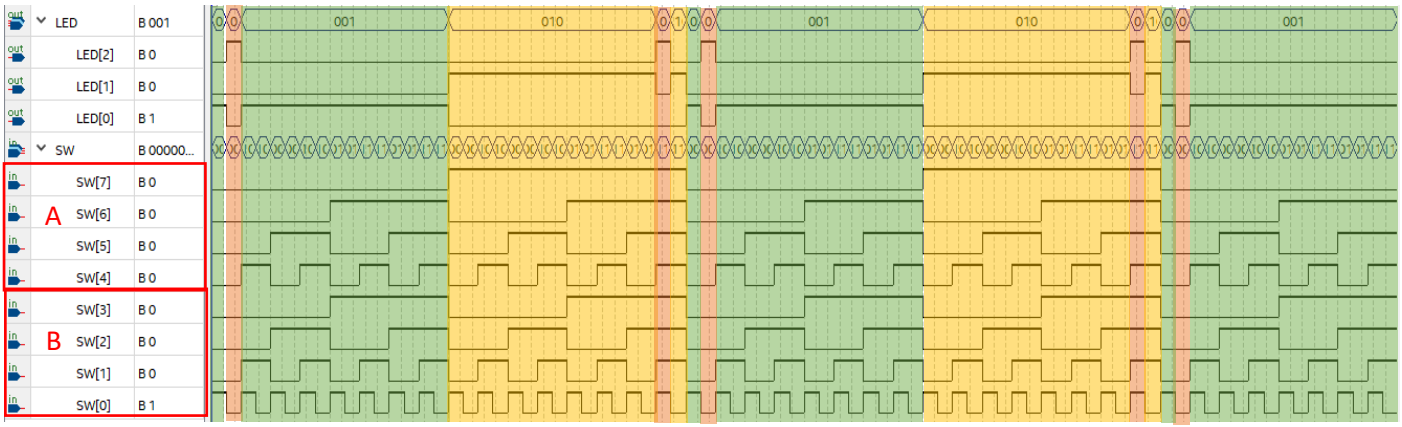
Top View - Wire Bond

Cyclone V - 5CSEMA5F31C6



LED[2]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)
LED[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)
LED[0]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)
SW[7]	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA (default)	
SW[6]	Input	PIN_AF9	3A	B3A_N0	PIN_AF9	2.5 V		12mA (default)	
SW[5]	Input	PIN_AD11	3A	B3A_N0	PIN_AD11	2.5 V		12mA (default)	
SW[4]	Input	PIN_AE11	3A	B3A_N0	PIN_AE11	2.5 V		12mA (default)	
SW[3]	Input	PIN_AC9	3A	B3A_N0	PIN_AC9	2.5 V		12mA (default)	
SW[2]	Input	PIN_AD10	3A	B3A_N0	PIN_AD10	2.5 V		12mA (default)	
SW[1]	Input	PIN_AE12	3A	B3A_N0	PIN_AE12	2.5 V		12mA (default)	
SW[0]	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	2.5 V		12mA (default)	

SIMALATION WAVEFORM



Areas are showing the result as down below,

Orange area , when A = B;

Green area , when A < B;

Yellow area , when A > B;

CONCLUSION

4 bit magnitude comparator has been experienced in this lab session, each bit has been compared with one bit comparator. One bit comparators are defined as component inside VHDL and Verilog codes. Each code consist of 4 components and 1 main code blocks. There are also other ways to design 4 bit comparators, I choose to design my code with components and logic operations to understand k – mapping deeply.