
Makefile

Make

□ Make :

□ Make :

□ make

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.

,

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□ Makefile : make 가 application
make가 .

□ : make [-f makefile] [option] ... target ...

Makefile

- Makefile
 - Make file (target), (dependency), (command)
 - (target) : object . (action)
 - (dependency) : target
 - (command) : make가 action. 가 . (shell)
-) target ...: dependency ...
command
...
- command Tab . Tab
target command .

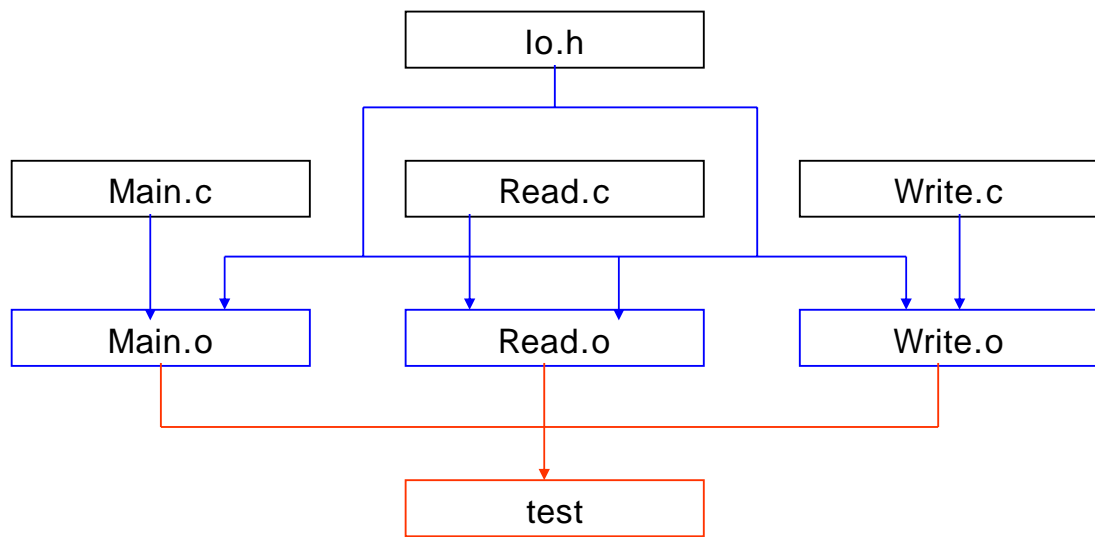
- application
- Mskefile


```
test : main.o read.o write.o
    gcc -o test main.o read.o write.o

main.o : io.h main.c
    gcc -c main.c

read.o : io.h read.c
    gcc -c read.c

write.o: io.h write.c
    gcc -c write.c
```



target

- ☐

dependencies

command

dependencies

target
- ☐

target
가

command

dependencies

target
가
- ☐

makefile

target

dependencies

targets(
- ☐

Default goal

target

makefile

target

Macro



- MacroName = macro - content



- \${MacroName}



Macro



Make macro makefile



Pre-defined macro

- Make -p make (,)

Macro

OBJECTS = main.o read.o write.o

SRCS = main.c read.c write.c <-

CC = gcc <- gcc

CFLAGS = -g -c <- gcc -g 가

TARGET = test <- test

\$(TARGET) : \$(OBJECTS)

\$(CC) -o \$(TARGET) \$(OBJECTS)

lean :

rm -rf \$(OBJECTS) \$(TARGET)

main.o : io.h main.c <- (1) macro CFLAGS setting

read.o : io.h read.c <- make가

write.o: io.h write.c

가

□ 가 make

```

□ pre-defined macro default
make가
make
.
```

```

□ . makefile

```

Macro (1)

```
> ls
sample.c
> make sample
cc sample.c -o sample
> ls
sample sample.c
```

macro

□ makefile (suffix)

- ❑ macro : .SUFFIX
- Makefile
- : .SUFFIX: old_suffix .new_suffix
- : .SUFFIX: .c.o

- macro : 가 macro가 . Macro
- , macro.
- \$* <- 가 (Target)
- \$@ <- (Target)
- \$< <-
- \$? <- (Target) list

macro

main.o : main.c io.h

gcc -c \$*.c

□ \$* 가 \$* main
.

test : \$(OBJS)

gcc -o \$@ \$*.c

□ \$@ . test .

.c.o :

gcc -c \$< (gcc -c \$*.c)

□ \$<
. .o .c
가 main.o main.c main.c \$< .