

1. delay(n), now()

(i) now()

```
unsigned char now(void) { return time; }
```

I use a char time to record the current time.

```
void myTimer0Handler(void){
//.....//
counter = (counter==4) ? 0 : counter+1;
if(!counter) time++;
//.....//
}
```

And update the time when counter count 5 times, where counter count when the timer0 interrupt happen.

In my project, I use a thread for thread manager, so there are at most 3 threads calling delay(n), if all 3 threads end delay at the same time, the worst case is “thread1 occupy the CPU all the 1st timer0 cycle, then context switch such that thread2 occupy the CPU all the 2nd timer0 cycle, finally context switch to thread3”. So all the threads will get correct delay in the sense that delay for “at least n time unit” and “less than (n+0.5) time unit”.

(ii) delay(n)

```
void delay(unsigned char n) {
D[ID] = now() + n;
bitmap[ID] = -2;
ThreadYield();
}
```

When doing delay, I use a char D[4] to record what the time this thread will be recovered and then I set the bitmap[ID] to -2 to indicate that the thread is being delay. After that I call the threadyield() to context switch to other thread.

2. robust thread termination and creation

I do push the address of threadexit() on the stack, so when the thread return, it will enter in the threadexit(), then it will terminate fine.

```
ThreadID ThreadCreate(FunctionPtr fp) {
//.....//
__asm
mov a,DPL
mov b,DPH
mov dptr,#_ThreadExit
```

```

push DPL
push DPH
push a
push b
__endasm;
//.....//
}

```

And I use a semaphore to control the total number of threads.

```

void Bootstrap(void) {
SemaphoreCreate(thread, 4);
__asm
mov _th_tail,#0x7C
__endasm;
}

ThreadID ThreadCreate(FunctionPtr fp) {
SemaphoreWait(thread,th_tail);
//.....//
}

void ThreadExit(void) {
SemaphoreSignal(thread,th_tail);
//.....//
}

```

Because the thread manager is also a thread , when all other threads exits, it will always in the thread manager, so enter in an infinite loop.

3. parking lot example

(i) log

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 00 | 4B | 27 | 00 | 00 | 00 | 00 | 00 | 00 | 25 | 6B | 00 | 00 | 00 | 00 | 00 | 30 |
| 10 | 26 | 5D | 00 | 00 | 00 | 00 | 00 | 03 | 27 | 4C | 00 | 00 | 00 | 00 | FF | 06 |
| 20 | 48 | 58 | 68 | 78 | 01 | 00 | 00 | 00 | 00 | 0A | 00 | 00 | 04 | 00 | 06 | 05 |
| 30 | 01 | 02 | 81 | 83 | 02 | 03 | 03 | 06 | 83 | 85 | 01 | 03 | 6C | 7C | 00 | 10 |
| 40 | 09 | 0B | F6 | 08 | 01 | 80 | 00 | 00 | 01 | 00 | 85 | 01 | 07 | 0A | 00 | 00 |
| 50 | 09 | 0B | 41 | 0A | 25 | 04 | BC | 05 | 09 | 03 | 09 | 00 | 05 | 03 | 00 | 00 |
| 60 | 09 | 0B | 08 | 04 | 26 | 87 | 03 | 00 | 11 | 00 | 00 | 18 | 5C | 00 | 00 | 00 |
| 70 | 09 | 0B | 0E | 08 | 31 | 01 | 00 | 00 | 19 | 00 | 00 | 00 | 00 | 01 | 00 | 00 |

My log is at 0x30~0x39 : 01 02 81 83 02 03 03 06 83 85

This means:

| | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Car 1 | Car 1 | Car 2 | Car 2 | Car 3 | Car 3 | Car 4 | Car 4 | Car 5 | Car 5 |
| in | out | in | out | in | out | in | out | in | out |

[illegible]

```
SemaphoreWait(print,p_tail);  
SemaphoreWait(print,p_tail);  
SemaphoreWait(print,p_tail);  
    //do print log//  
}
```

Result:

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 00 | 4B | 27 | 00 | 00 | 00 | 00 | 00 | 00 | 25 | 6B | 00 | 00 | 00 | 00 | 00 | 30 |
| 10 | 26 | 5D | 00 | 00 | 00 | 00 | 00 | 03 | 27 | 4C | 00 | 00 | 00 | 00 | FF | 06 |
| 20 | 48 | 58 | 68 | 78 | 01 | 00 | 00 | 00 | 00 | 0A | 00 | 00 | 04 | 00 | 06 | 05 |
| 30 | 01 | 02 | 81 | 83 | 02 | 03 | 03 | 06 | 83 | 85 | 01 | 03 | 6C | 7C | 00 | 10 |
| 40 | 09 | 08 | F6 | 08 | 01 | 80 | 00 | 00 | 01 | 00 | 85 | 01 | 07 | 0A | 00 | 00 |
| 50 | 09 | 08 | 41 | 0A | 25 | 04 | BC | 05 | 09 | 03 | 09 | 00 | 05 | 03 | 00 | 00 |
| 60 | 09 | 08 | 08 | 04 | 26 | 87 | 03 | 00 | 11 | 00 | 00 | 18 | 5C | 00 | 00 | 00 |
| 70 | 09 | 08 | 0E | 08 | 31 | 01 | 00 | 00 | 19 | 00 | 00 | 00 | 00 | 01 | 00 | 00 |

pyright ©2005-2016 James Rogers

Remove All Breakpoints

| | |
|-------|--------------|
| 08EBI | MOV A,@R0 |
| 08ECI | JNZ 04H |
| 08EEI | MOV R0,#4BH |
| 08F0I | MOV @R0,#01H |
| 08F2I | SETB 0AFH |
| 08F4I | MOV R0,#4BH |
| 08F6I | MOV A,@R0 |
| 08F7I | JNZ 0FBH |

DI / LD

1 2 3

4 5 6

7 8 9

* 0 #

AND Gate Disabled

Key Bounce Disabled

Standard

U No Parity 8-bit UART @ 4800 Baud

Rx car1 in plot1 at1
car2 in plot2 at1

Tx

Rx Reset

Tx Send

car1 in plot1 at1
car2 in plot2 at1

car1 out plot1 at2
car3 in plot1 at2

car2 out plot2 at3
car3 out plot1 at3

car4 in plot1 at3
car5 in plot2 at3

car5 out plot2 at5
car4 out plot1 at6