Started on	Thursday, 12 January 2023, 3:10 PM
State	Finished
Completed on	Thursday, 12 January 2023, 3:25 PM
Time taken	15 mins 36 secs
Marks	22.00/22.00
Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Complete

Mark 1.00 out of 1.00

The following are types of benchmark applications:

- [x] a. Component benchmarks
- [ ] b. Functional benchmarks
- [x] c. Kernel
- [x] d. Synthetic benchmarks
- [ ] e. Macro-benchmarks

Question **2**

Complete

Mark 2.00 out of 2.00

A disadvantage of the [Carry Select Adder] is that it uses redundant hardware to speed up the addition process.

The [Serial Adder] is the simplest type of adder because it uses a single full adder and a D-latch.

The [Carry Save Adder] is used when more than 2 numbers are to be added because it reduces the carry propagation time.

To get the final result of a [Carry Save Adder] which doesn't propagate the carry of each full adder, a normal type adder must be used to finally add the sum to the carry.

The [Ripple Carry Adder] is implemented by several full adders in series which connect their carry output to the input of the next one.

In order to reduce the time required to form the carry signals, the [Carry Lookahead Adder] uses a separate block which calculates the carry output of each full adder.

The multiplication of binary numbers with the Wallace Tree method is based on combining pairs of partial products with the help of multiple levels of [Carry Save Adder] .

Question **3**

Complete

Mark 1.00 out of 1.00

Fill in the gaps so that the code below will measure the execution time of an "add" instruction:

rdtsc

mov time_high, edx

mov time_low, eax

add var, ecx

rdtsc

sub eax, time_low

sub edx, time_high

mov time_high, edx

mov time_low, eax

Question **4**

Complete

Mark 1.00 out of 1.00

Variables can be declared inside processes and only be used within the process it was declared in.

Signals can only hold the last value assigned to them.

Signals cannot be used to store intermediary results within a process.

Signals have their values assigned only when the process execution suspends.

Variables are assigned using the **:=** assignment symbol.

Signals are assigned using the **<=** assignment symbol.

Variables that are assigned immediately take the value of the assignment.

Question **5**

Complete

Mark 1.00 out of 1.00

The Time-Stamp Counter (TSC):

- [x] a. counts CPU cycles
- [ ] b. counts seconds
- [x] c. is a 64-bit model specific register
- [ ] d. is a 32-bit model specific register
- [x] e. is loaded in EDX:EAX by the RDTSC instruction
- [ ] f. is loaded in DX:AX by the RDTSC instruction

Question **6**

Complete

Mark 1.00 out of 1.00

This MIPS pipeline hazard:

1) **R2** <- R5 + R3
2) R4 <- **R2** + R6

- a. is a WAW (Write After Write) hazard
- b. is a RAW (Read After Write) hazard
- c. Can be prevented by inserting a minimum of 4 **NoOp** instructions between (1) and (2)
- d. Can be prevented by inserting a minimum of 3 **NoOp** instructions between (1) and (2)

Question **7**

Complete

Mark 1.00 out of 1.00

When measuring the performance with the RDTSC instruction the programmer has to be aware of which issues?

- a. Context switches
- b. Out-of-order execution
- c. Time-Stamp Counter Overflow
- d. Frequency changes
- e. Current time zone

Question **8**

Complete

Mark 1.00 out of 1.00

The following are **not** methods of multiplying 2 n-bit numbers:

- a. Vector Multiplier
- b. Higher-Radix Multiplication
- c. Wallace Tree
- d. Shift-and-Add Multiplication
- e. Booth's Technique

Question **9**

Complete

Mark 1.00 out of 1.00

A VHDL process:

- a. executes after the other processes complete their execution
- b. can contain concurrent statements
- c. **must** contain a sensitivity list or a wait statement
- d. cannot contain concurrent statements
- e. executes in parallel with other processes

Question **10**

Complete

Mark 1.00 out of 1.00

Choose the correct answers:

- a. A 2-way set associative cache memory with the capacity of *8 KB* and the set size of *8 B* has a number of *512 sets* per RAM.
- b. A 2-way set associative cache memory with the capacity of *8 KB* and the set size of *8 B* has a number of *1024 sets* per RAM.
- c. A 2-way set associative cache memory with the capacity of *8 KB* and the set size of *8 B* has a number of *2048 sets* per RAM.
- d. A direct-mapped cache memory with the capacity of *8 KB* and the set size of *8 B* has a number of *2048 sets* per RAM.
- e. A direct-mapped cache memory with the capacity of *8 KB* and the set size of *8 B* has a number of *1024 sets* per RAM.
- f. A direct-mapped cache memory with the capacity of *8 KB* and the set size of *8 B* has a number of *512 sets* per RAM.

Question **11**

Complete

Mark 1.00 out of 1.00

The Instruction Fetch (IF) datapath is composed of:

- a. Data Memory
- b. Sign Extend
- c. Instruction Memory
- d. Register Block
- e. Program counter (PC)
- f. Adder

Question **12**

Complete

Mark 1.00 out of 1.00

The following signals are set to active (1) while the MIPS executes an ADD operation ($rd <- $rs + $rt):

- [ ] a. RegRead
- [x] b. RegDst
- [ ] c. MemRead
- [ ] d. MemtoReg
- [x] e. RegWrite

Question **13**

Complete

Mark 1.00 out of 1.00

Which of the following are performance metrics of the CPU?

- [x] a. Performance vs. Power – performance to energy ratio
- [ ] b. Bandwidth (B/s)
- [x] c. IPS – instructions per second (integer arithmetic operations)
- [x] d. FLOPS – floating point operations per second
- [ ] e. Capacity vs. Power – capacity to energy ratio
- [x] f. Clock frequency (Hz)
- [ ] g. Speed (B/s)
- [ ] h. Latency (response time)

Question **14**

Complete

Mark 1.00 out of 1.00

The purpose of the **opcode** in an R-type (Register) instruction is:

- [ ] a. The opcode bits are 0 and can be used to expand the instruction set with additional R-type instructions.
- [ ] b. Specifies the function to be executed
- [x] c. Specifies the type of instruction to be executed
- [ ] d. Specifies the operation to be executed

Question **15**

Complete

Mark 1.00 out of 1.00

R-type (register) instructions are the following:

- [x] a. Or
- [x] b. Add
- [ ] c. Load
- [ ] d. Store
- [ ] e. Jump

Question **16**

Complete

Mark 1.00 out of 1.00

A good benchmark should have some of the following qualities:

Select one or more:

- [x] a. Provides relevant performance measures
- [x] b. Presents unbiased results
- [ ] c. Uses only synthetic pieces of code
- [ ] d. Several runs of the benchmark on the same machine produce exactly the same results

Question **17**

Complete

Mark 2.00 out of 2.00

Choose only the correct answers:

- [x] a. Each step of instruction execution for the pipeline MIPS is performed in a clock cycle.
- [x] b. Each step of instruction execution for the sequential MIPS is performed in a clock cycle.
- [ ] c. In a pipeline MIPS, a new instruction is fetched only after the previous has finished its execution
- [x] d. In a sequential MIPS, a new instruction is fetched only after the previous has finished its execution
- [ ] e. Each step of instruction execution for the sequential MIPS is performed in multiple clock cycles.
- [ ] f. Each step of instruction execution for the pipeline MIPS is performed in multiple clock cycles.

Question **18**

Complete

Mark 1.00 out of 1.00

Arrange the MIPS instruction steps from the first to last executed:

Instruction fetch , Instruction decode , Execution , Memory access , Write back

Question **19**

Complete

Mark 1.00 out of 1.00

Select the correct type of memory:

Dynamic memories need periodic refresh of the stored data.

Static memories keep the information as long as there is a supply voltage present.

Dynamic memories keep the data for a limited time.

For Dynamic memories, the circuit selection is done by the RAS and CAS signals.

Question **20**

Complete

Mark 1.00 out of 1.00

(Choose only true statements) Picoblaze:

Select one or more:

- a. its ALU implements multiplication and division instructions
- b. its ALU implements the following logical instructions: AND, OR, XOR
- c. all its instructions execute in 1 clock cycle
- d. is a fully embedded 8-bit RISC microcontroller

◄ Final project

Jump to...

Colocviu - marti16_1 ►