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1. **TYPES OF DYNAMIC RAMDOM ACCESS MEMORY**

* Asynchronous DRAM is the basic type of DRAM on which all other types are based. Asynchronous DRAMs have connections for power, address inputs and bidirectional data lines.

Although this type of DRAM is asynchronous, the system is run by a memory controller which is clocked, and this limits the speed of the system to multiples of the clock rate.

TYPES OF ASDRAM

* RAS only Refresh, ROR: This is a classic asynchronous DRAM type and it is refreshed by opening each row in turn. The refresh cycles are spread across the overall refresh interval. An external counter is required to refresh the row sequentially.
* CAS before RAS refresh CBR: To reduce the level of external circuitry, the counter required for the refresh was incorporated into the main chip. This became the standard format for refresh of an asynchronous DRAM.
* **FAST PAGE MODE (FPM) DRAM**: FPM DRAM was designed to be faster than the conventional types of DRAM. As such, it was the main type of DRAM used in PC’s; although it Is now well out of date as it was only able to support memory bus speeds up to about 66MHz.
* **EXTENDED DATA OUT DRAM**: EDO DRAM was a form of DRAM that provided a performance increase over FPM DRAM. Yet , this type of DRAM was still only able to operate at speeds of up to about 66MHz. EDO DRAM is sometimes referred to as Hyper Page Mode enabled DRAM because it is a development of FPM types of DRAM to which it bears similarities.
* **BURST EXTENDED DATA OUT DRAM**: The Burst EDO DRAM was a type of DRAM that gave improved performance of the straight EDO DRAM. The advantages of the BEDO DRAM type is that it could process four memory addresses in one burst saving three clock when compared to EDO memory.
* **SYNCHRONOUS DRAM**: Synchronous DRAM is a type of DRAM that is much faster than previous, conventional forms of RAM and DRAM. It operated in a synchronous mode, synchronizing with the CPU.
* **RAMBUS DRAM**: This type of DRAM that was developed by Rambus Inc, obviously taking its name from the company. It was a competitor to SDRAM and DPR SDRAM and was able to operate at much faster speeds than precious versions of DRAM.

1. **DIFFERENCES BETWEEN SRAM AND DRAM**

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|  | **SRAM** | **DRAM** |
| 1 | *Stored bits in memory cells composed of flip flops* | *Memory cells are composed of capacitors and transistors* |
| 2 | *SRAM makes use of an array of 6 transistors* | *Makes use of single transistor and capacitor for each memory cell* |
| 3 | *Low density/less memory per chip due to more circuitry required for a single cell* | *High chip density/more memory per chip compared to SRAM due to less circuitry for a single cell* |
| 4 | *More power consumption than DRAM because of low chip density* | *Less Power consumption than SRAM because of simple circuitry* |
| 5 | *Each cell which can store a single bit requires six transistors* | *Each cell requires a capacitor which stores bit as charge and a transistor.* |

1. **DIFFERECES BETWEEN NORTH BRIDGE AND SOUTH BRIDGE**

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|  | **NORTHBRDGE** | **SOUTHBRIDGE** |
| 1 | *The portion of the chipset hub that connects faster I/O buses (for example AGP bus) to the system bus* | *The portion that connects to slower I/O buses (e.g an ISA bus) to the system bus* |
| 2 | *The fast end of the hub containing the graphics and memory controller* | *The slower end of the hub containing the I/O controller hub* |
| 3 | *Its chipset interconnects and controls* | *It takes control of storage (hard disk) and USB* |
| 4 | *It is directly connected to the CPU* | *It is not directly connected to the CPU* |