# Page 2

SODIMM connector interface, Expansion connectors, Current monitors

# Page 3

JTAG interface, Memory card interface, USB interface, reset key&LED, Optional connections

# Page 4

I2C: LEDs and joystick, Boot mode control, Accelerometer and analog input

## Page 5

UART: USB-to-serial interface, RS232 interface, and XBee interface

### Page 6

QVGA display module interface

# Page 7

UDA1380 codec interface

# Page 8

100/10Mbps Ethernet interface

UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic. However, always check jumper positions on actual boards since there is no guarantee that all jumpers are in default place.

### **Rev 2.2**

Changed U11 to XNOR-gate to fix NAND boot problem. SD-card detect always powered (affect R11). D2-VCC terminated to +3V3 instead of VBUS.

#### **Rev 2.1**

No schematic changes, only layout update.

#### **Rev 2.0**

Added R114, R115 and C81.

Changed J14 to 2x7 pin list. Added OTP control jumper. Added 100/10Mbps Ethernet interface (all of page 8).

#### **Rev 1.1**

Change RS232 DSUB9 to Male pinout. Corrected USB TX/RX LED mixup on page 5. Added R102/R103/R104/R105.

#### **Rev 1.0**

Original revision



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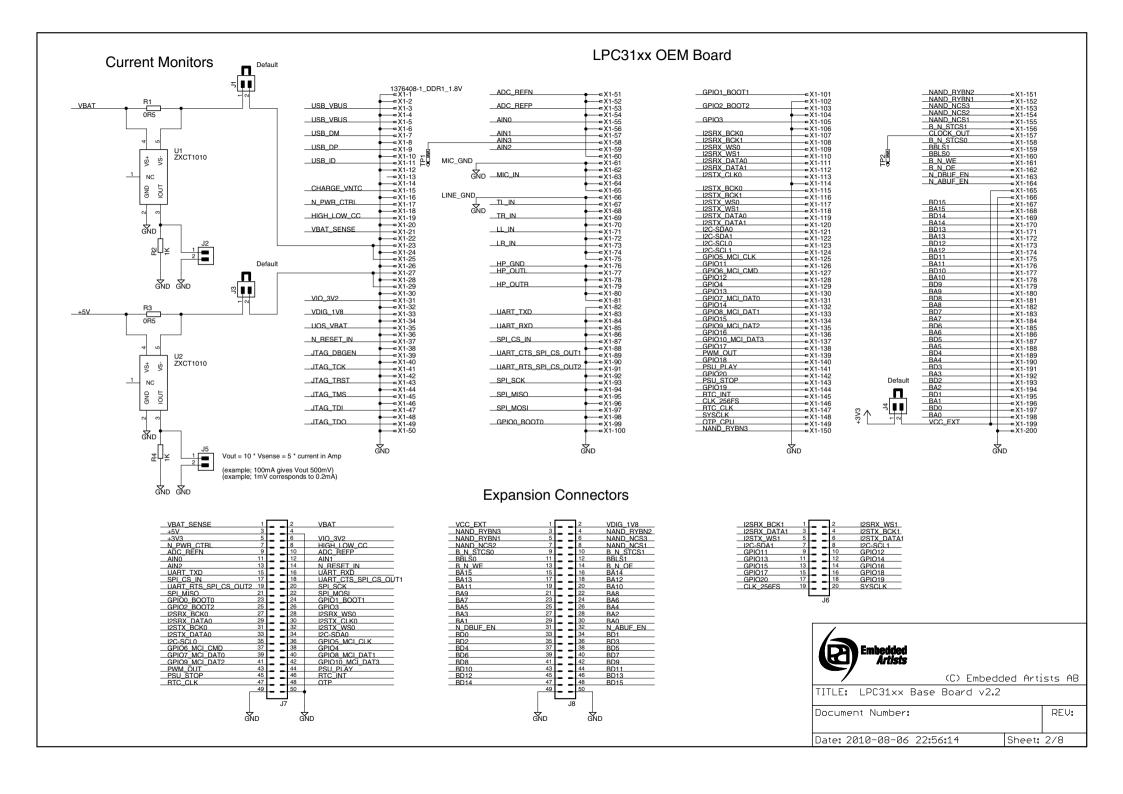
TITLE: LPC31xx Base Board v2.2

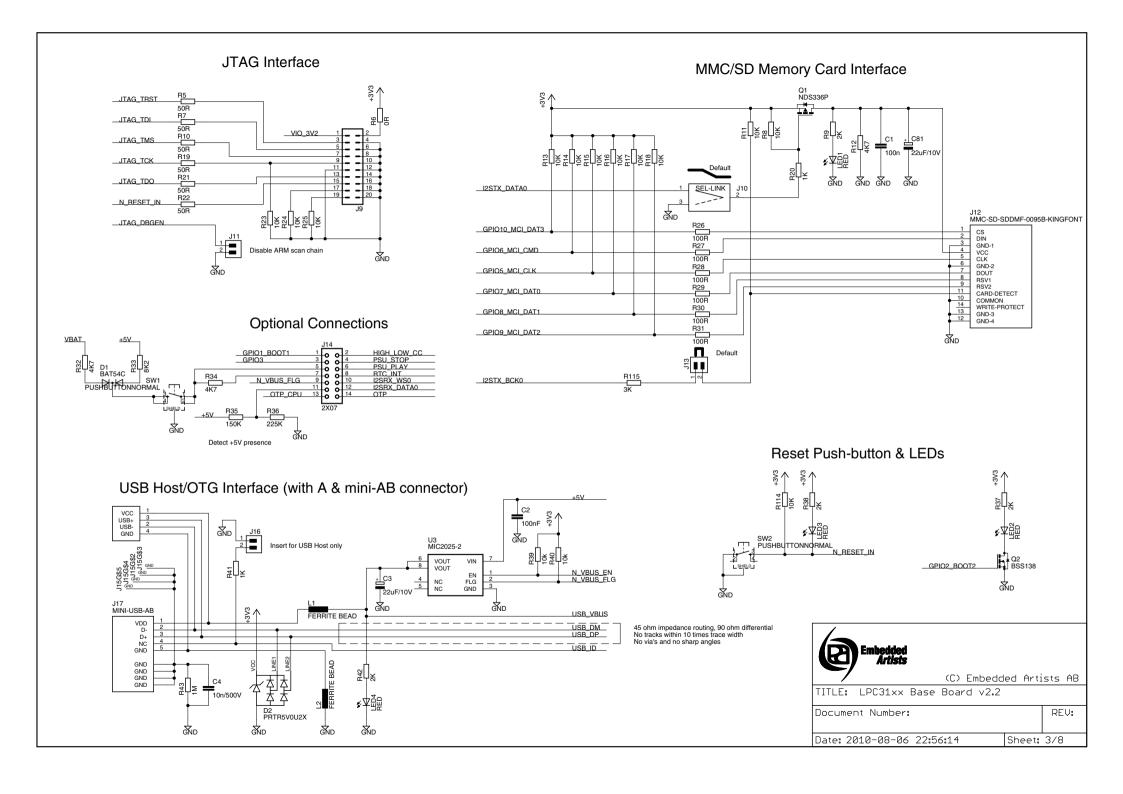
Document Number:

REV:

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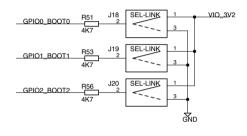




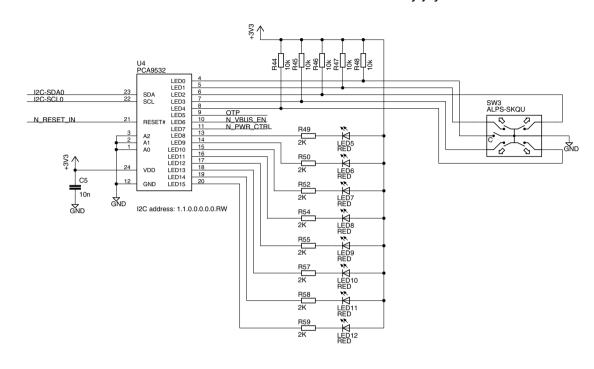
#### Boot mode

GPI00	GPIO1	GPIO2	Boot source
LOW	LOW	LOW	NAND boot
LOW	LOW	HIGH	SPI boot
LOW	HIGH	LOW	USB via DFU class
LOW	HIGH	HIGH	MMC/SD card
HIGH	LOW	HIGH	Functional test mode
HIGH	HIGH	LOW	UART 115.2kbps 8N1
HIGH	HIGH	HIGH	Test mode

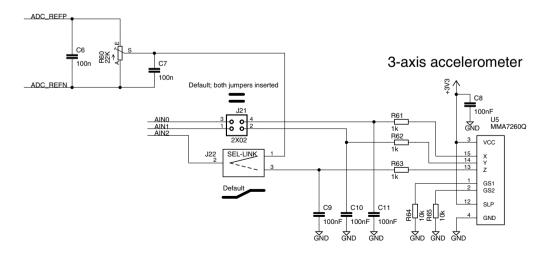
#### Default; no jumpers inserted Default set on cpu/OEM board

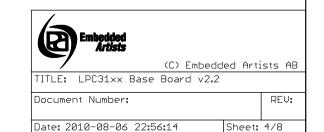


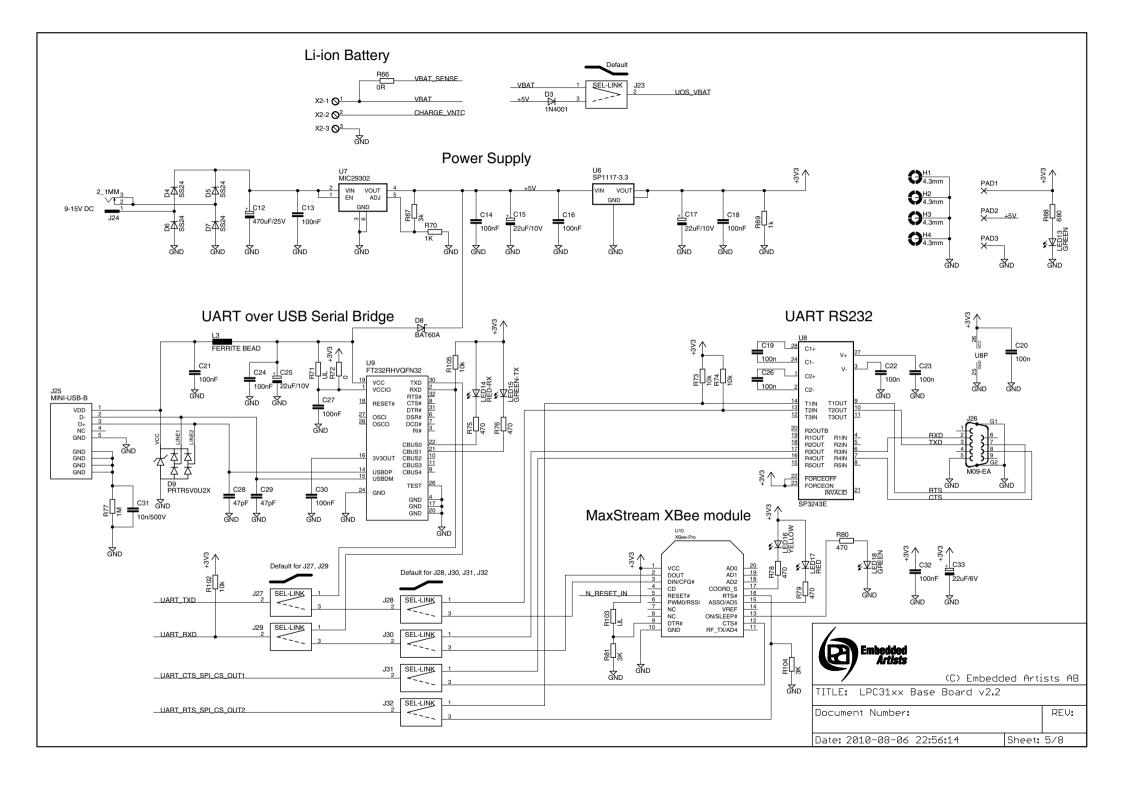
# LEDs and 5-key joystick switch



# **Analog Input**



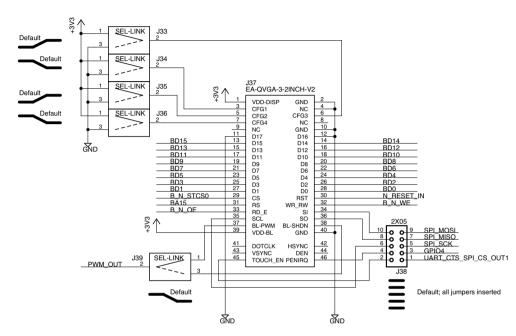




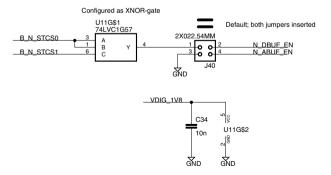
#### Connector for color QVGA LCD

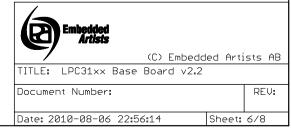
# Interface Setting

	CFG1	CFG2	CFG3	CFG4	Interface mode	
	HIGH	LOW	LOW	HIGH	16-bit parallel	D
	LOW	LOW	HIGH	LOW	9-bit parallel	
Ī	LOW	LOW	LOW	HIGH	8-bit parallel	=



## **Enable Buffers**





#### Stereo Audio Codec <sup>2</sup>∏¥ Microphone input C35 10uF/16V Interface to I2S1 C36 10uF/16V GND I2C address: 0.0.1.1.0.1.0.RW Default; all jumpers inserted Line input 1 C37 10uF/16V U12 UDA1380HN SEL-LINK 15 12 13 14 SEL\_L3\_IIC L3MODE/A1 L3CLOCK/SCL VINM C38 10uF/16V \_\_I2C-SCL1 \_\_I2C-SDA1 SEL-LINK VINL L3DATA/SDA \_LR\_IN 2X06 C39 10uF/16V GND \_\_I2SRX\_BCK1 \_I2SRX\_WS1 BCKO WSO DATAO BCKI WSI DATAI VOUTL VOUTR C40 C41 220pF 220pF I2SRX\_DATA1 I2STX\_BCK1 VOUTL\_HP VOUTR\_HP VREF\_HP GND GND Line input 2 / Line output R89 OR R91 UL VREF SYSCLK 100R CLK 256FS SEL-LINK C42 C43 10uF/16V \_TL\_IN 100nF SYSCLK R90 100R RESET GND GND 11 RTCB VDDA(HP) TR IN C44 C45 ₫ND ₫ND 100nF C46 C47 220pF 220pF C51 GND 10uF/16V 80 ¥ ¥0 ¥ GND GND VDDA(ADC) VSSA(ADC) GND GND GND GND C48 C50 C49 10uF/16V 100nF 100nF GND GND GND SEL-LINK 22 24 VDDA(DAC) VSSA(DAC) HP OUTL C53 C52 Headphone output GND 10uF/16V 100nF SEL-LINK GND \_HP\_OUTR R101 VADCP VADCN 100R EXP EXP Default C55 C54 GND άνρ 100nF 10uF/16V SEL-LINK GND \_HP GND BLM18AG221SN1D C56 (C) Embedded Artists AB 10uF/16V TITLE: LPC31xx Base Board v2.2 Document Number: REV: Date: 2010-08-06 22:56:14 Sheet: 7/8

# 10/100Mbps Ethernet

