Sireesh N

D.no. 7/147, Prakash road, Anantapur, India, PIN: 515001• sireesh1992@gmail.com •+917845105950

EDUCATION

Program	Institution	%/CGPA	Year
BTech + MTech in Electrical Engineering	IIT Madras, Chennai	**8.02**	2015
XII	PRK Junior College, Anantapur	**92.9**	2009
X	CVR Memorial High School, Anantapur	**88.9**	2007

SCHOLASTIC ACHIEVEMENTS

- Secured GPA of **9.57/10** in the final year of graduation.

RELEVANT COURSEWORK

Core	Computer Architecture, CAD for VLSI Systems, DSP Architectures and embedded systems, Digital system testing and testable design, Microprocessor Lab
Programming	Data Structures and Algorithms, Machine Learning (Coursera), Computational Engineering
Minor (Physics)	Classical Physics, Quantum Physics, Quantum computation and quantum information
Math	Calculus I, II, Linear algebra and numerical analysis, differential equations, Probability foundations, Graph Theory

SKILLS

Programming Languages	C, **C++**, **Java**, Python, R
Web technologies	HTML5, CSS, JavaScript, AngularJS

EMPLOYMENT

- **Software developer at Citi** **(Jul'15 –Present)**
  - Involved in development of electronic trading tools for FX trading.

    Major projects
    - *Real time credit checking system:* Trade validating system which broadly does regulatory and credit related checks. Contributed in building and optimizing socket API which decreased the checking latency by around 10 times.
    - *Counterparty risk management*: Risk management system which calculates and maintains clients exposure and facilitates reporting.
    - *Automated test framework*: Working on building an automated test framework to validate the above systems which saves enormous testing time.
    - *Trade rating system*: Currently a key member of the team which develops and maintains the FX trade rating system at Citi.

PROJECTS

- **Senior thesis: Design and implementation of Industrial class Processor** **(Jun '14 – May '15)**
  - Designed and implemented parameterized multiple issue multithreaded out of order processor.
  - Achieved a clock of 1.2 GHz for fetch with of 2 and instruction window of size 32 on 65 nm UMC library.
  - *Technologies used:* Bluespec Systemverilog
- **Common Path Pessimism Removal during static timing analysis** **(Dec '13 – Feb '14)**
  - Designed a **parallel algorithm** for removal of inherent pessimism involved in early-late split-timing analysis.
  - Placed 2nd in TAU 2014, an international timing contest sponsored by **ACM** and proved to be **at least 200 % faster** than all other submissions with **90%** accuracy when benchmarked with circuits >1 million gates.

- *Technologies used:* C, Posix Threads

- **Quantum circuit decomposition** **(Oct '13 – Nov '13)**
  - Designed and implemented an algorithm for decomposing multi qubit unitary gates into single qubit unitary and CNOT gates.
  - *Technologies used:* Python, TeX
- **Circuit simulation software in C** **(Aug '11 – Apr '11)**
  - Developed a program to simulate the steady state behavior of circuit with linear elements.
  - Calculated voltages and currents at different nodes by creating a nodal analysis matrix and solving it.

INTERNSHIPS

- **Internship at Reverseinformatics, IITM Research Park** **(May '13 – Jul '13)**
  - **Low cost Computer Cluster:** Built a Beowulf cluster, a low cost commodity grade computer cluster with 25 compute nodes.
  - **Time Series Analysis:** Developed a multicore R program that runs on Beowulf cluster to test different time series analysis techniques on given data.
  - *Technologies used:* R programming language, C, Shell scripting
- **Internship at Electronics Corporation of India Ltd** **(May '12 – Jun '12)**
  - **PCI based MIL core:** Designed and implemented a PCI based MIL core to interface PCI based remote terminals to MIL (military standard) bus.
  - Developed a glue logic which maps the data and interrupts from one core to the other appropriately.

CO-CURRICULAR AND EXTRA-CURRICULAR ACTIVITIES

- Teaching Assistant for an undergraduate course 'Digital Systems' with 160 students.
- Teaching Assistant for graduate level lab course 'VLSI design Lab'.
- Finalist of 'digital circuits design' event at shaastra 2011.
- Member of organizing team of 'Watts Up', an electrical engineering department event in shaastra 2012.