UE22CS251B : Microprocessor and Computer Architecture

Paracache Simulator- 2 way set associative and cache type analysis

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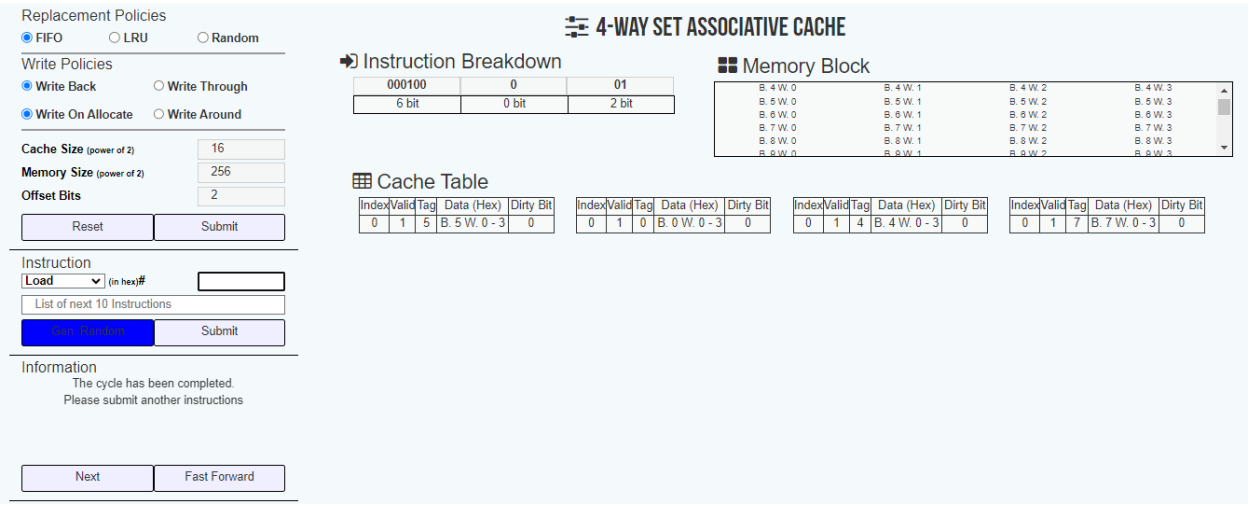
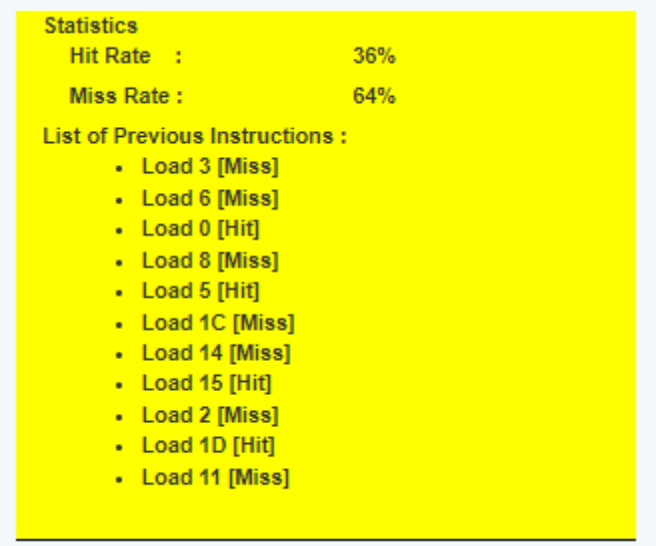
Semester 4 Section J

1. Consider 4 way set associative mapping with following design : cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:
   3,6,0,8,5,1c,14,15,2,1D,11





2. **Cache type analysis:** Memory size: 64, Offset:0, Cache size:8
   Input=L-0,L-3,L-4,L-1,L-2,L-5,L-7,S-6,L-0,L-3,L-1,L-11,L-5,L-15,L-9,S-4,L-0,L-4,S-3,L-12

Cache Comparison

1. Direct Mapped Cache[8]

HIT 40% MISS 60% || ADD. RESOURCES 184 NAND

Instruction Breakdown

010	010	0
3 bit	3 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	BLOCK 0 WORD 0 - 0	0
1	1	001	BLOCK 9 WORD 0 - 0	0
2	1	010	BLOCK 12 WORD 0 - 0	0
3	1	0	BLOCK 3 WORD 0 - 0	1
4	1	0	BLOCK 4 WORD 0 - 0	1
5	1	010	BLOCK 15 WORD 0 - 0	0
6	1	0	BLOCK 6 WORD 0 - 0	0
7	1	0	BLOCK 7 WORD 0 - 0	0

2. Fully Associative Cache[8]

HIT 25% MISS 75% || ADD. RESOURCES 1808 NAND

Instruction Breakdown

010010	0
6 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	17	BLOCK 11 WORD 0 - 0	0
1	1	21	BLOCK 15 WORD 0 - 0	0
2	1	9	BLOCK 9 WORD 0 - 0	0
3	1	4	BLOCK 4 WORD 0 - 0	0
4	1	0	BLOCK 0 WORD 0 - 0	0
5	1	3	BLOCK 3 WORD 0 - 0	0
6	1	18	BLOCK 12 WORD 0 - 0	0
7	1	6	BLOCK 6 WORD 0 - 0	0

3. 2-Way Set Associative Cache[4]

HIT 40% MISS 60% || ADD. RESOURCES 336 NAND

Instruction Breakdown

0100	10	0
4 bit	2 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 0	0
1	1	2	B. 9 W. 0 - 0	0
2	1	4	B. 12 W. 0 - 0	0
3	1	0	B. 3 W. 0 - 0	1

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 4 W. 0 - 0	1
1	1	5	B. 15 W. 0 - 0	0
2	1	1	B. 6 W. 0 - 0	0
3	1	1	B. 7 W. 0 - 0	0

4. 4-Way Set Associative Cache[2]

HIT 35% MISS 65% || ADD. RESOURCES 520 NAND

Instruction Breakdown

01001	0	0
5 bit	1 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	9	B. 12 W. 0 - 0	0
1	1	8	B. 11 W. 0 - 0	0

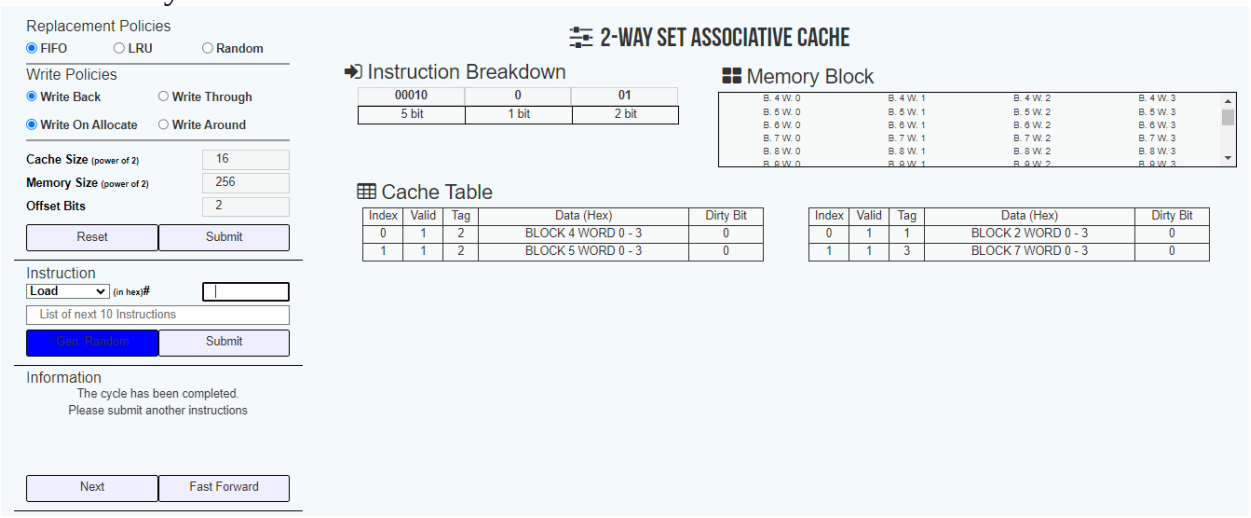
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B. 4 W. 0 - 0	1
1	1	10	B. 15 W. 0 - 0	0

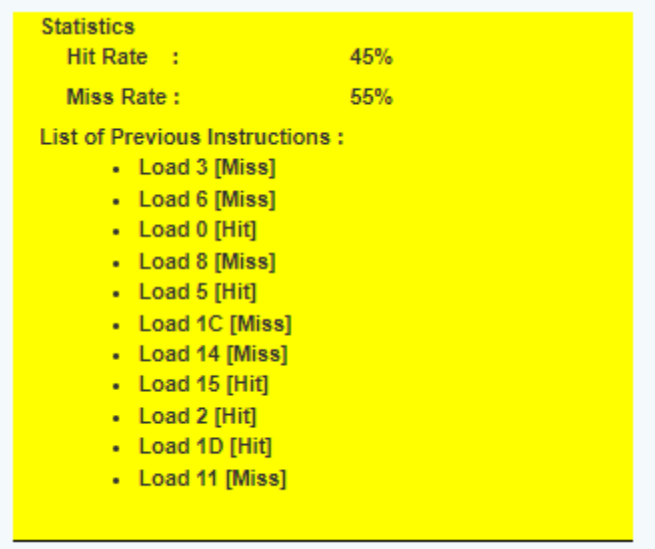
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 2 W. 0 - 0	0
1	1	4	B. 9 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	3	B. 6 W. 0 - 0	0
1	1	1	B. 3 W. 0 - 0	0

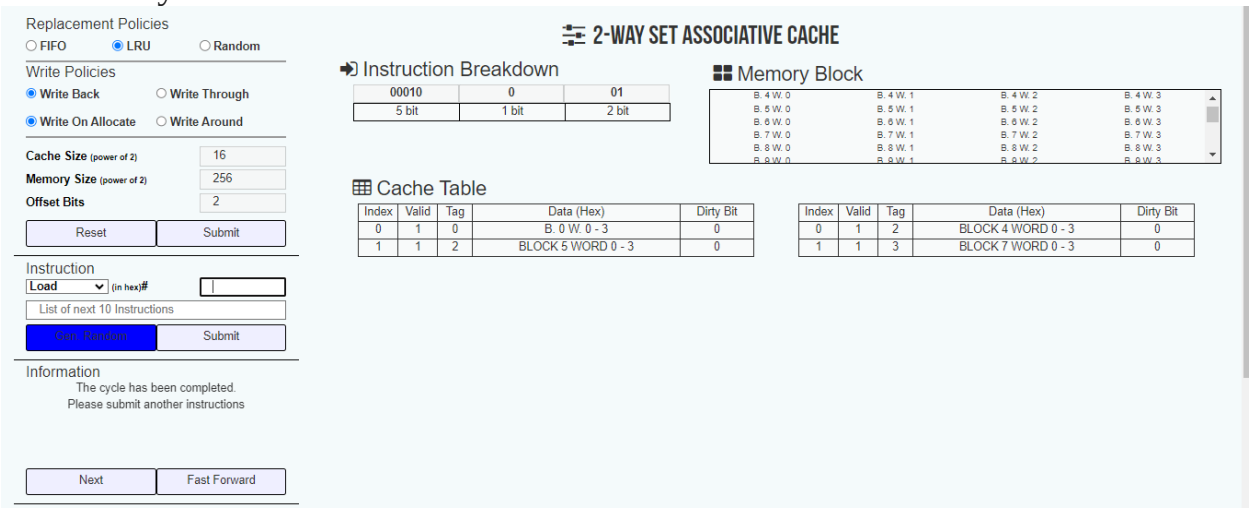
3. Consider 2 way set associative mapping with following design : cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:
   3,6,0,8,5,1c,14,15,2,1D,11
   Use LRU and FIFO as replacement policy

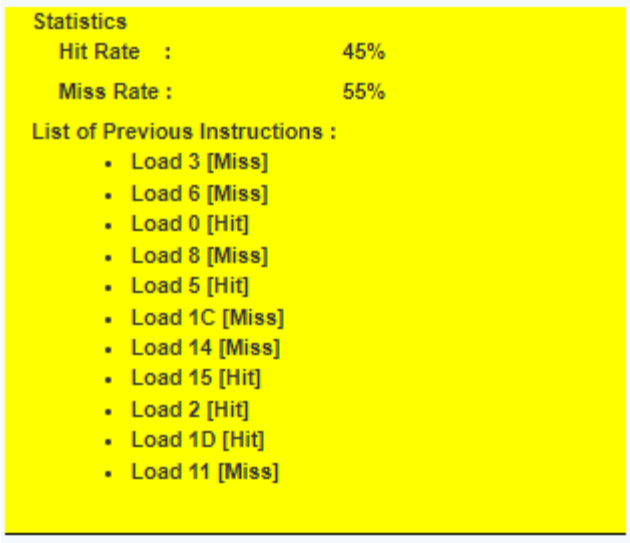
   FIFO Policy:





LRU Policy:





SET Associative mapping:

Try using PARACACHE SIMULATOR for the above exercise for the following configuration.

1. Cache Size: 32 words
2. Memory Size: 131072 words[main memory].
3. Block Size: 4 words

given as word addresses.

1. 1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221
2. 6, 214, 175, 214, 6, 84, 65, 174, 64, 105, 85, 215

2 way set associative mapping, FIFO policy and write back policy to calculate hit and miss ratio