

MPCA – Paracache Simulator

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Load 0:

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

8

Memory Size (power of 2)

64

Offset Bits

2

Reset

Submit

Instruction

Load (in hex)#

0

List of next 10 Instructions

Gen. Random

Submit

Information

Cache table is updated accordingly.
Block 0 with offset 0 to 3 is transferred to cache

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :

DIRECT MAPPED CACHE

Instruction Breakdown

000	0	00
3 bit	1 bit	2 bit

Memory Block

B 0 W 0	B 0 W 1	B 0 W 2	B 0 W 3
B 1 W 0	B 1 W 1	B 1 W 2	B 1 W 3
B 2 W 0	B 2 W 1	B 2 W 2	B 2 W 3
B 3 W 0	B 3 W 1	B 3 W 2	B 3 W 3
B 4 W 0	B 4 W 1	B 4 W 2	B 4 W 3
B 5 W 0	B 5 W 1	B 5 W 2	B 5 W 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 3	0
1	0	-	0	0

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load 0 [Miss]

Store 2:

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

8

Memory Size (power of 2)

64

Offset Bits

2

Reset

Submit

Instruction

Store (in hex)#

2

List of next 10 Instructions

Gen. Random

Submit

Information

Highlighted cache is updated with dirty bit = 1

Next

Fast Forward

Statistics

Hit Rate : 63%
Miss Rate : 38%

List of Previous Instructions :

- Load 0 [Miss]
- Store 2 [Hit]
- Load 0 [Miss]
- Load 0 [Hit]
- Store 2 [Miss]
- Store 2 [Hit]
- Store 2 [Hit]
- Store 2 [Hit]

DIRECT MAPPED CACHE

Instruction Breakdown

000	0	10
3 bit	1 bit	2 bit

Memory Block

B 0 W 0	B 0 W 1	B 0 W 2	B 0 W 3
B 1 W 0	B 1 W 1	B 1 W 2	B 1 W 3
B 2 W 0	B 2 W 1	B 2 W 2	B 2 W 3
B 3 W 0	B 3 W 1	B 3 W 2	B 3 W 3
B 4 W 0	B 4 W 1	B 4 W 2	B 4 W 3
B 5 W 0	B 5 W 1	B 5 W 2	B 5 W 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 3	1
1	0	-	0	0

Load B

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back

☐ Write Through

☒ Write On Allocate

☐ Write Around

Cache Size (power of 2)

8

Memory Size (power of 2)

64

Offset Bits

2

Reset

Submit

Instruction

Load

(in hex#)

B

List of next 10 Instructions

Gen. Random

Submit

Information

Cache replace the old index. Since dirty bit is 1, Memory will be updated.

Next

Fast Forward

Statistics

Hit Rate : 50%

Miss Rate : 50%

List of Previous Instructions :

• Load 0 [Miss]

• Store 2 [Hit]

DIRECT MAPPED CACHE

Instruction Breakdown

001	0	11
3 bit	1 bit	2 bit

Memory Block

B. 0 W. 0	B. 0 W. 1	B. 0 W. 2	B. 0 W. 3
B. 1 W. 0	B. 1 W. 1	B. 1 W. 2	B. 1 W. 3
B. 2 W. 0	B. 2 W. 1	B. 2 W. 2	B. 2 W. 3
B. 3 W. 0	B. 3 W. 1	B. 3 W. 2	B. 3 W. 3
B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 3	1
1	0	-	0	0

Assignment Questions

Question 1:

1)DMC WB

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back

☐ Write Through

☒ Write On Allocate

☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

131072

Offset Bits

2

Reset

Submit

Instruction

Load

(in hex#)

List of next 10 Instructions

Gen. Random

Submit

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 33%

Miss Rate : 67%

List of Previous Instructions :

• Load 1 [Miss]

• Load 134 [Miss]

• Load 212 [Miss]

• Load 1 [Hit]

• Load 135 [Hit]

• Load 213 [Hit]

• Load 162 [Miss]

• Load 161 [Hit]

• Load 2 [Miss]

• Load 44 [Miss]

• Load 41 [Miss]

• Load 221 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

000000010001	000	01
12 bit	3 bit	2 bit

Memory Block

B. 88 W. 0	B. 88 W. 1	B. 88 W. 2	B. 88 W. 3
B. 89 W. 0	B. 89 W. 1	B. 89 W. 2	B. 89 W. 3
B. 8A W. 0	B. 8A W. 1	B. 8A W. 2	B. 8A W. 3
B. 8B W. 0	B. 8B W. 1	B. 8B W. 2	B. 8B W. 3
B. 8C W. 0	B. 8C W. 1	B. 8C W. 2	B. 8C W. 3
B. 8D W. 0	B. 8D W. 1	B. 8D W. 2	B. 8D W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000010001	BLOCK 88 WORD 0 - 3	0
1	1	000000000010	BLOCK 11 WORD 0 - 3	0
2	0	-	0	0
3	0	-	0	0
4	1	000000010000	BLOCK 84 WORD 0 - 3	0
5	1	000000001001	BLOCK 4D WORD 0 - 3	0
6	0	-	0	0
7	0	-	0	0

2) DMC WRITE THROUGH

Write Policies

☐ Write Back
 ☒ Write Through
 ☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

131072

Offset Bits

2

Reset

Submit

Instruction

Load

in hex#

List of next 10 Instructions

Submit

Information

The cycle has been completed
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 33%

Miss Rate : 67%

List of Previous Instructions :

- Load 1 (Miss)
- Load 134 (Miss)
- Load 212 (Miss)
- Load 1 (Hit)
- Load 135 (Hit)
- Load 212 (Hit)
- Load 162 (Miss)
- Load 161 (Hit)
- Load 2 (Miss)
- Load 64 (Miss)
- Load 41 (Miss)
- Load 221 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

00000011001	000	01
12 bit	3 bit	2 bit

Memory Block

B 33 W 0	B 33 W 1	B 33 W 2	B 33 W 3
B 34 W 0	B 34 W 1	B 34 W 2	B 34 W 3
B 35 W 0	B 35 W 1	B 35 W 2	B 35 W 3
B 36 W 0	B 36 W 1	B 36 W 2	B 36 W 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000010001	BLOCK 88 WORD 0 - 3	0
1	1	00000000010	BLOCK 11 WORD 0 - 3	0
2	0	-	0	0
3	0	-	0	0
4	1	00000001000	BLOCK 84 WORD 0 - 3	0
5	1	000000001001	BLOCK 40 WORD 0 - 3	0
6	0	-	0	0
7	0	-	0	0

ii)

Write Policies

☐ Write Back
 ☐ Write Through
 ☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

131072

Offset Bits

2

Reset

Submit

Instruction

Load

in hex#

List of next 10 Instructions

Submit

Information

The cycle has been completed
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 17%

Miss Rate : 83%

List of Previous Instructions :

- Load 6 (Miss)
- Load 214 (Miss)
- Load 175 (Miss)
- Load 214 (Miss)
- Load 6 (Hit)
- Load 64 (Miss)
- Load 61 (Miss)
- Load 134 (Miss)
- Load 64 (Hit)
- Load 195 (Miss)
- Load 85 (Miss)
- Load 215 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

000000010000	101	01
12 bit	3 bit	2 bit

Memory Block

B 71 W 0	B 71 W 1	B 71 W 2	B 71 W 3
B 72 W 0	B 72 W 1	B 72 W 2	B 72 W 3
B 73 W 0	B 73 W 1	B 73 W 2	B 73 W 3
B 74 W 0	B 74 W 1	B 74 W 2	B 74 W 3
B 75 W 0	B 75 W 1	B 75 W 2	B 75 W 3
B 76 W 0	B 76 W 1	B 76 W 2	B 76 W 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	1	00000000100	BLOCK 21 WORD 0 - 3	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	1	00000001000	BLOCK 85 WORD 0 - 3	0
6	0	-	0	0
7	0	-	0	0

Write Policies

☐ Write Back
 ☒ Write Through
 ☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

131072

Offset Bits

2

Reset

Submit

Instruction

Load

in hex#

List of next 10 Instructions

Submit

Information

The cycle has been completed
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 17%

Miss Rate : 83%

List of Previous Instructions :

- Load 6 (Miss)
- Load 214 (Miss)
- Load 175 (Miss)
- Load 214 (Miss)
- Load 6 (Hit)
- Load 84 (Miss)
- Load 65 (Miss)
- Load 174 (Miss)
- Load 64 (Hit)
- Load 195 (Miss)
- Load 85 (Miss)
- Load 215 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

000000010000	101	01
12 bit	3 bit	2 bit

Memory Block

B 85 W 0	B 85 W 1	B 85 W 2	B 85 W 3
B 86 W 0	B 86 W 1	B 86 W 2	B 86 W 3
B 87 W 0	B 87 W 1	B 87 W 2	B 87 W 3
B 88 W 0	B 88 W 1	B 88 W 2	B 88 W 3
B 89 W 0	B 89 W 1	B 89 W 2	B 89 W 3
B 90 W 0	B 90 W 1	B 90 W 2	B 90 W 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	1	00000000100	BLOCK 21 WORD 0 - 3	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	1	00000001000	BLOCK 85 WORD 0 - 3	0
6	0	-	0	0
7	0	-	0	0

Question 2:

i) DMC WB

Write Policies

☒ Write Back
 ☐ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2): 32
Memory Size (power of 2): 65536
Offset Bits: 4

Instruction
 Load

Information
 The cycle has been completed.
 Please submit another instructions.

Statistics
 Hit Ratio: 20%
 Miss Ratio: 75%
 List of Previous Instructions:
 • Load 1 (Miss)
 • Load 124 (Miss)
 • Load 212 (Miss)
 • Load 1 (Hit)
 • Load 125 (Miss)
 • Load 213 (Miss)
 • Load 152 (Miss)
 • Load 151 (Hit)
 • Load 2 (Miss)
 • Load 48 (Miss)
 • Load 49 (Hit)
 • Load 221 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

00000010001	0	0001
11 Hit	1 Hit	4 Hit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000010001	BLOCK 22 WORD 0 - 15	0
1	1	00000010000	BLOCK 21 WORD 0 - 15	0

Memory Block

Block	Word	Hex
0	0	0x00000000
0	1	0x00000001
0	2	0x00000002
0	3	0x00000003
0	4	0x00000004
0	5	0x00000005
0	6	0x00000006
0	7	0x00000007
0	8	0x00000008
0	9	0x00000009
0	10	0x0000000A
0	11	0x0000000B
0	12	0x0000000C
0	13	0x0000000D
0	14	0x0000000E
0	15	0x0000000F
1	0	0x00000010
1	1	0x00000011
1	2	0x00000012
1	3	0x00000013
1	4	0x00000014
1	5	0x00000015
1	6	0x00000016
1	7	0x00000017
1	8	0x00000018
1	9	0x00000019
1	10	0x0000001A
1	11	0x0000001B
1	12	0x0000001C
1	13	0x0000001D
1	14	0x0000001E
1	15	0x0000001F

WRITE THROUGH

Write Policies

☐ Write Back
 ☒ Write Through

☐ Write On Allocate
 ☐ Write Around

Cache Size (power of 2): 32
Memory Size (power of 2): 65536
Offset Bits: 4

Instruction
 Load

Information
 The cycle has been completed.
 Please submit another instructions.

Statistics
 Hit Ratio: 20%
 Miss Ratio: 75%
 List of Previous Instructions:
 • Load 1 (Miss)
 • Load 124 (Miss)
 • Load 212 (Miss)
 • Load 1 (Hit)
 • Load 125 (Miss)
 • Load 213 (Miss)
 • Load 152 (Miss)
 • Load 151 (Hit)
 • Load 2 (Miss)
 • Load 48 (Miss)
 • Load 49 (Hit)
 • Load 221 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

00000010001	0	0001
11 Hit	1 Hit	4 Hit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000010001	BLOCK 22 WORD 0 - 15	0
1	1	00000010000	BLOCK 21 WORD 0 - 15	0

Memory Block

Block	Word	Hex
0	0	0x00000000
0	1	0x00000001
0	2	0x00000002
0	3	0x00000003
0	4	0x00000004
0	5	0x00000005
0	6	0x00000006
0	7	0x00000007
0	8	0x00000008
0	9	0x00000009
0	10	0x0000000A
0	11	0x0000000B
0	12	0x0000000C
0	13	0x0000000D
0	14	0x0000000E
0	15	0x0000000F
1	0	0x00000010
1	1	0x00000011
1	2	0x00000012
1	3	0x00000013
1	4	0x00000014
1	5	0x00000015
1	6	0x00000016
1	7	0x00000017
1	8	0x00000018
1	9	0x00000019
1	10	0x0000001A
1	11	0x0000001B
1	12	0x0000001C
1	13	0x0000001D
1	14	0x0000001E
1	15	0x0000001F

ii)

Write Policies

☒ Write Back
 ☐ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

65536

Offset Bits

4

Reset

Submit

Instruction

Load

on hex#

List of next 10 Instructions

Run Program

Submit

Information

The cycle has been completed.

Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate :

17%

Miss Rate :

83%

List of Previous Instructions :

- Load 6 [Miss]
- Load 214 [Miss]
- Load 175 [Miss]
- Load 214 [Miss]
- Load 6 [Hit]
- Load 84 [Miss]
- Load 65 [Miss]
- Load 174 [Miss]
- Load 84 [Hit]
- Load 160 [Miss]
- Load 85 [Miss]
- Load 215 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

00000010000	1	0101
11 bit	1 bit	4 bit

Memory Block

B. 21 W. 0	B. 21 W. 1	B. 21 W. 2	B. 21 W. 3	B. 21 W. 4	B. 21 W. 5	B. 21 W. 6	B. 21 W. 7	B. 21 W. 8	B. 21 W. 9	B. 21 W. A	B. 21 W. B
B. 22 W. 0	B. 22 W. 1	B. 22 W. 2	B. 22 W. 3	B. 22 W. 4	B. 22 W. 5	B. 22 W. 6	B. 22 W. 7	B. 22 W. 8	B. 22 W. 9	B. 22 W. A	B. 22 W. B
B. 23 W. 0	B. 23 W. 1	B. 23 W. 2	B. 23 W. 3	B. 23 W. 4	B. 23 W. 5	B. 23 W. 6	B. 23 W. 7	B. 23 W. 8	B. 23 W. 9	B. 23 W. A	B. 23 W. B
B. 24 W. 0	B. 24 W. 1	B. 24 W. 2	B. 24 W. 3	B. 24 W. 4	B. 24 W. 5	B. 24 W. 6	B. 24 W. 7	B. 24 W. 8	B. 24 W. 9	B. 24 W. A	B. 24 W. B

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000000100	BLOCK 8 WORD 0 - 15	0
1	1	00000010000	BLOCK 21 WORD 0 - 15	0

WRITE THROUGH

ParaCache

Direct Mapped Cache

Fully Associative Cache

2-Way SA

4-Way SA

Cache Type Analysis

Virtual Memory

Knowledge Base

Write Policies

☐ Write Back
 ☒ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

65536

Offset Bits

4

Reset

Submit

Instruction

Load

on hex#

List of next 10 Instructions

Run Program

Submit

Information

The cycle has been completed.

Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate :

25%

Miss Rate :

75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Miss]
- Load 213 [Miss]
- Load 162 [Miss]
- Load 161 [Hit]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Hit]
- Load 221 [Miss]
- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Hit]
- Load 135 [Miss]
- Load 213 [Miss]
- Load 162 [Miss]
- Load 161 [Hit]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Hit]
- Load 221 [Miss]
- Load 8 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

00000010000	1	0101
11 bit	1 bit	4 bit

Memory Block

B. 21 W. 0	B. 21 W. 1	B. 21 W. 2	B. 21 W. 3	B. 21 W. 4	B. 21 W. 5	B. 21 W. 6	B. 21 W. 7	B. 21 W. 8	B. 21 W. 9	B. 21 W. A	B. 21 W. B
B. 22 W. 0	B. 22 W. 1	B. 22 W. 2	B. 22 W. 3	B. 22 W. 4	B. 22 W. 5	B. 22 W. 6	B. 22 W. 7	B. 22 W. 8	B. 22 W. 9	B. 22 W. A	B. 22 W. B
B. 23 W. 0	B. 23 W. 1	B. 23 W. 2	B. 23 W. 3	B. 23 W. 4	B. 23 W. 5	B. 23 W. 6	B. 23 W. 7	B. 23 W. 8	B. 23 W. 9	B. 23 W. A	B. 23 W. B

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000000100	BLOCK 8 WORD 0 - 15	0
1	1	00000010000	BLOCK 21 WORD 0 - 15	0