

UE22CS251B : Microprocessor and Computer Architecture  
**Paracache Simulator- 2 way set associative and cache type analysis**  
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**Semester 4 Section J**

- Consider 4 way set associative mapping with following design : cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:  
3,6,0,8,5,1c,14,15,2,1D,11

Replacement Policies

☒ FIFO    ☐ LRU    ☐ Random

Write Policies

☒ Write Back    ☐ Write Through

☒ Write On Allocate    ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

**4-WAY SET ASSOCIATIVE CACHE**

➔ Instruction Breakdown

000100	0	01
6 bit	0 bit	2 bit

➡ Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3

➡ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B. 5 W. 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	B. 4 W. 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	7	B. 7 W. 0 - 3	0

Instruction

Load  (in hex)#

List of next 10 Instructions

Information

The cycle has been completed.  
Please submit another instructions

**Statistics**

Hit Rate : 36%

Miss Rate : 64%

List of Previous Instructions :

- Load 3 [Miss]
- Load 6 [Miss]
- Load 0 [Hit]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 1C [Miss]
- Load 14 [Miss]
- Load 15 [Hit]
- Load 2 [Miss]
- Load 1D [Hit]
- Load 11 [Miss]

## 2. Cache type analysis: Memory size: 64, Offset:0, Cache size:8

Input=L-0,L-3,L-4,L-1,L-2,L-5,L-7,S-6,L-0,L-3,L-1,L-11,L-5,L-15,L-9,S-4,L-0,L-4,S-3,L-12

### Cache Comparison

#### 1. Direct Mapped Cache[8]

HIT 40% MISS 60% || ADD. RESOURCES 184 NAND

Instruction Breakdown

010	010	0
3 bit	3 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	BLOCK 0 WORD 0 - 0	0
1	1	001	BLOCK 9 WORD 0 - 0	0
2	1	010	BLOCK 12 WORD 0 - 0	0
3	1	0	BLOCK 3 WORD 0 - 0	1
4	1	0	BLOCK 4 WORD 0 - 0	1
5	1	010	BLOCK 15 WORD 0 - 0	0
6	1	0	BLOCK 6 WORD 0 - 0	0
7	1	0	BLOCK 7 WORD 0 - 0	0

#### 2. Fully Associative Cache[8]

HIT 25% MISS 75% || ADD. RESOURCES 1808 NAND

Instruction Breakdown

010010	0
6 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	17	BLOCK 11 WORD 0 - 0	0
1	1	21	BLOCK 15 WORD 0 - 0	0
2	1	9	BLOCK 9 WORD 0 - 0	0
3	1	4	BLOCK 4 WORD 0 - 0	0
4	1	0	BLOCK 0 WORD 0 - 0	0
5	1	3	BLOCK 3 WORD 0 - 0	0
6	1	18	BLOCK 12 WORD 0 - 0	0
7	1	6	BLOCK 6 WORD 0 - 0	0

#### 3. 2-Way Set Associative Cache[4]

HIT 40% MISS 60% || ADD. RESOURCES 336 NAND

Instruction Breakdown

0100	10	0
4 bit	2 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 0	0
1	1	2	B. 9 W. 0 - 0	0
2	1	4	B. 12 W. 0 - 0	0
3	1	0	B. 3 W. 0 - 0	1

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 4 W. 0 - 0	1
1	1	5	B. 15 W. 0 - 0	0
2	1	1	B. 6 W. 0 - 0	0
3	1	1	B. 7 W. 0 - 0	0

#### 4. 4-Way Set Associative Cache[2]

HIT 35% MISS 65% || ADD. RESOURCES 520 NAND

Instruction Breakdown

01001	0	0
5 bit	1 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	9	B. 12 W. 0 - 0	0
1	1	8	B. 11 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B. 4 W. 0 - 0	1
1	1	10	B. 15 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 2 W. 0 - 0	0
1	1	4	B. 9 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	3	B. 6 W. 0 - 0	0
1	1	1	B. 3 W. 0 - 0	0

3. Consider 2 way set associative mapping with following design : cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

3,6,0,8,5,1c,14,15,2,1D,11

Use LRU and FIFO as replacement policy

FIFO Policy:

Replacement Policies  
☒ FIFO ☐ LRU ☐ Random

Write Policies  
☒ Write Back ☐ Write Through  
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)   
Memory Size (power of 2)   
Offset Bits

Instruction  
Load (in hex)#   
List of next 10 Instructions

Information  
The cycle has been completed.  
Please submit another instructions

### 2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00010	0	01
5 bit	1 bit	2 bit

Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 4 WORD 0 - 3	0
1	1	2	BLOCK 5 WORD 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 2 WORD 0 - 3	0
1	1	3	BLOCK 7 WORD 0 - 3	0

#### Statistics

Hit Rate : 45%

Miss Rate : 55%

#### List of Previous Instructions :

- Load 3 [Miss]
- Load 6 [Miss]
- Load 0 [Hit]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 1C [Miss]
- Load 14 [Miss]
- Load 15 [Hit]
- Load 2 [Hit]
- Load 1D [Hit]
- Load 11 [Miss]

## LRU Policy:

Replacement Policies

☐ FIFO ☒ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

(in hex)#

List of next 10 Instructions

Information

The cycle has been completed.  
Please submit another instructions

**2-WAY SET ASSOCIATIVE CACHE**

**Instruction Breakdown**

00010	0	01
5 bit	1 bit	2 bit

**Memory Block**

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 3	0
1	1	2	BLOCK 5 WORD 0 - 3	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 4 WORD 0 - 3	0
1	1	3	BLOCK 7 WORD 0 - 3	0

<b>Statistics</b>	
Hit Rate :	45%
Miss Rate :	55%
<b>List of Previous Instructions :</b>	
<ul style="list-style-type: none"> <li>• Load 3 [Miss]</li> <li>• Load 6 [Miss]</li> <li>• Load 0 [Hit]</li> <li>• Load 8 [Miss]</li> <li>• Load 5 [Hit]</li> <li>• Load 1C [Miss]</li> <li>• Load 14 [Miss]</li> <li>• Load 15 [Hit]</li> <li>• Load 2 [Hit]</li> <li>• Load 1D [Hit]</li> <li>• Load 11 [Miss]</li> </ul>	

## SET Associative mapping:

Try using PARACACHE SIMULATOR for the above exercise for the following configuration.

1. Cache Size: 32 words
2. Memory Size: 131072 words[main memory].
3. Block Size: 4 words

given as word addresses.

1. 1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221
2. 6, 214, 175, 214, 6, 84, 65, 174, 64, 105, 85, 215

2 way set associative mapping, FIFO policy and write back policy to calculate hit and miss ratio

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

131072

Offset Bits

4

Reset

Submit

Instruction

Load  (in hex)#

List of next 10 Instructions

Run Random

Submit

Information

The cycle has been completed.  
Please submit another instructions

Next

Fast Forward

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0000000100010	0	0001
13 bit	0 bit	4 bit

Memory Block

B. 22 W. 0	B. 22 W. 1	B. 22 W. 2	B. 22 W. 3	B. 22 W. 4	B. 22 W. 5	B. 22 W. 6	B. 22 W. 7	B. 22 W. 8	B. 22 W. 9	B. 22 W. 10	B. 22 W. 11	B. 22 W. 12	B. 22 W. 13	B. 22 W. 14	B. 22 W. 15	B. 22 W. 16	B. 22 W. 17	B. 22 W. 18	B. 22 W. 19	B. 22 W. 20	B. 22 W. 21	B. 22 W. 22	B. 22 W. 23	B. 22 W. 24	B. 22 W. 25	B. 22 W. 26	B. 22 W. 27	B. 22 W. 28	B. 22 W. 29	B. 22 W. 30	B. 22 W. 31
B. 23 W. 0	B. 23 W. 1	B. 23 W. 2	B. 23 W. 3	B. 23 W. 4	B. 23 W. 5	B. 23 W. 6	B. 23 W. 7	B. 23 W. 8	B. 23 W. 9	B. 23 W. 10	B. 23 W. 11	B. 23 W. 12	B. 23 W. 13	B. 23 W. 14	B. 23 W. 15	B. 23 W. 16	B. 23 W. 17	B. 23 W. 18	B. 23 W. 19	B. 23 W. 20	B. 23 W. 21	B. 23 W. 22	B. 23 W. 23	B. 23 W. 24	B. 23 W. 25	B. 23 W. 26	B. 23 W. 27	B. 23 W. 28	B. 23 W. 29	B. 23 W. 30	B. 23 W. 31
B. 24 W. 0	B. 24 W. 1	B. 24 W. 2	B. 24 W. 3	B. 24 W. 4	B. 24 W. 5	B. 24 W. 6	B. 24 W. 7	B. 24 W. 8	B. 24 W. 9	B. 24 W. 10	B. 24 W. 11	B. 24 W. 12	B. 24 W. 13	B. 24 W. 14	B. 24 W. 15	B. 24 W. 16	B. 24 W. 17	B. 24 W. 18	B. 24 W. 19	B. 24 W. 20	B. 24 W. 21	B. 24 W. 22	B. 24 W. 23	B. 24 W. 24	B. 24 W. 25	B. 24 W. 26	B. 24 W. 27	B. 24 W. 28	B. 24 W. 29	B. 24 W. 30	B. 24 W. 31
B. 25 W. 0	B. 25 W. 1	B. 25 W. 2	B. 25 W. 3	B. 25 W. 4	B. 25 W. 5	B. 25 W. 6	B. 25 W. 7	B. 25 W. 8	B. 25 W. 9	B. 25 W. 10	B. 25 W. 11	B. 25 W. 12	B. 25 W. 13	B. 25 W. 14	B. 25 W. 15	B. 25 W. 16	B. 25 W. 17	B. 25 W. 18	B. 25 W. 19	B. 25 W. 20	B. 25 W. 21	B. 25 W. 22	B. 25 W. 23	B. 25 W. 24	B. 25 W. 25	B. 25 W. 26	B. 25 W. 27	B. 25 W. 28	B. 25 W. 29	B. 25 W. 30	B. 25 W. 31

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	BLOCK 4 WORD 0 - 15	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	22	BLOCK 22 WORD 0 - 15	0

### Statistics

Hit Rate : 17%

Miss Rate : 83%

### List of Previous Instructions :

- Load 1 [Miss]
- Load 134 [Miss]
- Load 212 [Miss]
- Load 1 [Miss]
- Load 135 [Miss]
- Load 213 [Miss]
- Load 162 [Miss]
- Load 161 [Hit]
- Load 2 [Miss]
- Load 44 [Miss]
- Load 41 [Hit]
- Load 221 [Miss]