**Digital Design and Computer Organisation Laboratory**

**UE22CS251A**

**3rd Semester, Academic Year 2023**

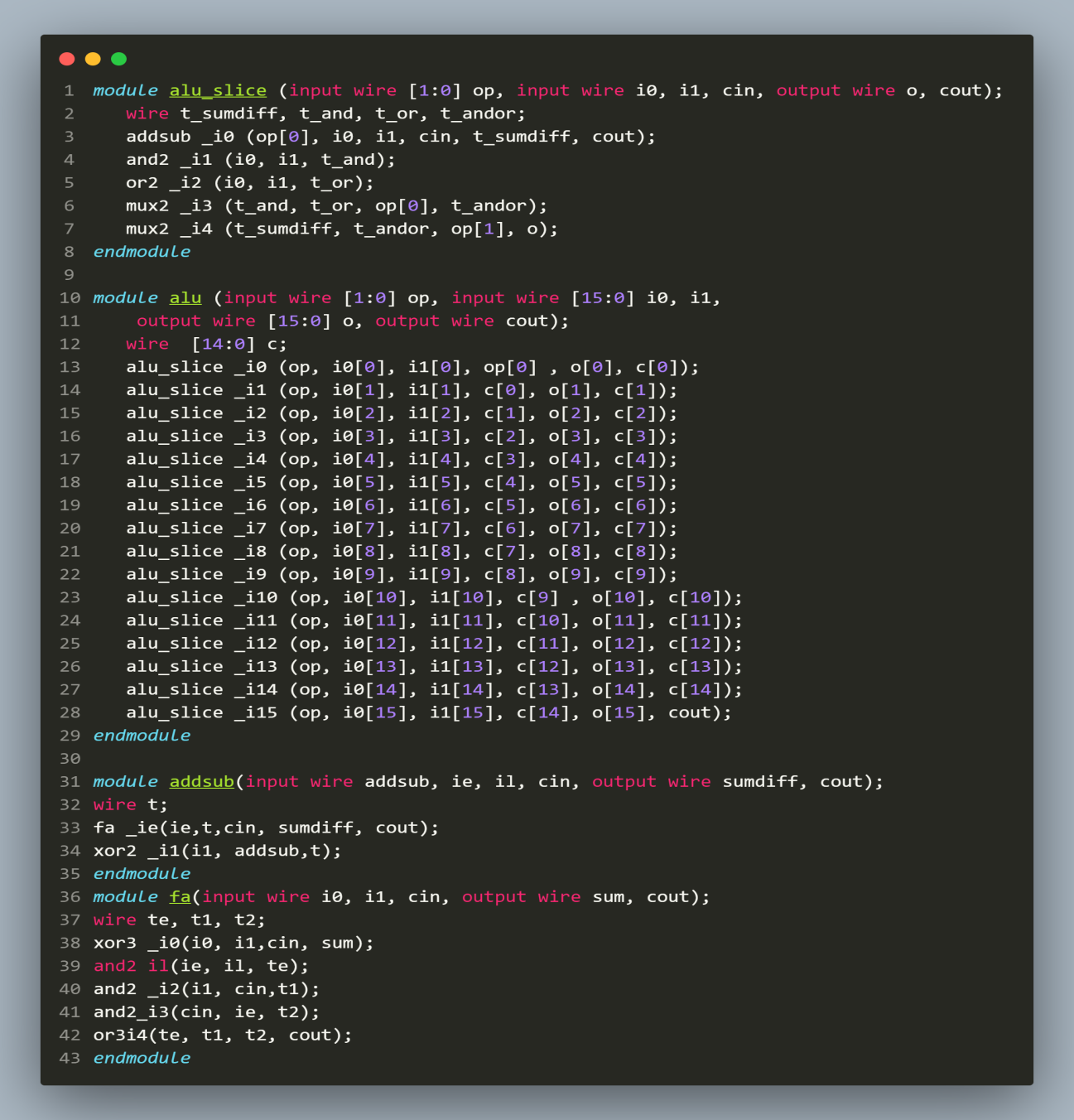
Date: 06-11-2023

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| --- | --- | --- |
| Name: Siri N Shetty | SRN: PES2UG22CS556 | Section: J |

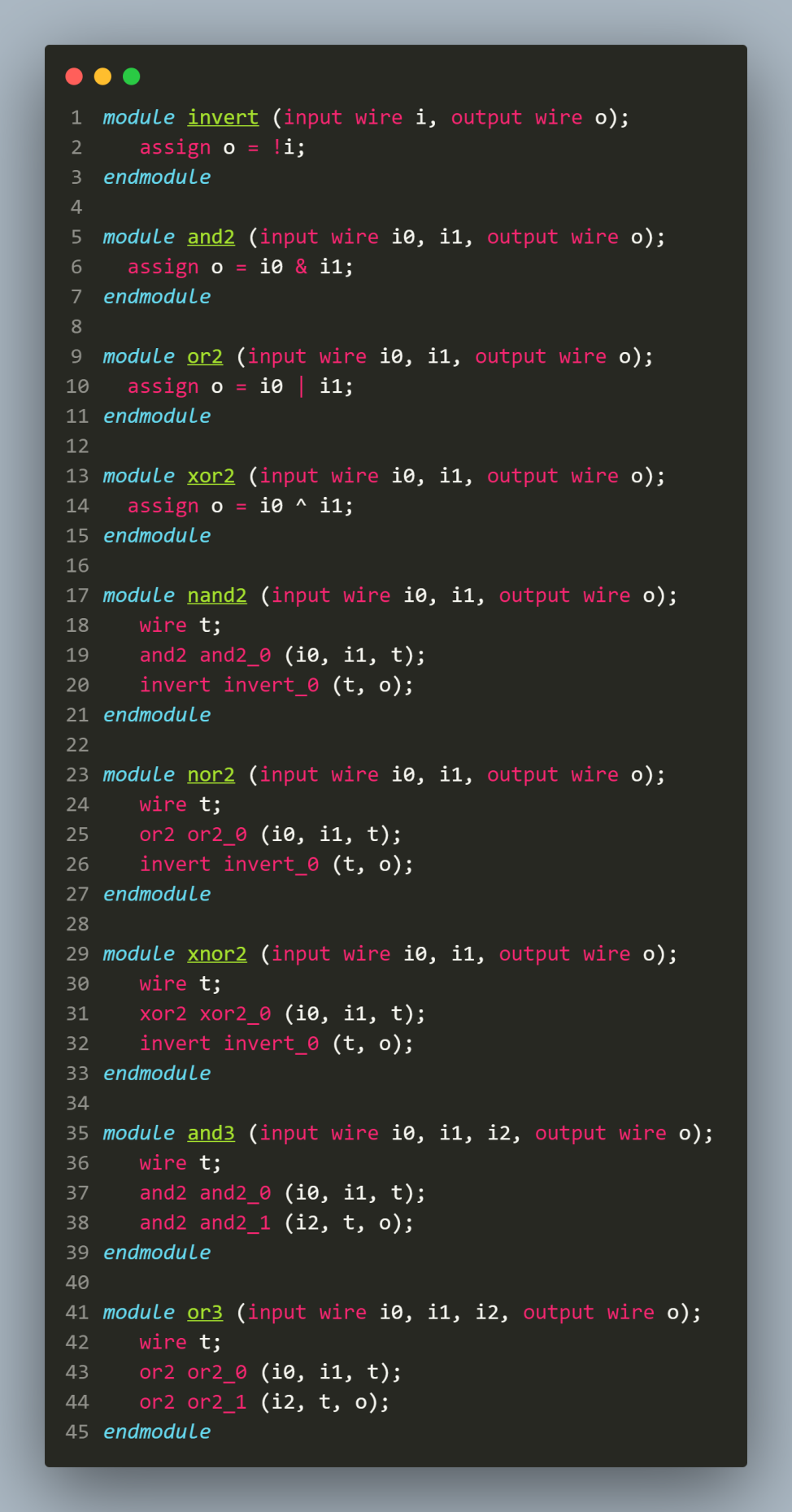
Week#\_\_\_\_7\_\_\_\_\_\_\_Program Number: \_\_\_\_1\_\_\_

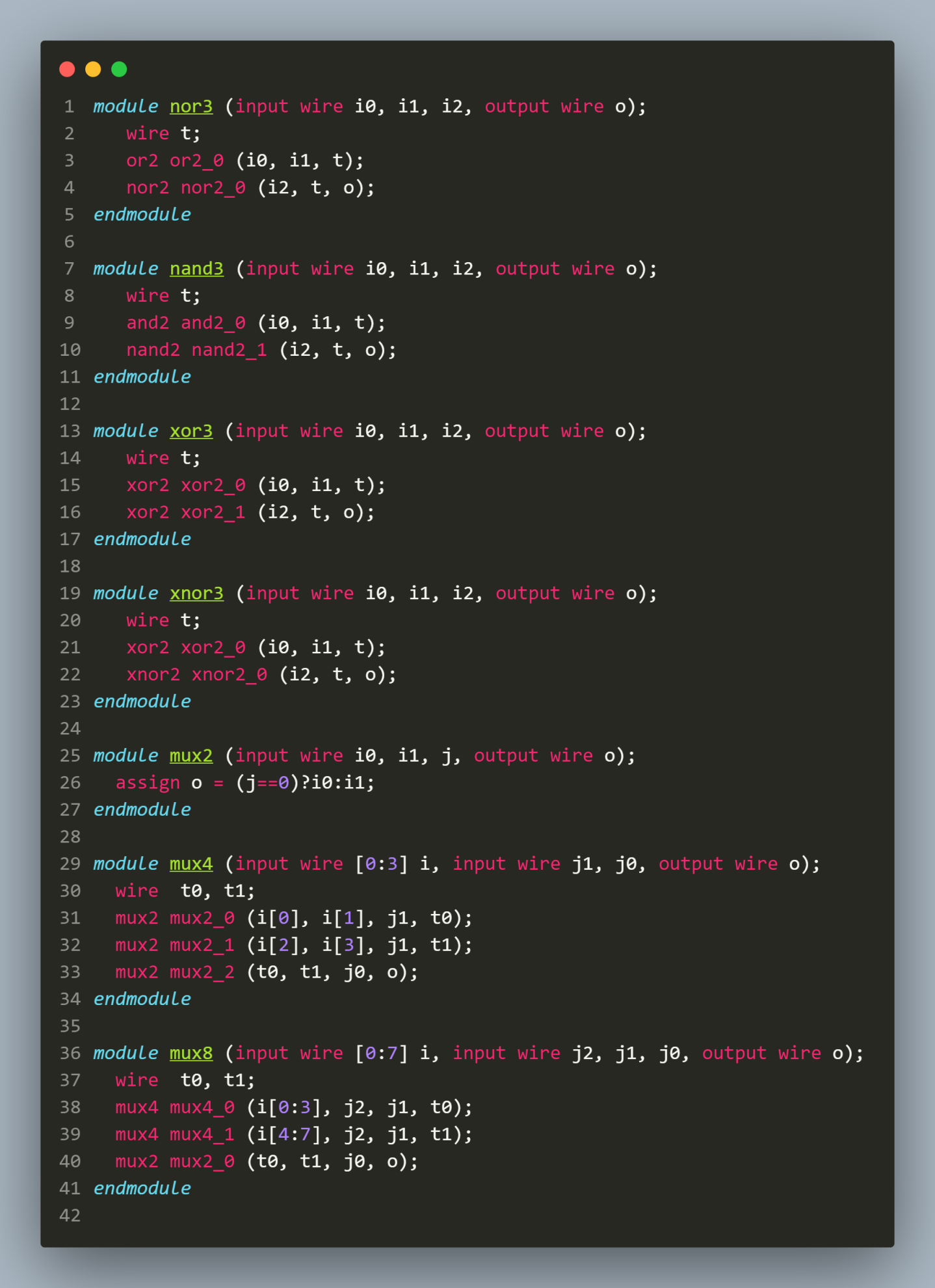
TITLE: **Microprocessor Control Logic**

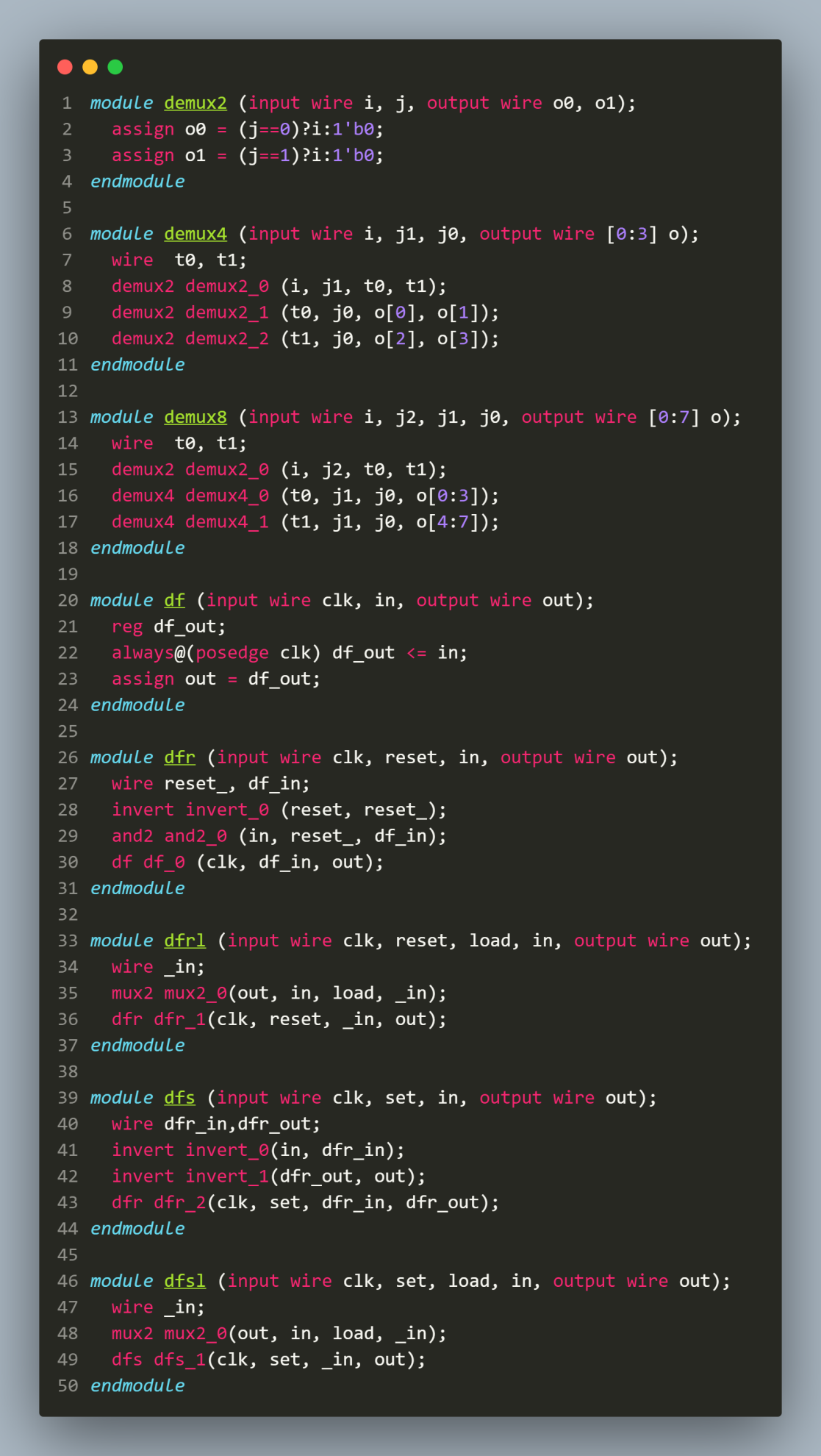
1. Verilog Code Screenshot (alu.v)



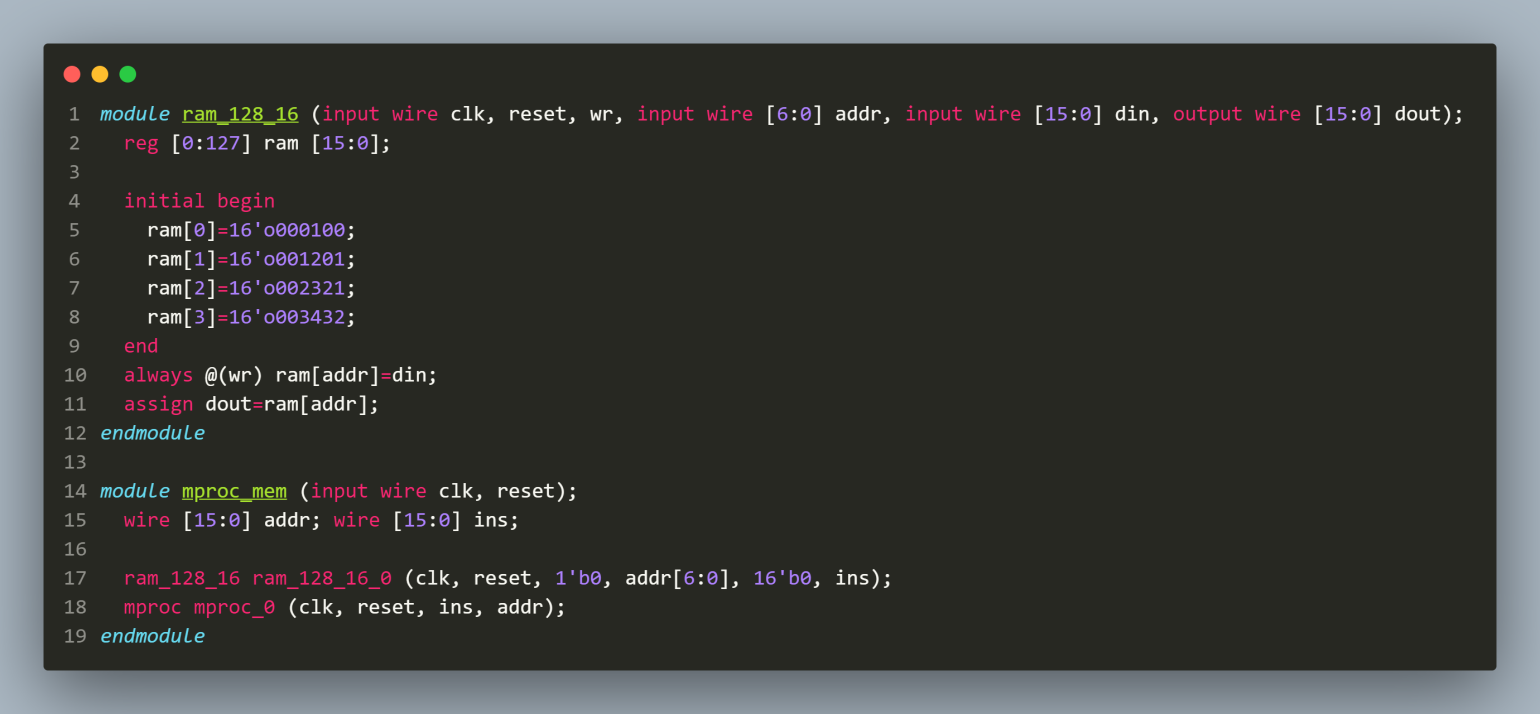
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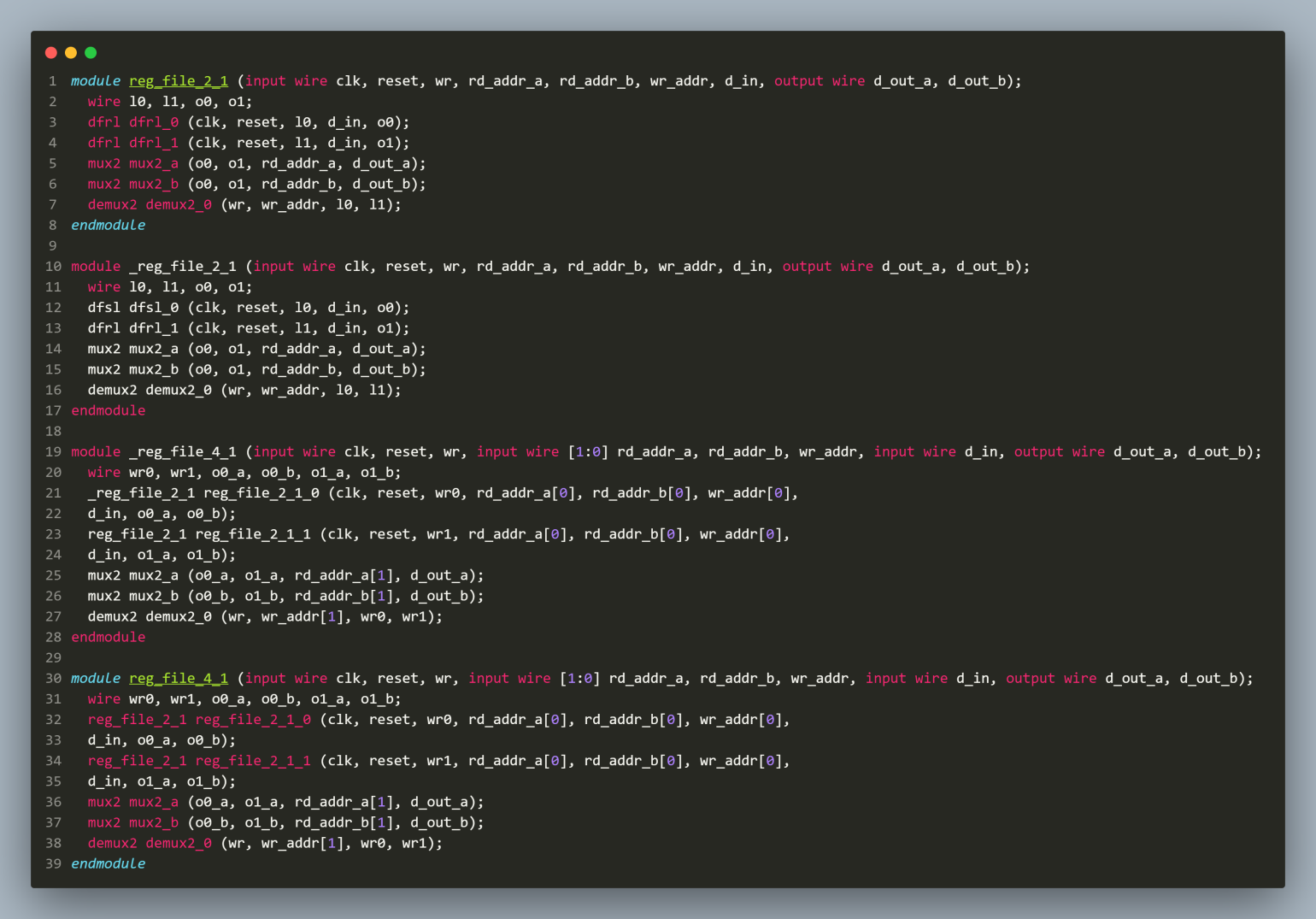




1. Verilog Code Screenshot (mproc\_mem.v)



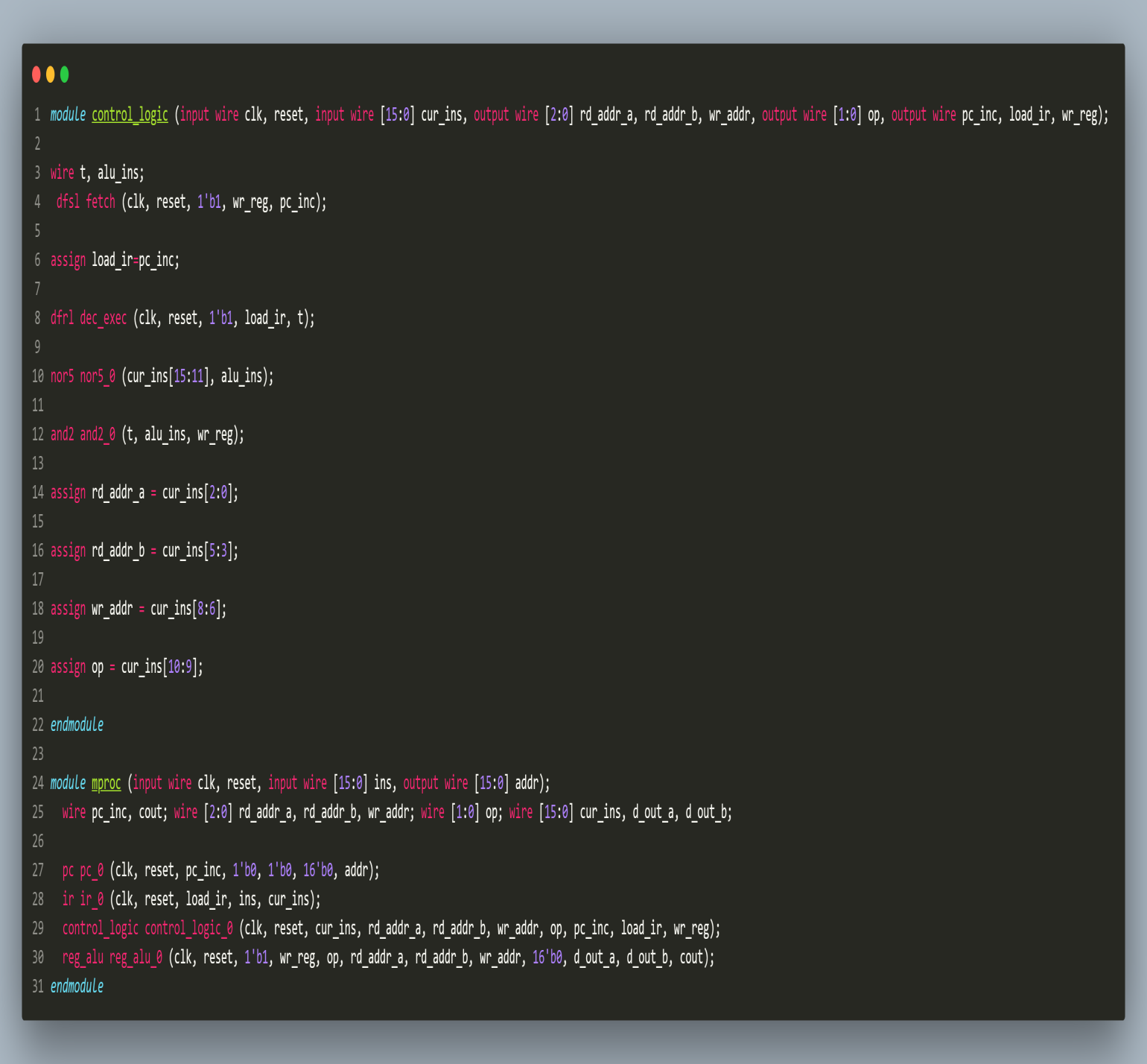
1. Verilog Code Screenshot (reg\_alu.v)





1. Verilog Code Screenshot (mproc.v)

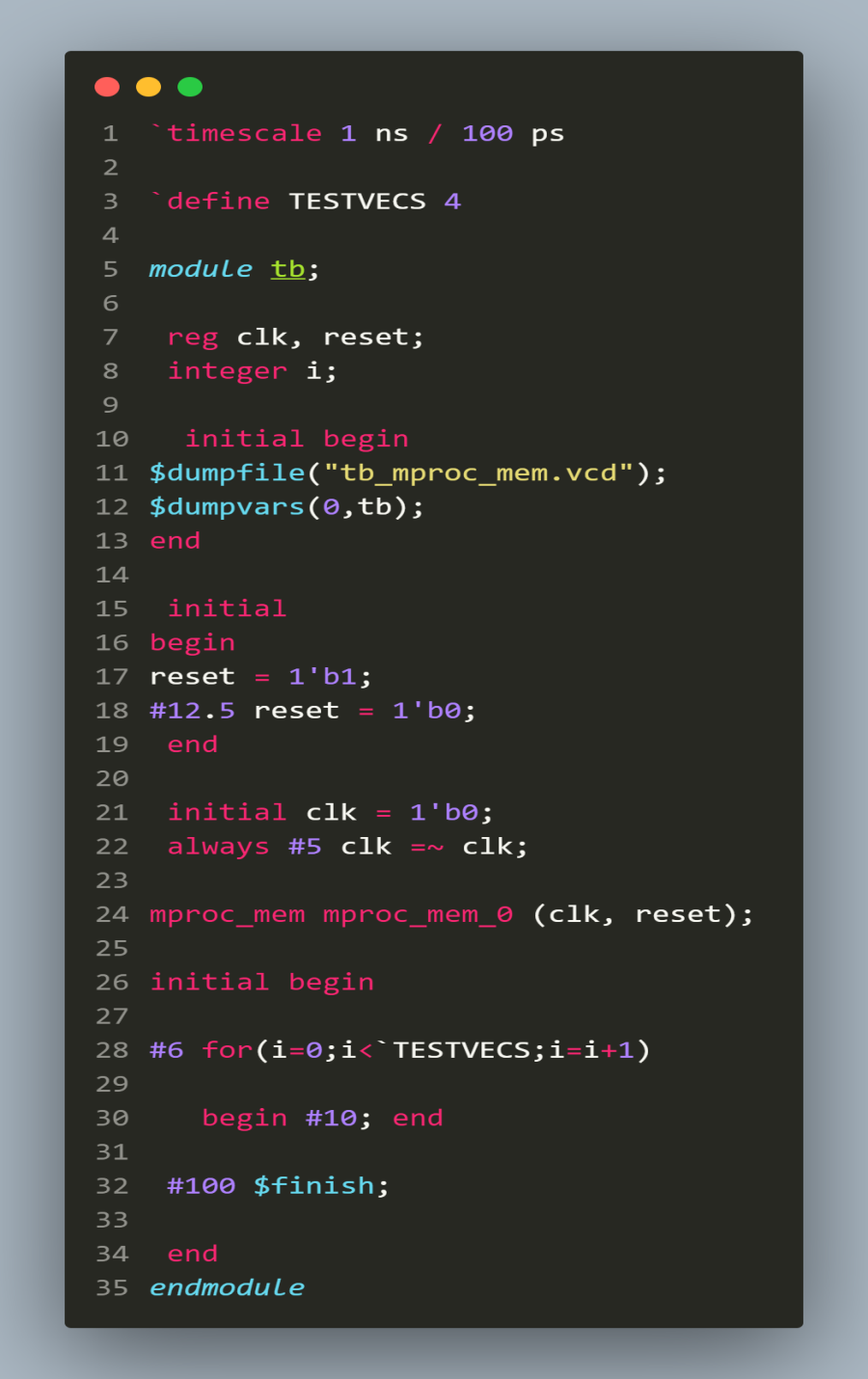




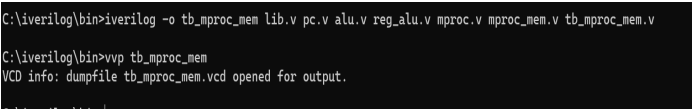
1. Verilog Code Screenshot (pc.v)



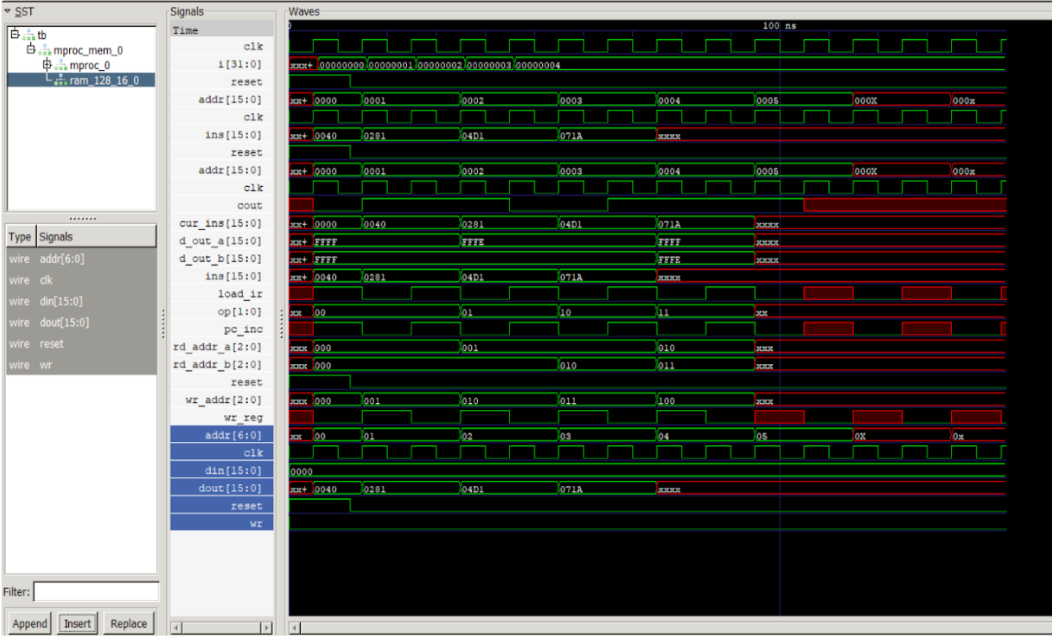
1. Verilog Code Screenshot (tb\_mproc\_mem.v)



1. Verilog VVP Output Screen Shot



1. GTKWAVE Screenshot



1. Output Table to be completed and included



**Disclaimer:**

* The programs and output submitted is duly written, verified and executed by me.
* I have not copied from any of my peers or from the external resource such as internet.
* If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name: Siri N Shetty

SRN: PES2UG22CS556

Section: J

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