X10 on the Single-chip Cloud Computer (SCC)

Keith Chapman, Ahmed Hussein, Antony Hosking

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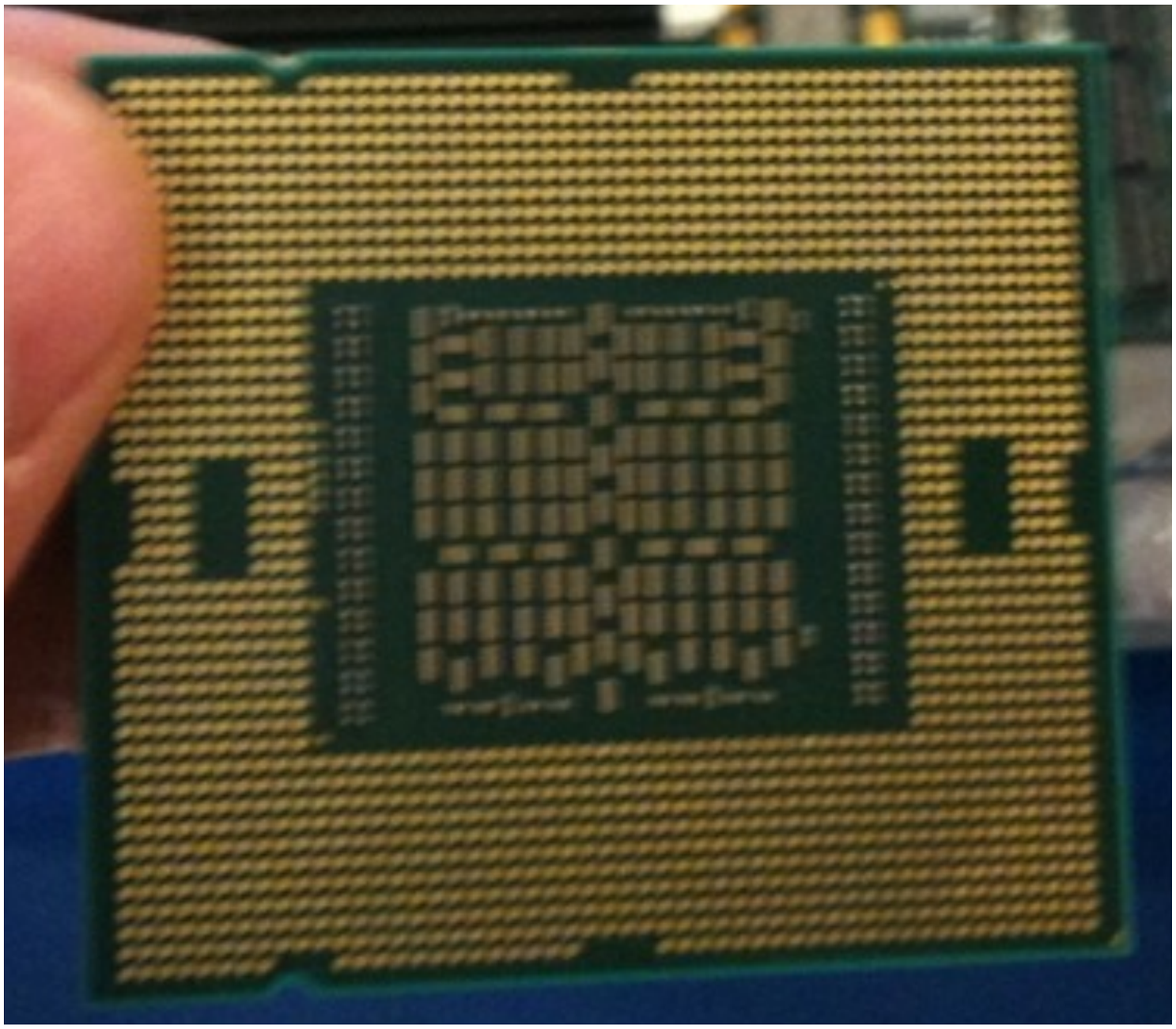
What is the SCC



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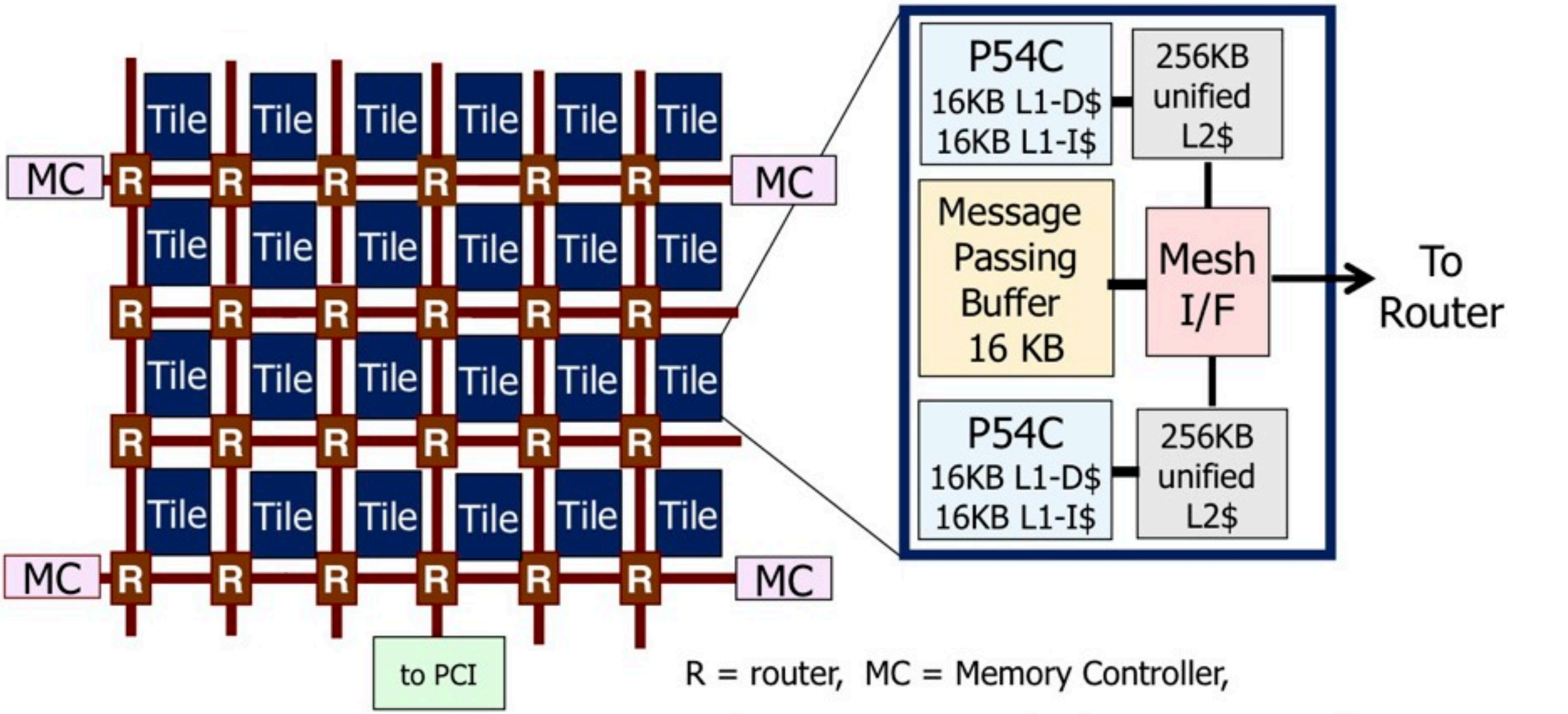

R = router, MC = Memory Controller,

P54C = second generation Pentium® core, CC = cache cntrl.

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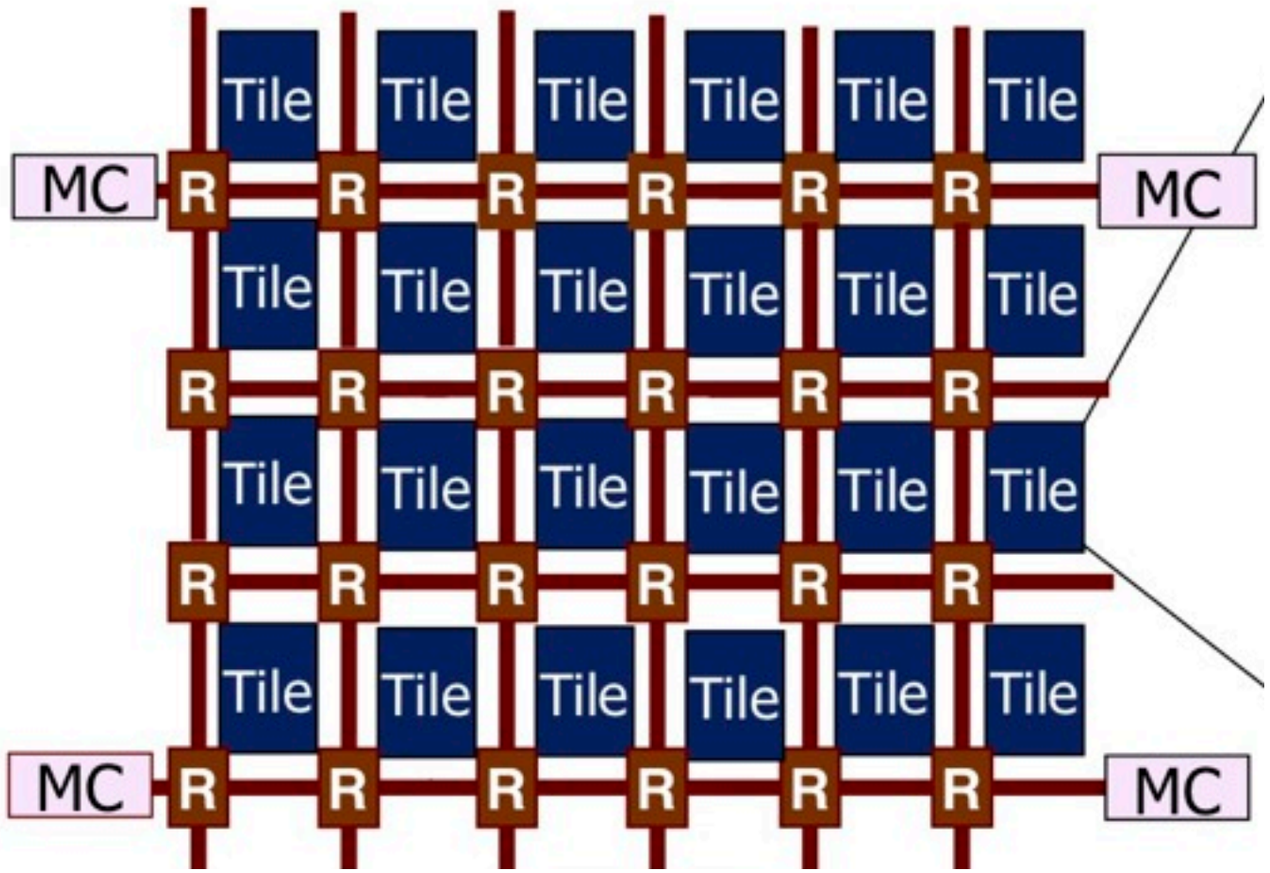

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What is the SCC

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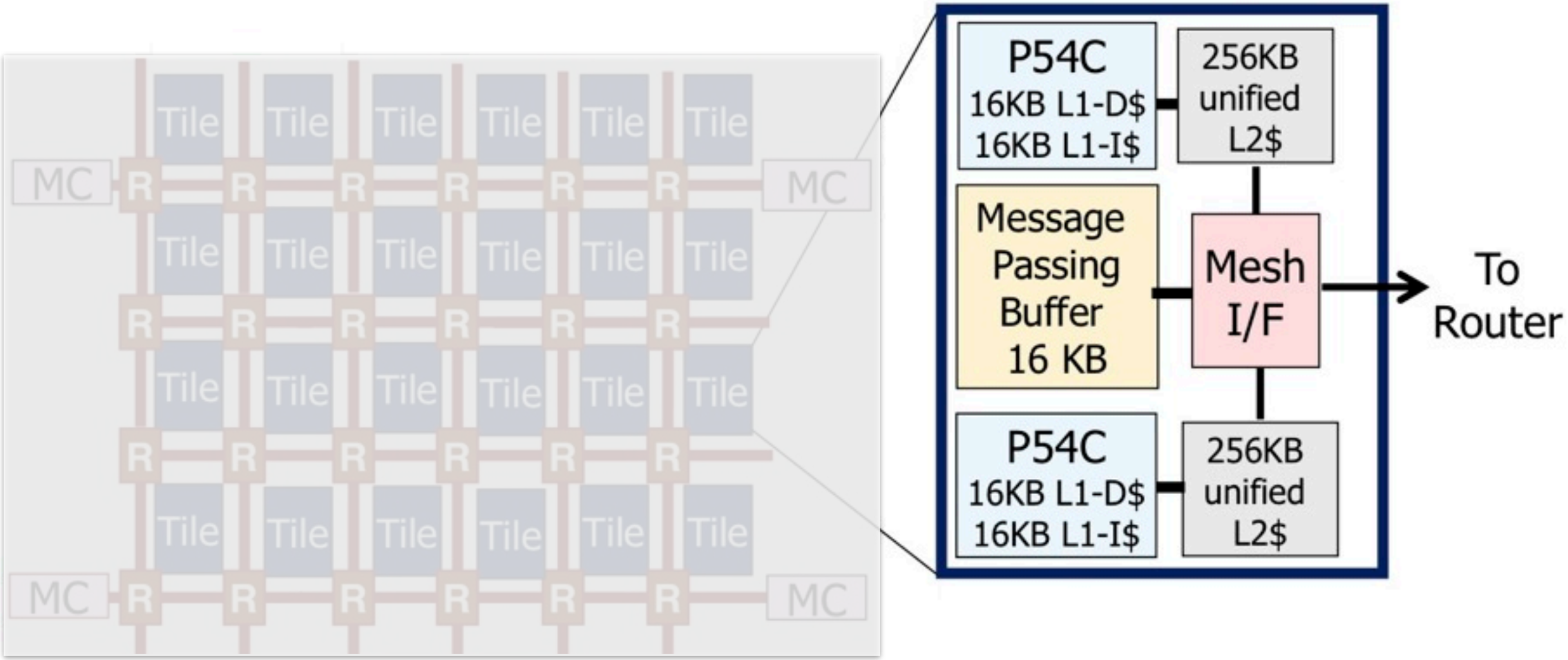

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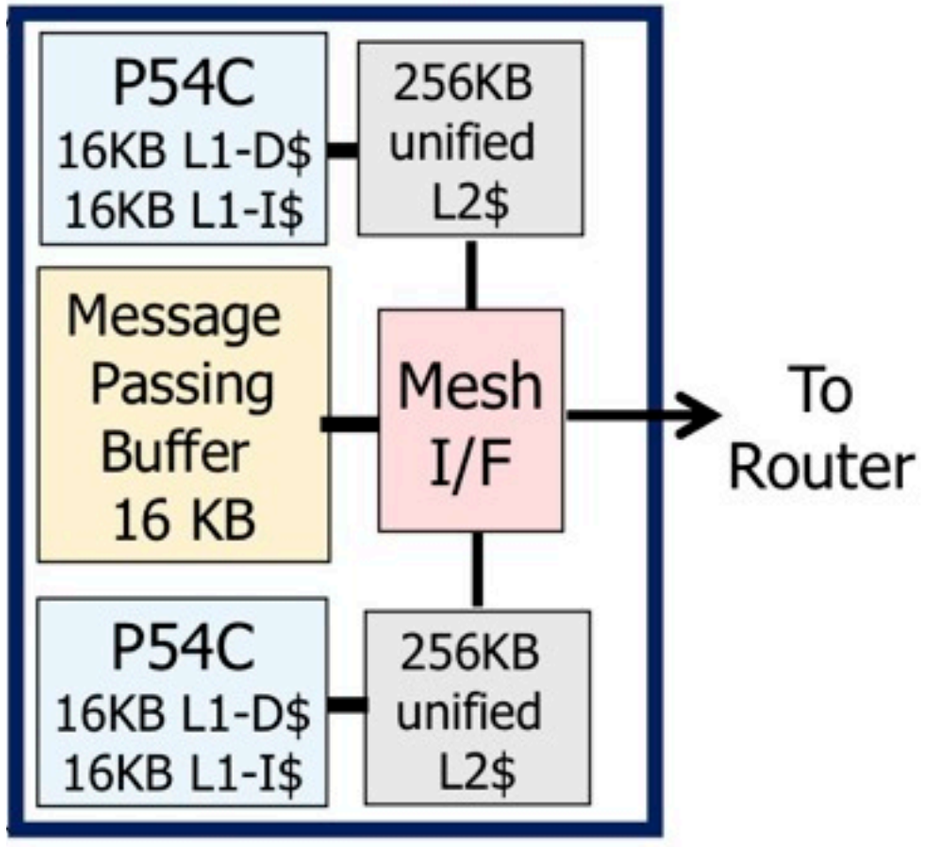

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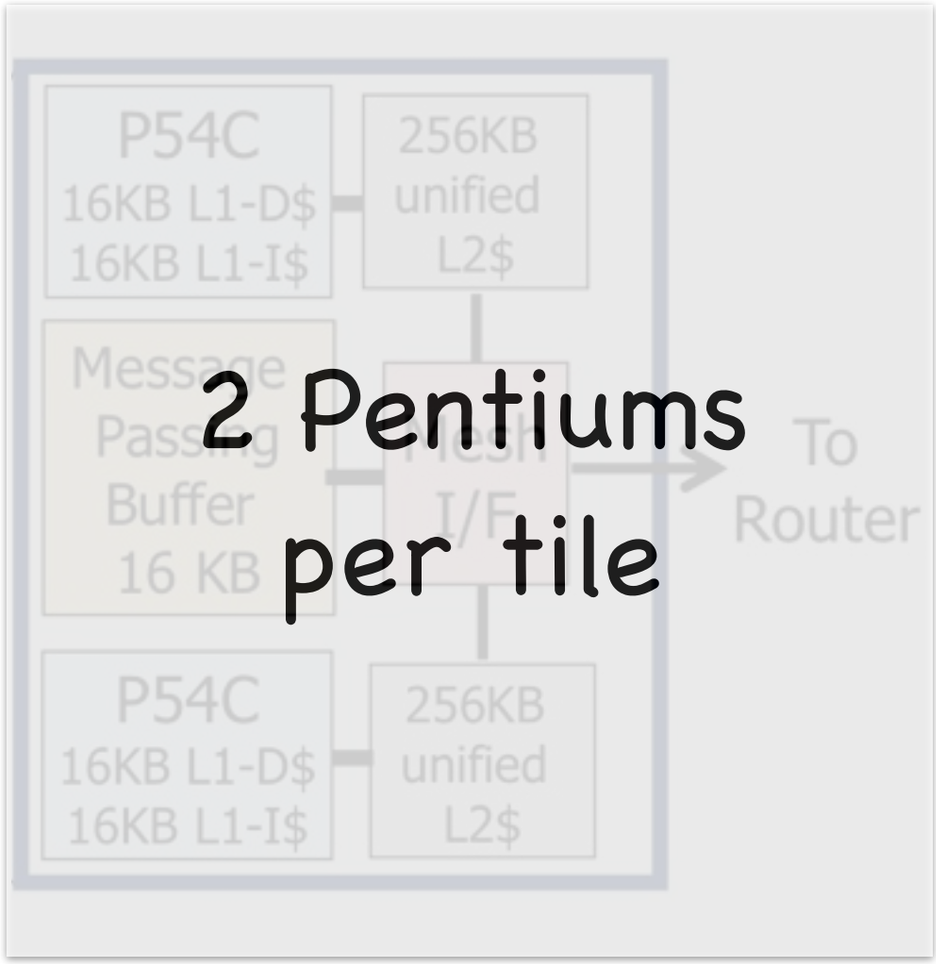

2 Pentiums per tile

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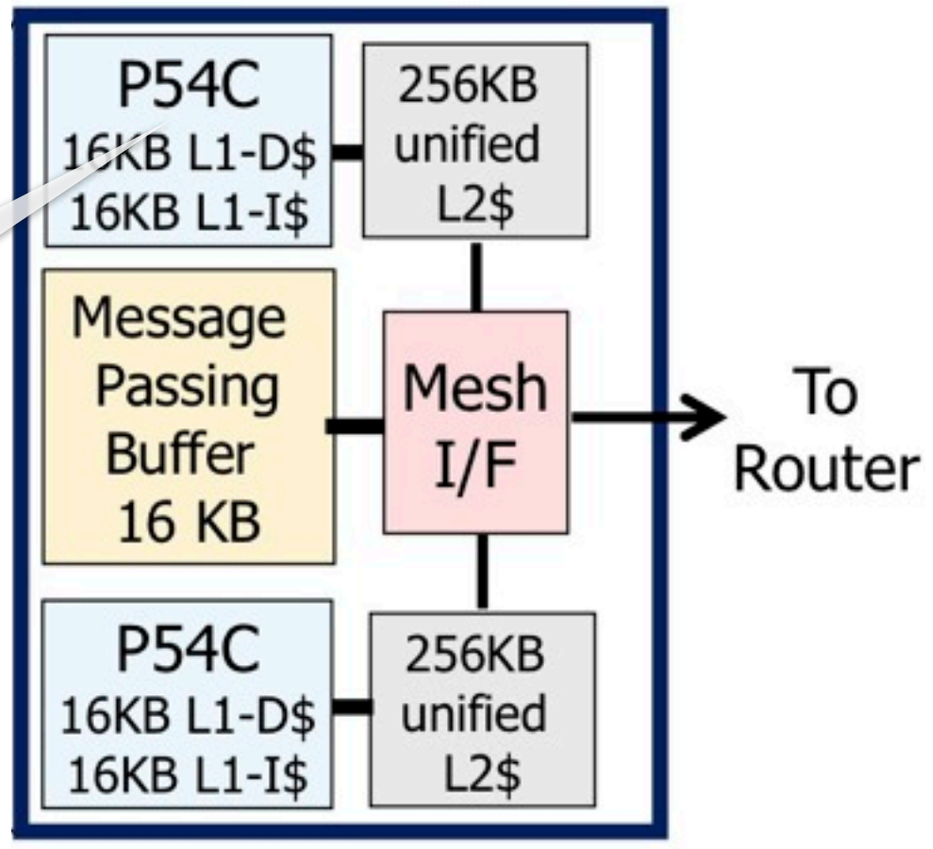
What is the SCC

16 KB L1 D$ + I$



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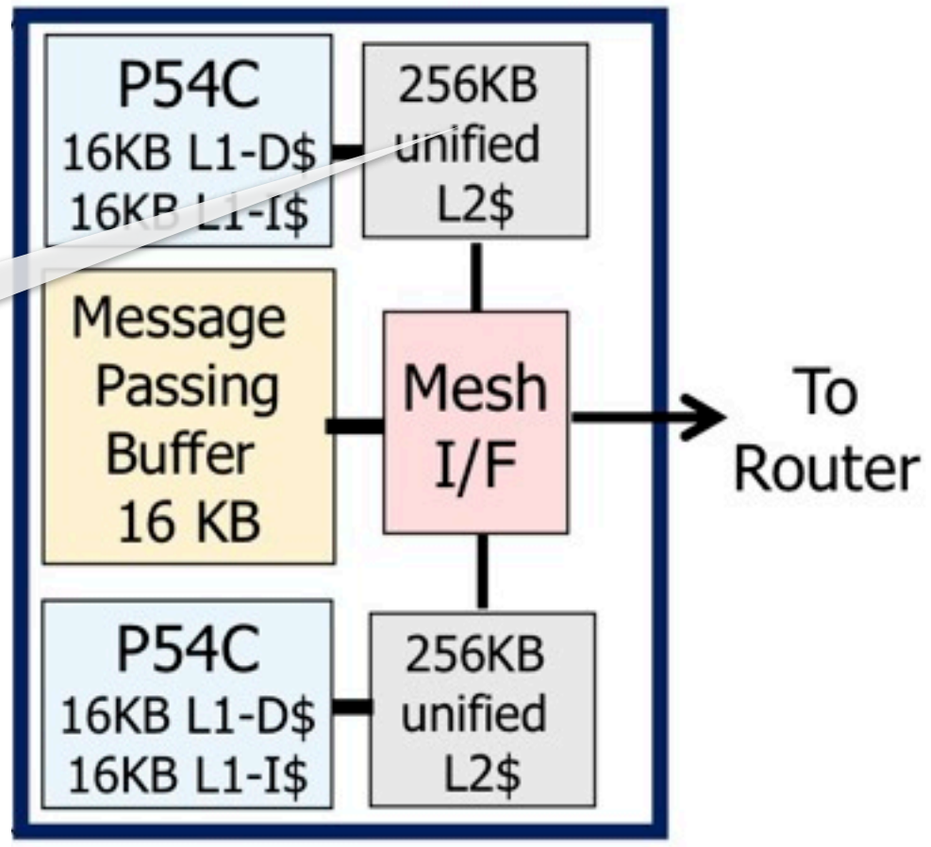
What is the SCC

256 KB L2$



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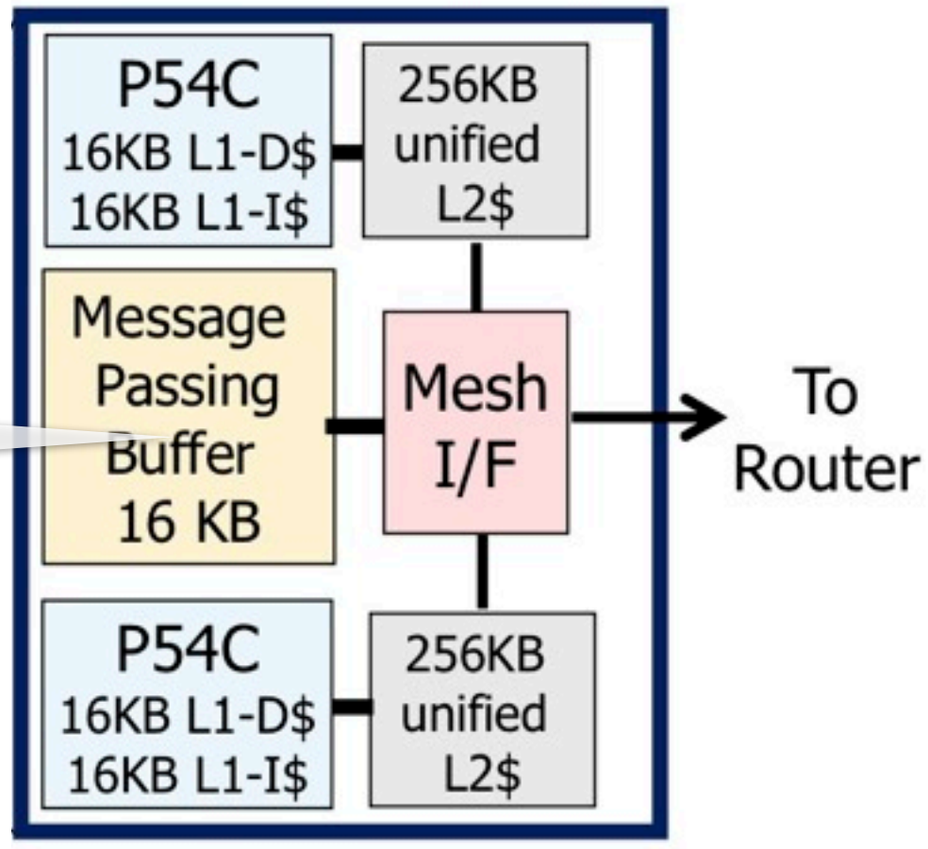
What is the SCC

16 KB message passing buffer



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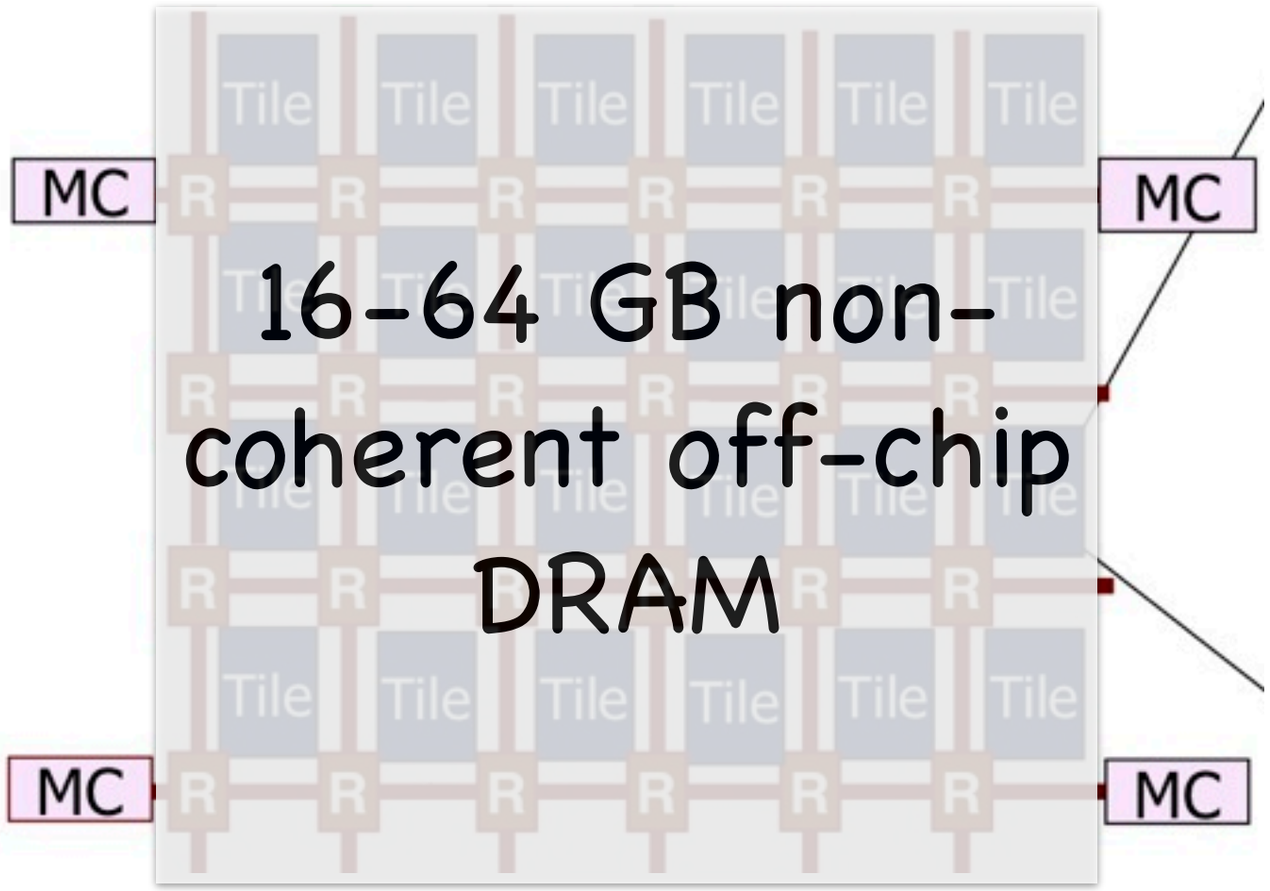
What is the SCC



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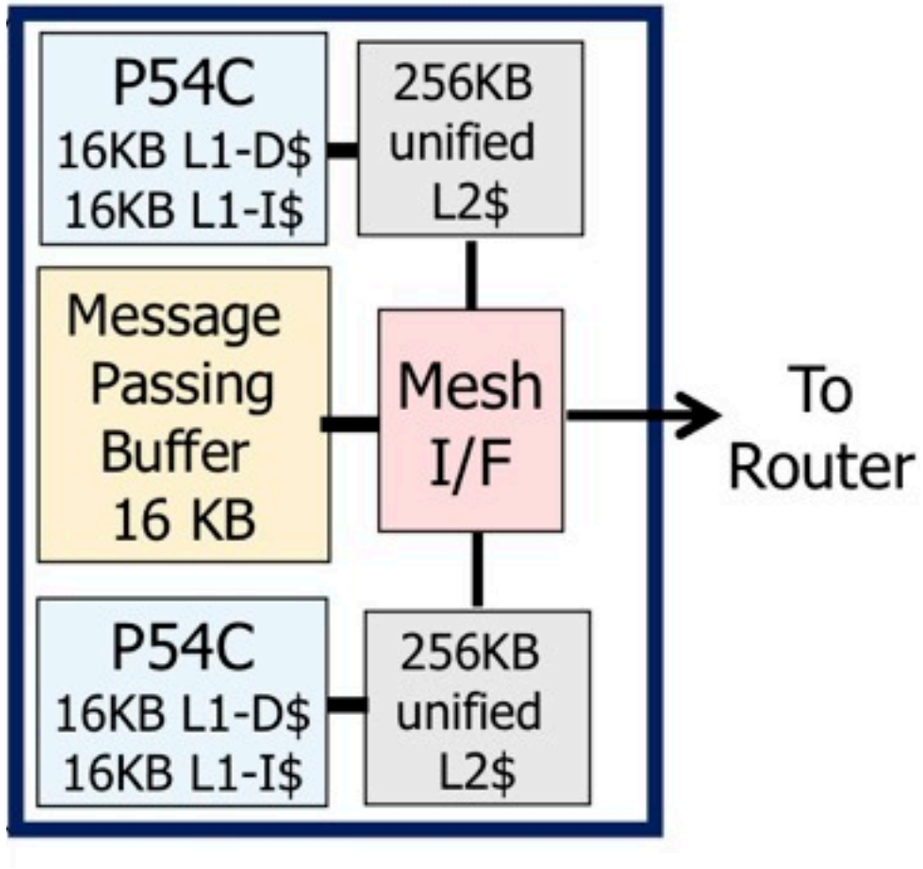
Message Passing Buffer

- Shared on-chip SRAM
- Mapped by all cores
- Cached in L1
- Tagged for fast invalidate
- 8 KB per core
- 384 KB total accessible



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RCCE native messaging

- Fast, thin layer over MPB
- One-sided *put/get* API
- RCCE flags allocatable in each MPB for coordination (one T&S register per core)
- Two-sided *send/recv* built on one-sided API using RCCE Flags

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X10 (C++) on the SCC

- Relatively straightforward
  - cross-compile using SCC tool chain
  - MPI or sockets over MPB out of the box
- What about RCCE?

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X10RT API

- Used by X10 runtime to communicate between *places*
- Send serialized object graphs
- Registered receiver callbacks for different types of message
- Probe occasionally for incoming messages
- Don't block waiting for messages to arrive

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X10RT + MPI + SCC

- X10RT with MPI binding
- SCC MPI library with alternative channels
  - mpi-mpb: direct MPB
  - mpi-sock: sockets via mesh TCP/IP driver
  - mpi-shm: shared memory

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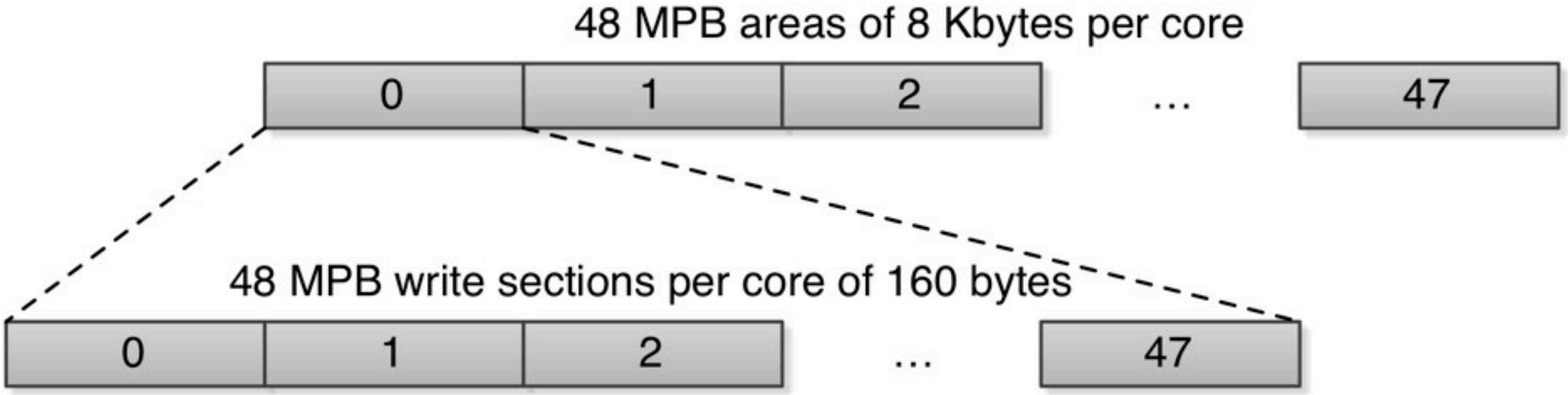
mpi-mpb MPB management



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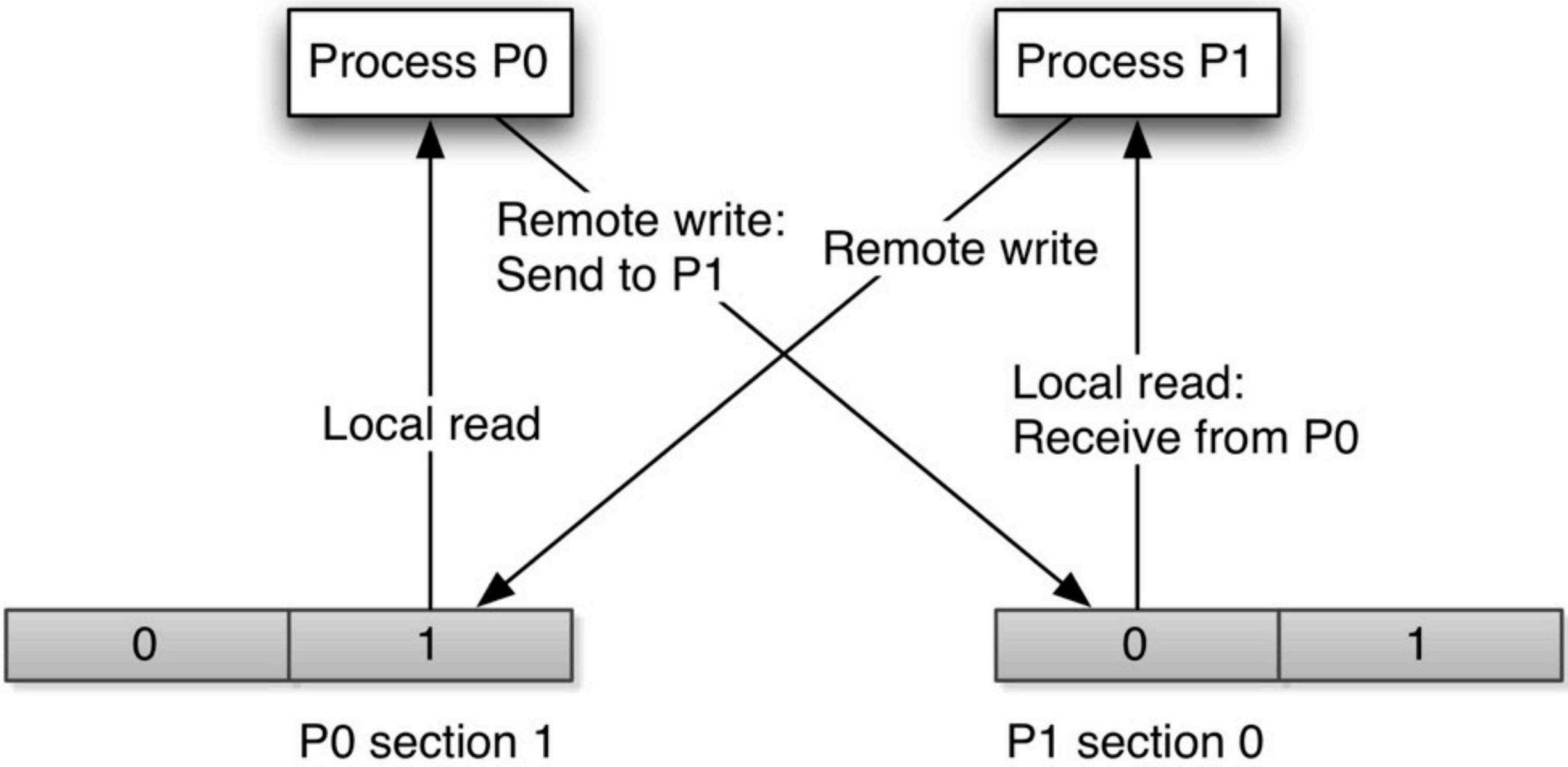
mpi-mpb send/receive



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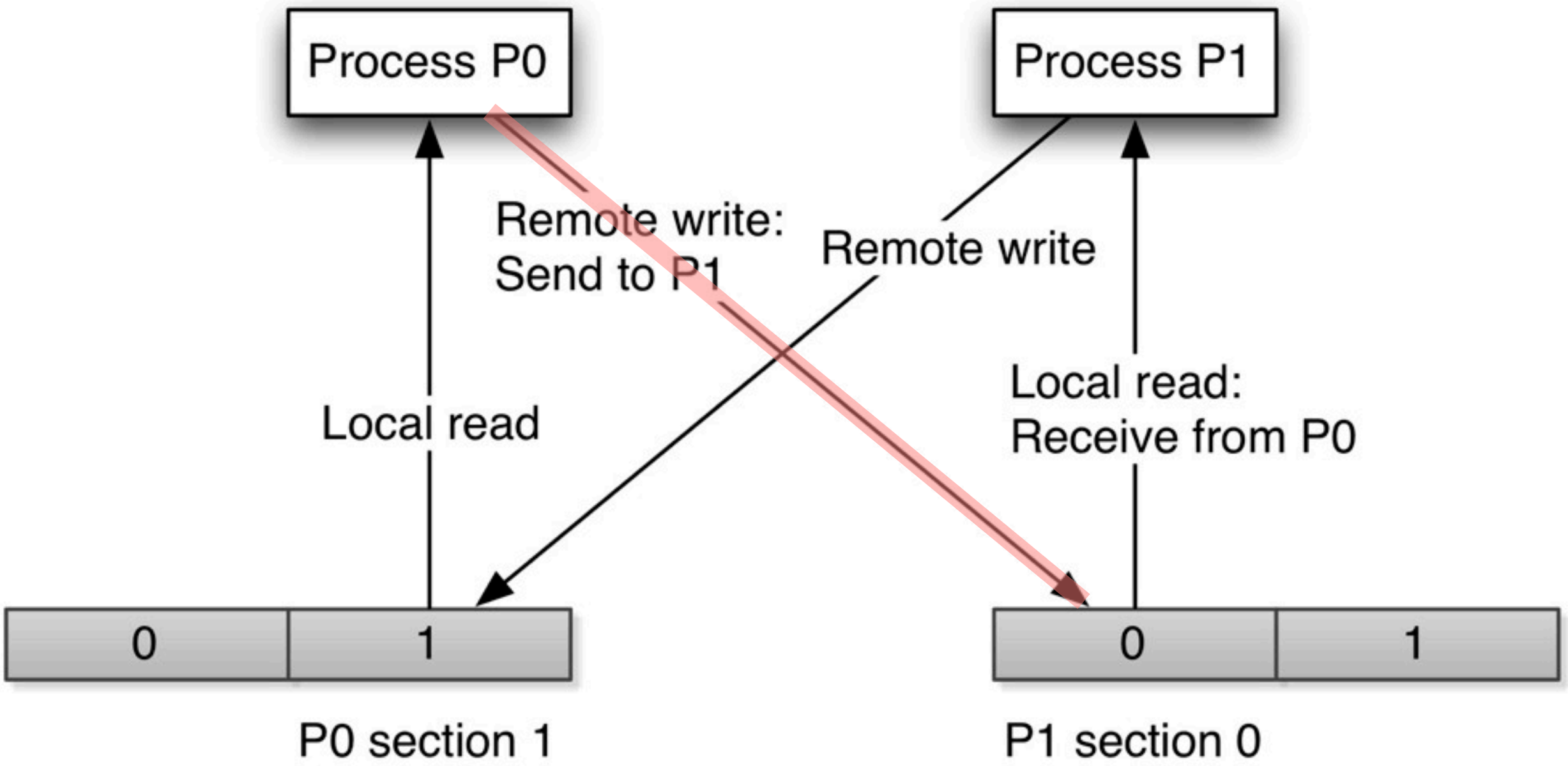

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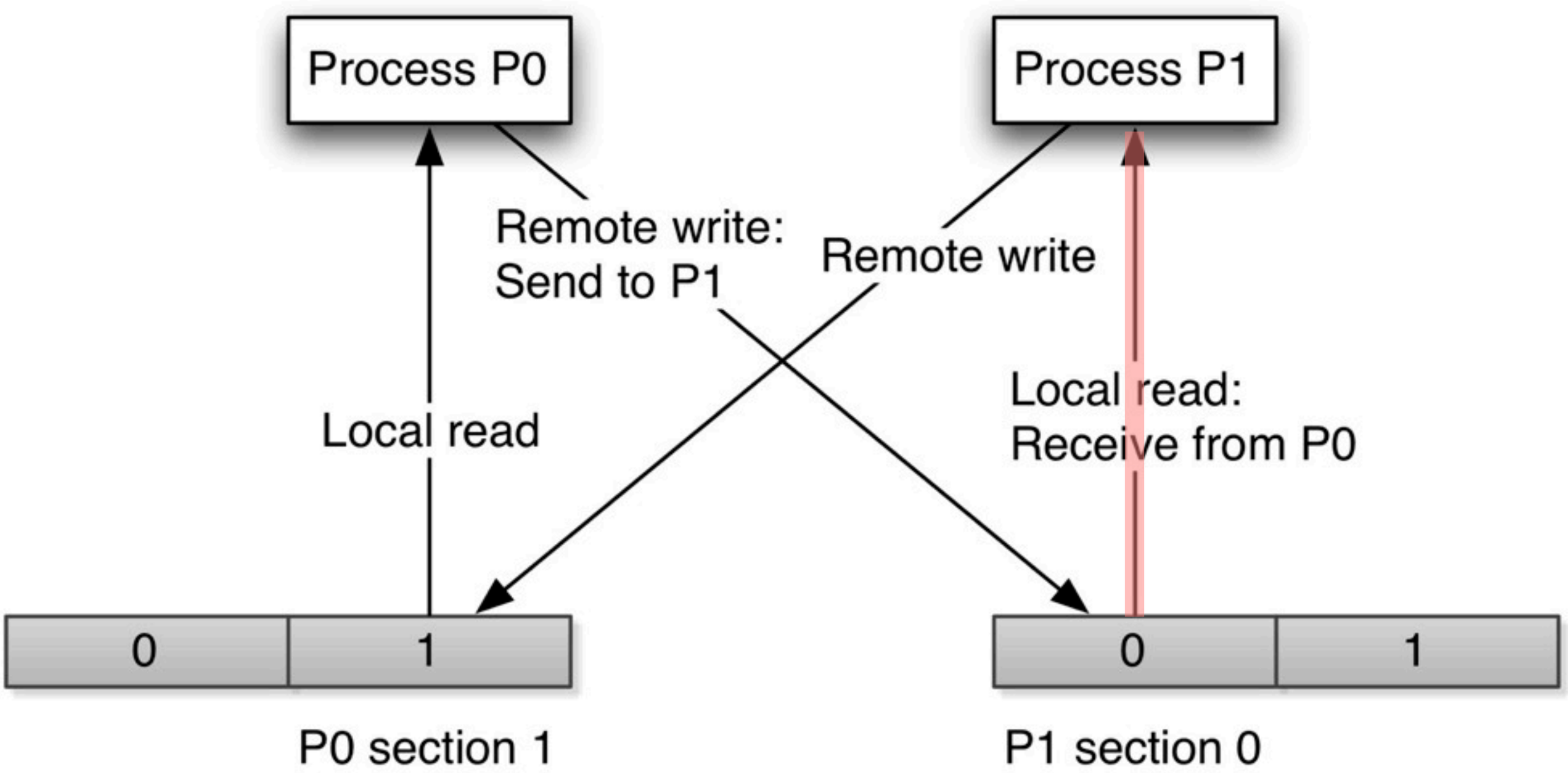

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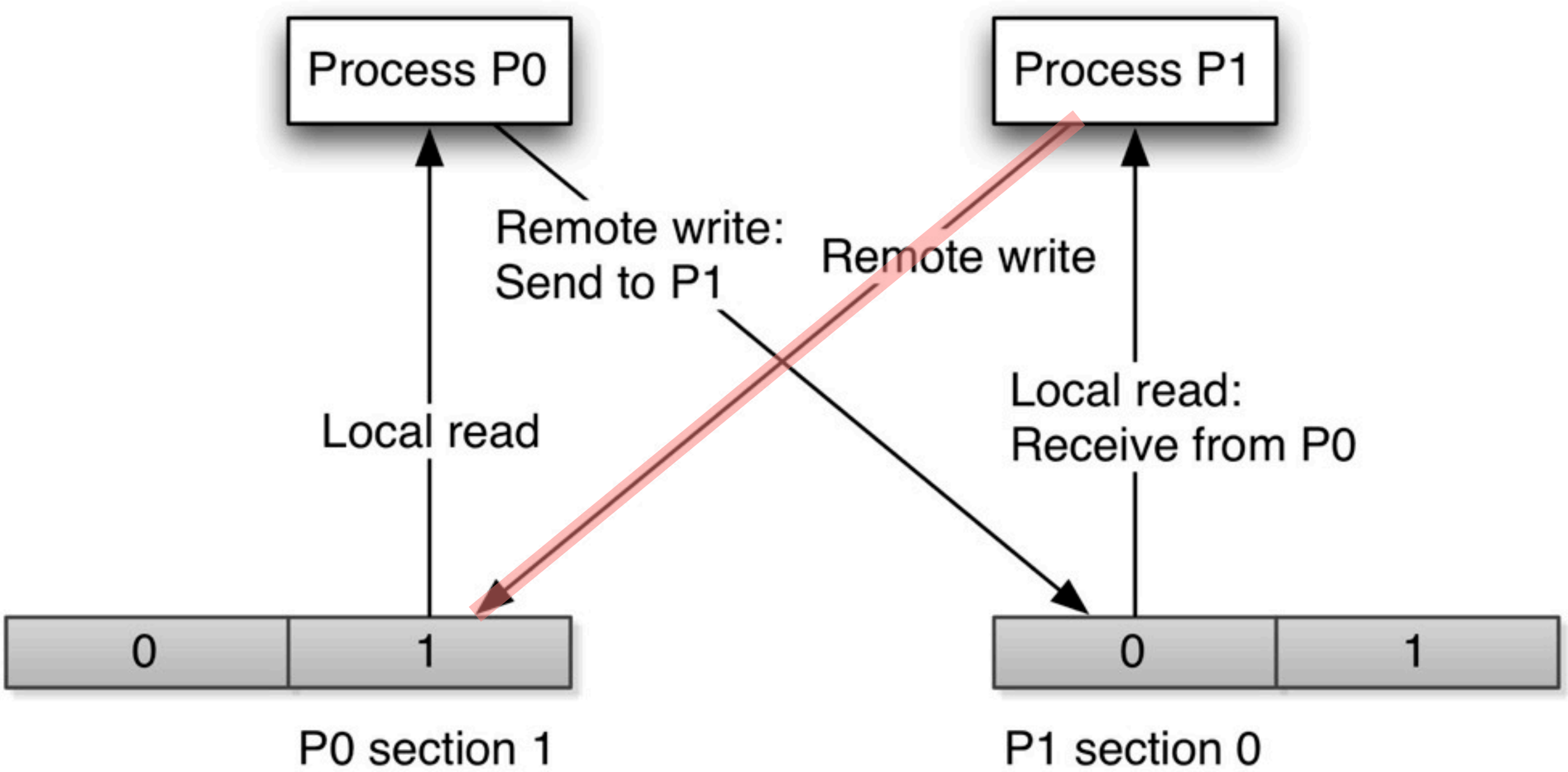

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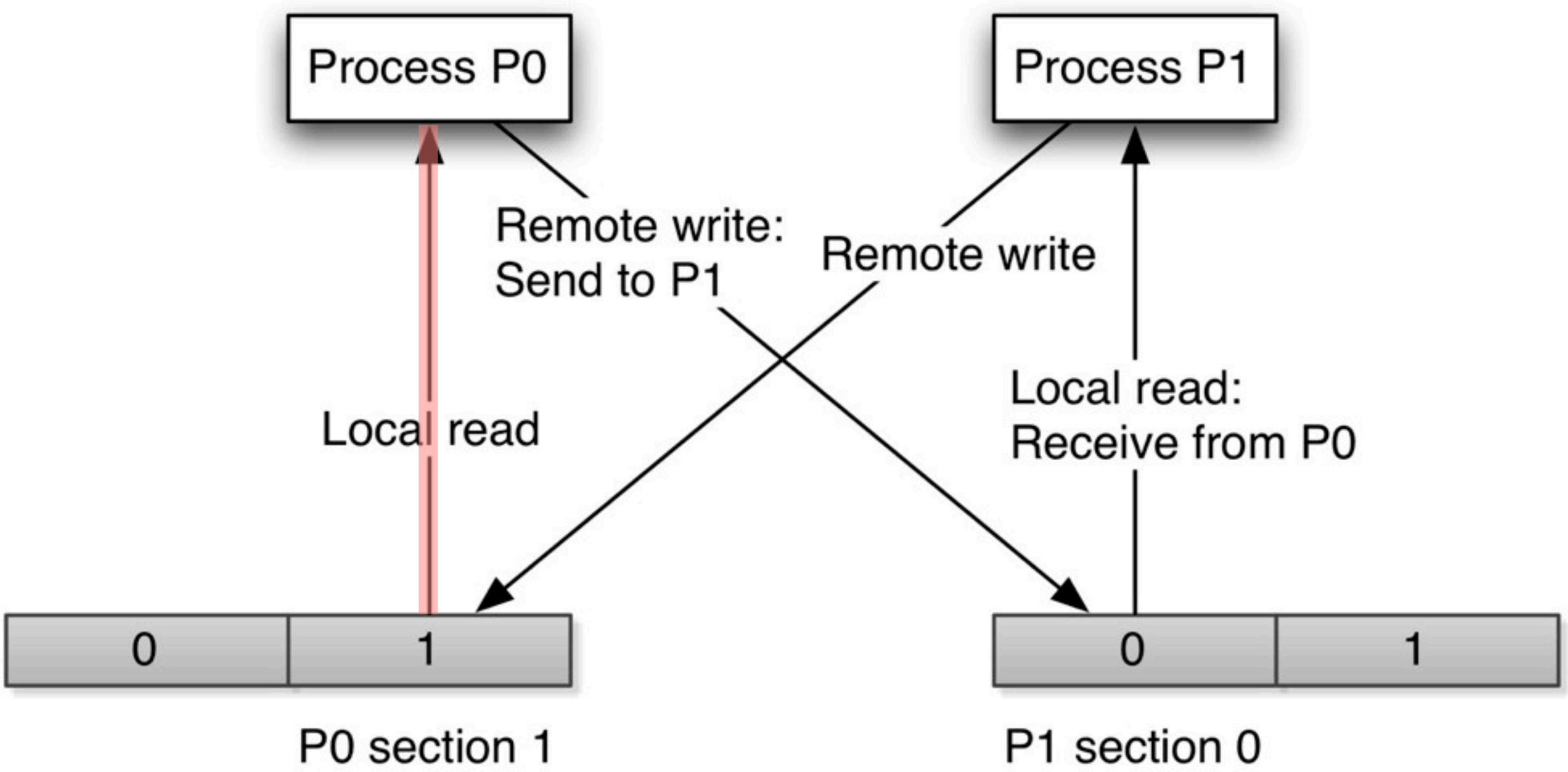

X10RT+"RCCE"+SCC

- RCCE send/recv are blocking
- RCCE non-blocking recv_test requires knowing sender to test
- RCCE does not support X10RT tags

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X10RT+"RCCE"+SCC

- Re-implement as RCCE-X10
  - one-sided non-blocking send
  - non-blocking probe

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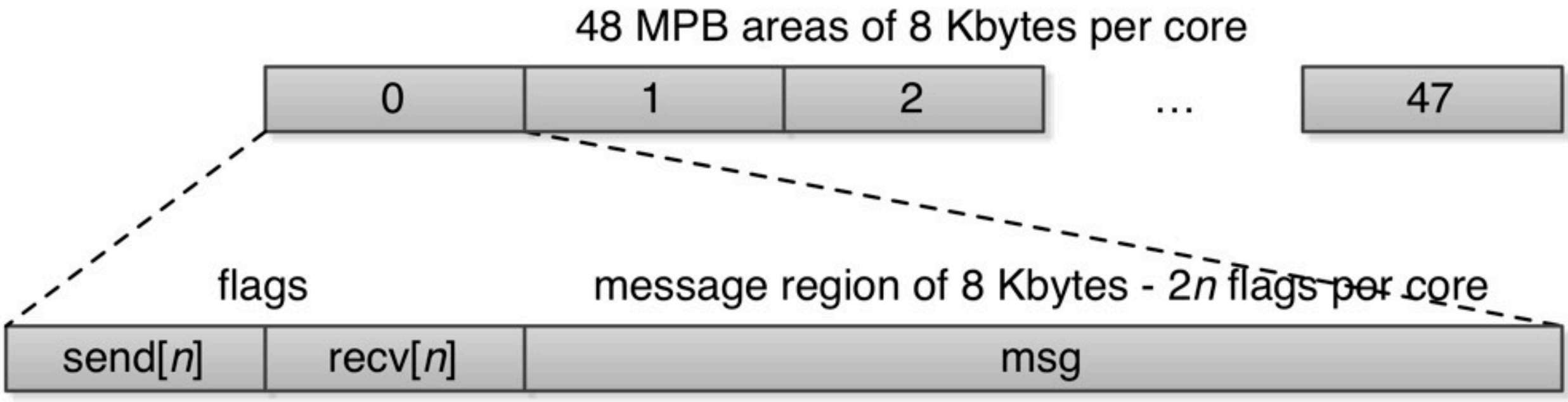
RCCE-X10 MPB Management



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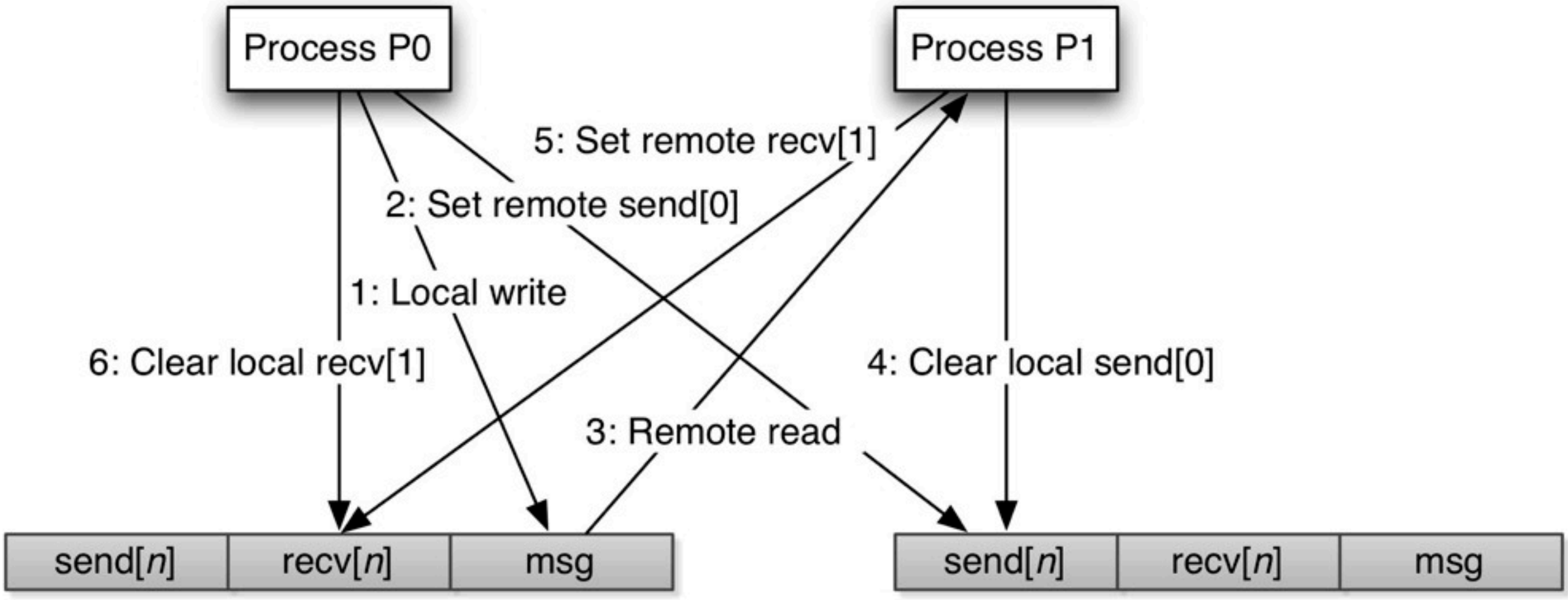
RCCE-X10 send/ receive



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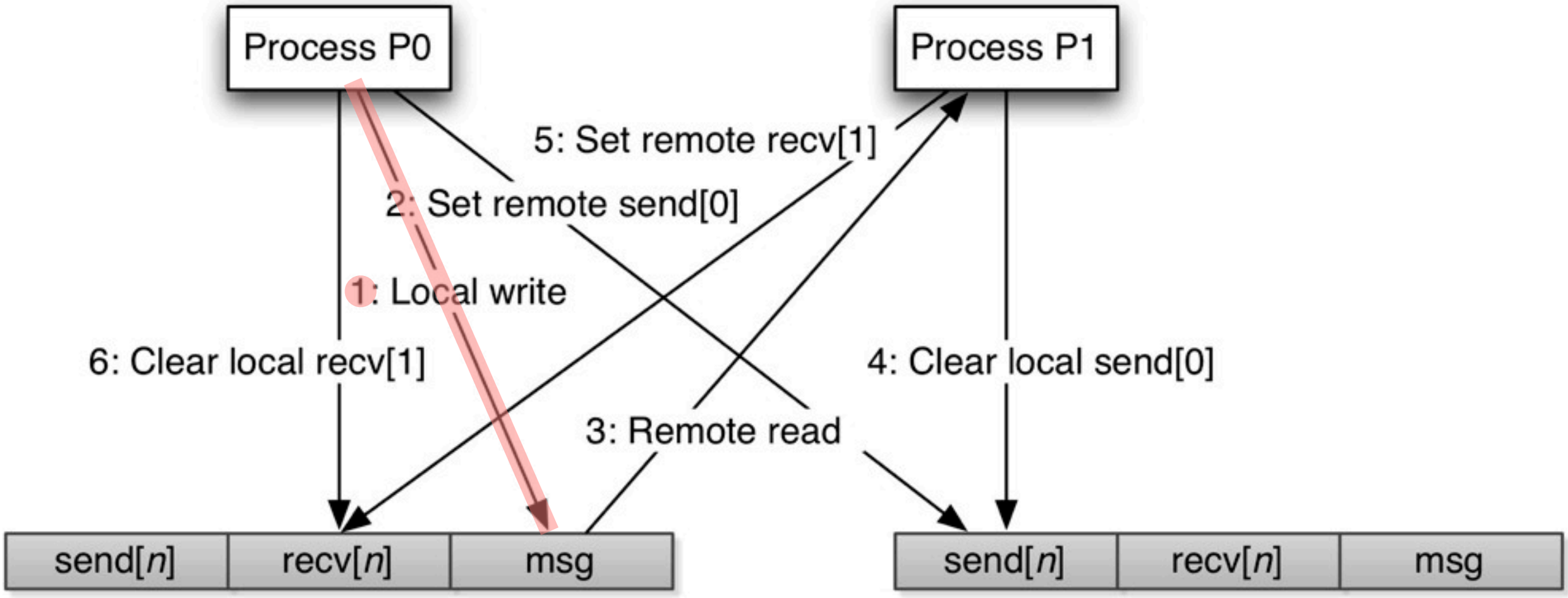

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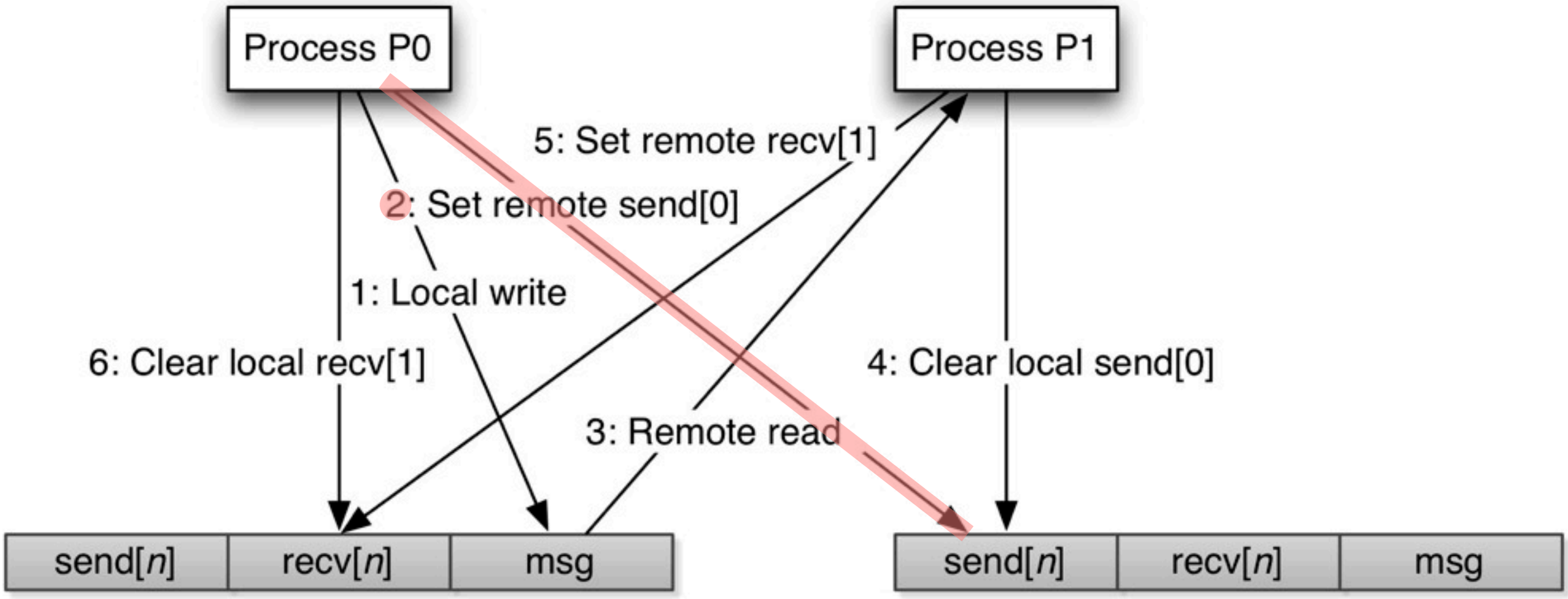

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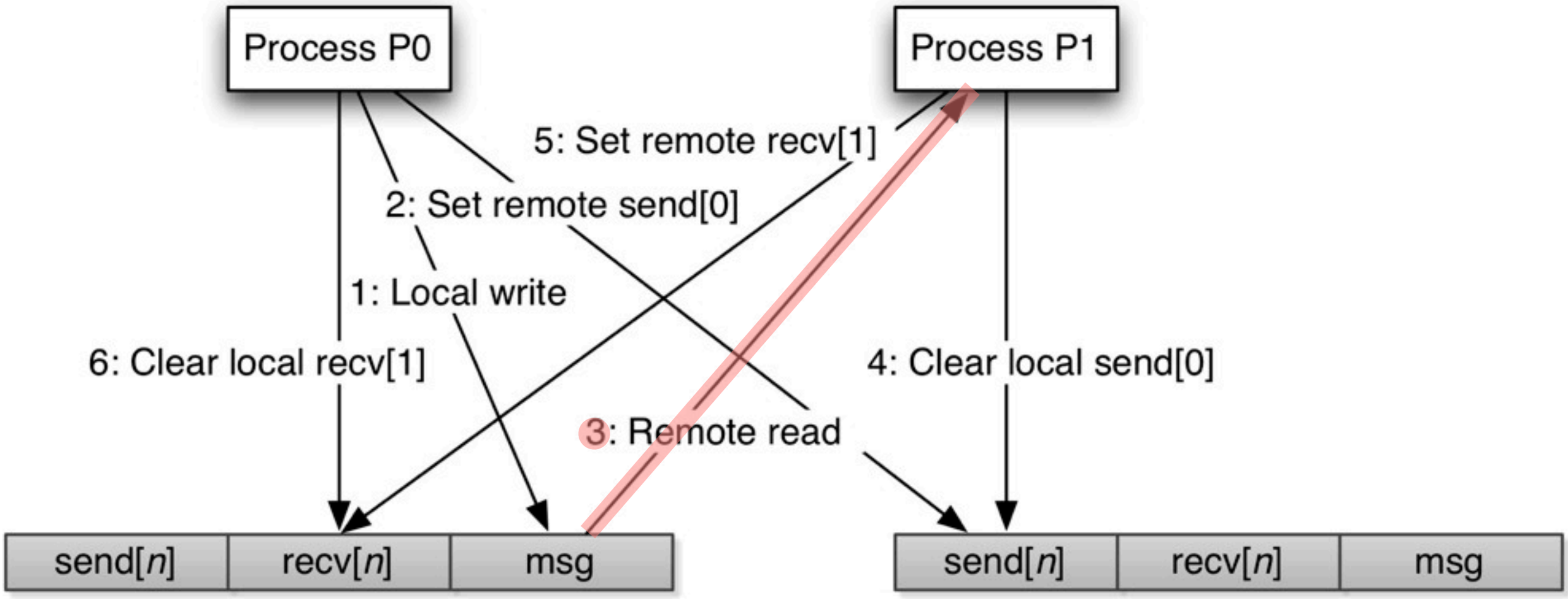

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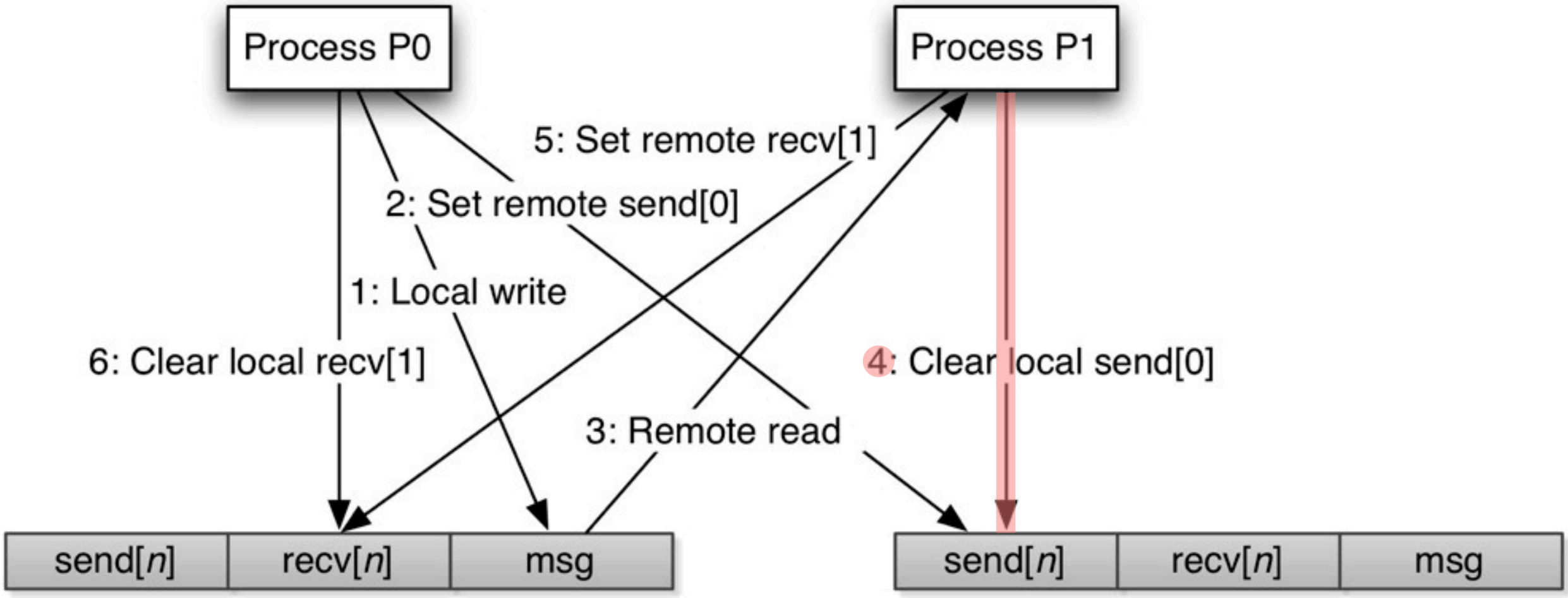

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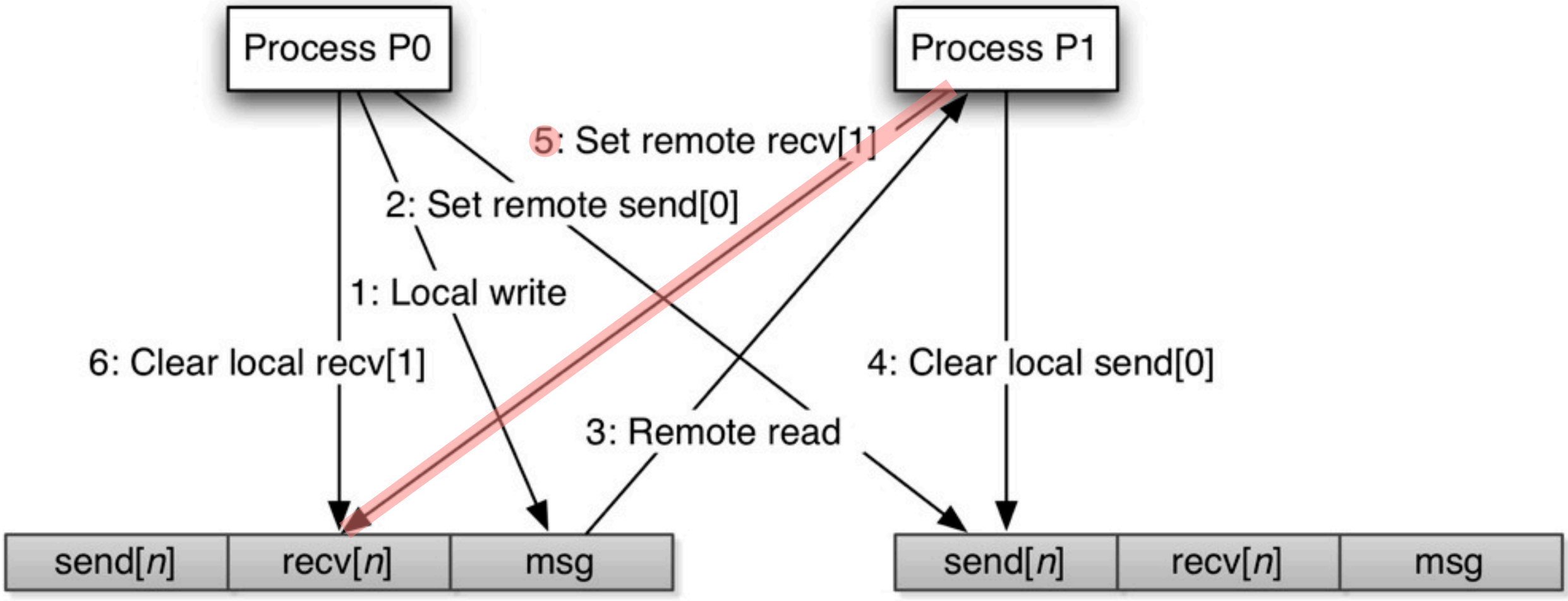

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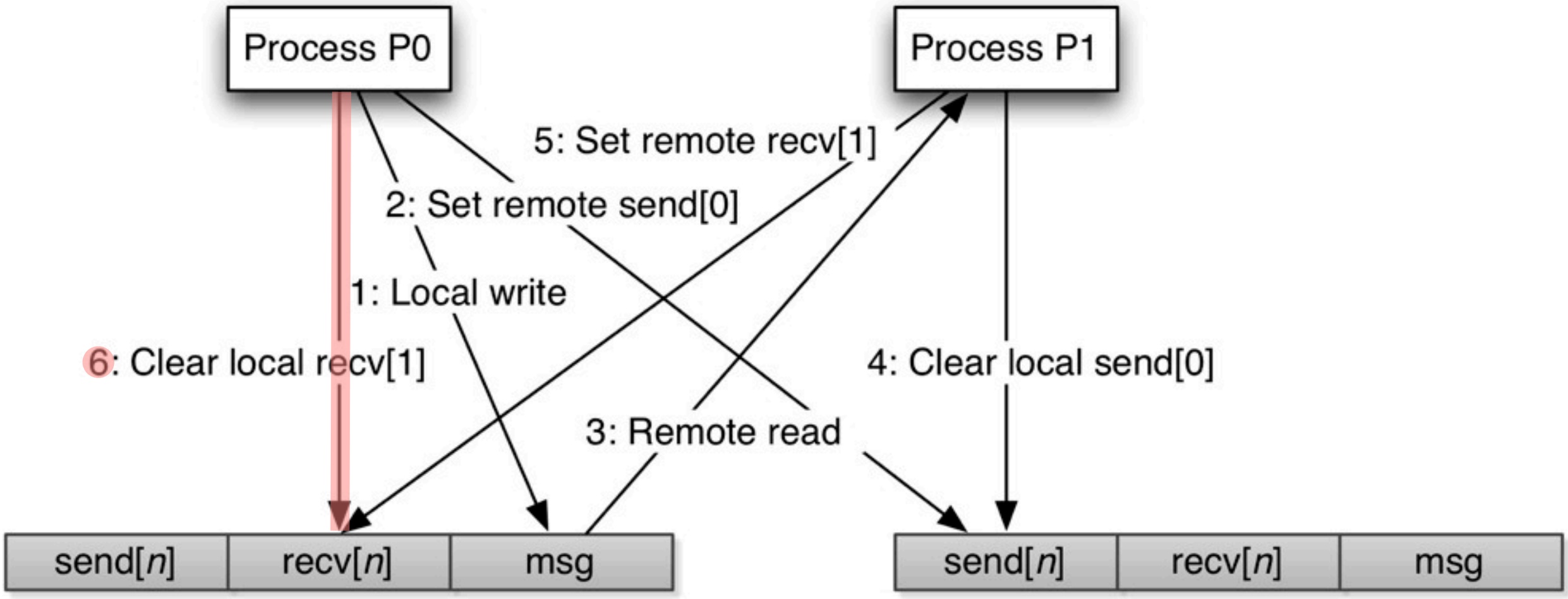

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Experiments

- One place per SCC core
- One worker thread per place
- Results in paper without GC
- 322 MB private memory per core
- 2 benchmarks: ANUChem-HF and BC
- X10 post-2.1.1 trunk dated January 13th

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Benchmarks

- ANUChem Hartree-Fock (HF) quantum chemistry benchmark
  - Benzene STO-3G workload (in paper)
  - Benzene 3-21G with GC
- Betweenness Centrality (BC) social network actor centrality benchmark
  - Dijkstra's shortest path algorithm
  - small, medium, large workloads

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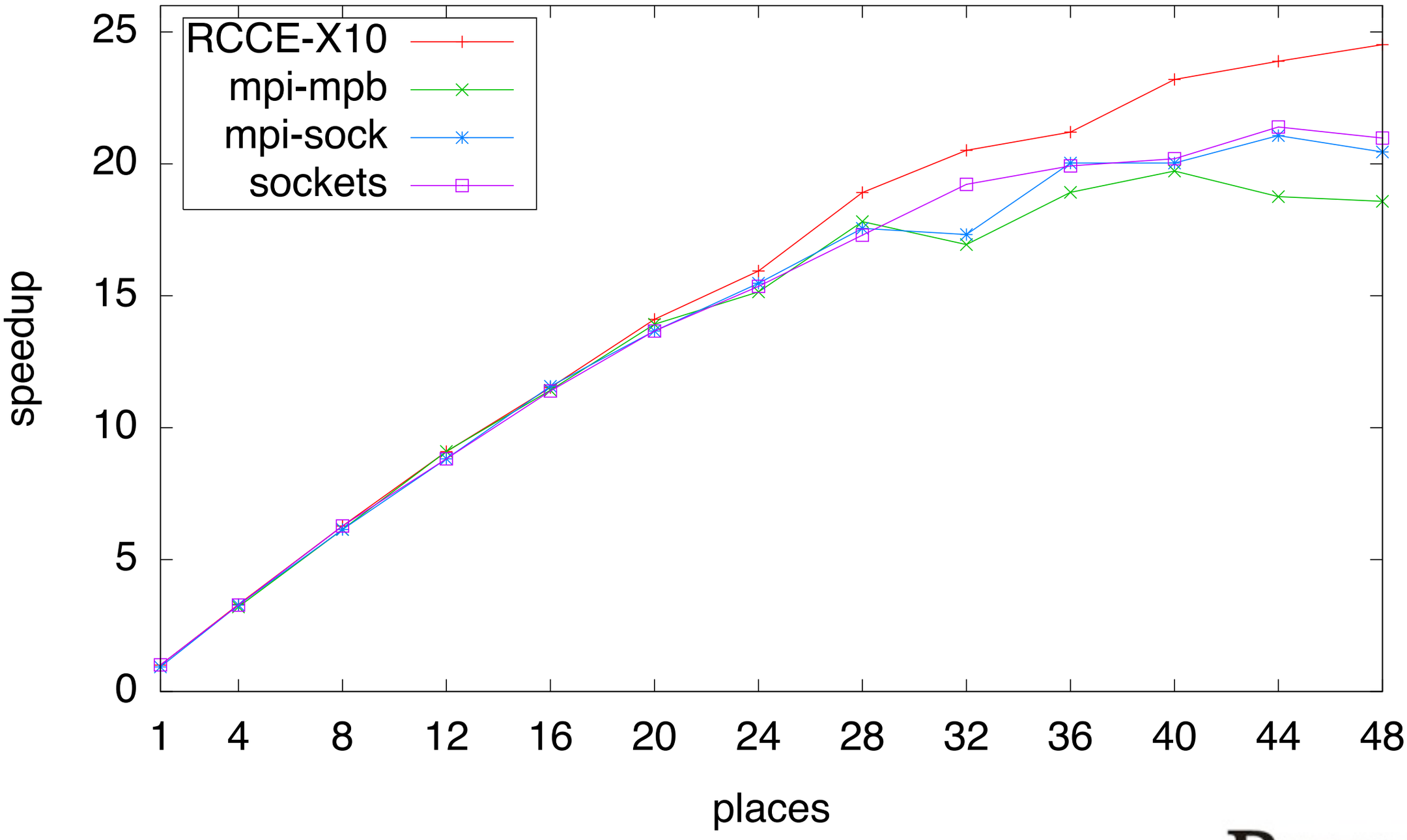
BC large workload



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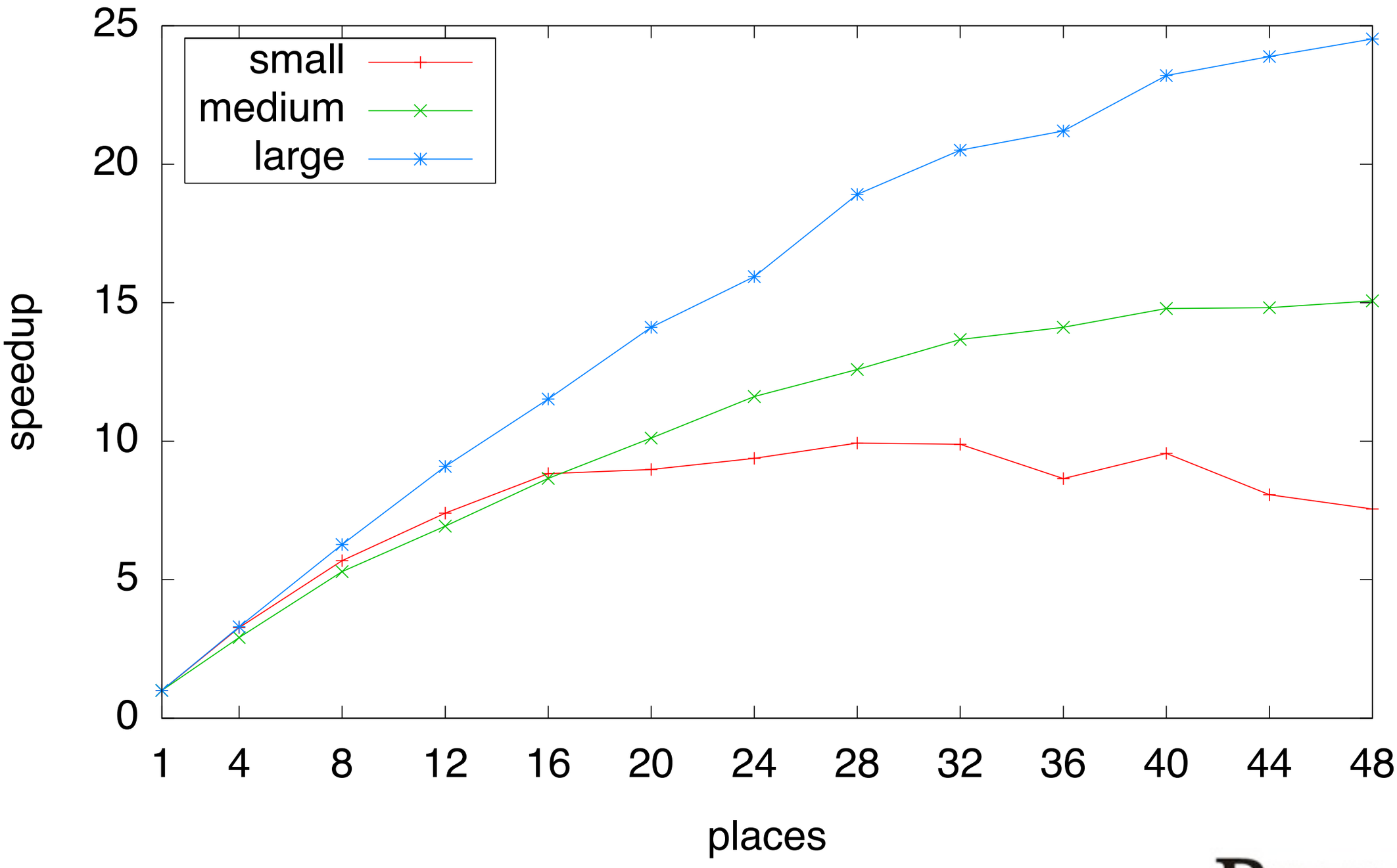
BC varying workload



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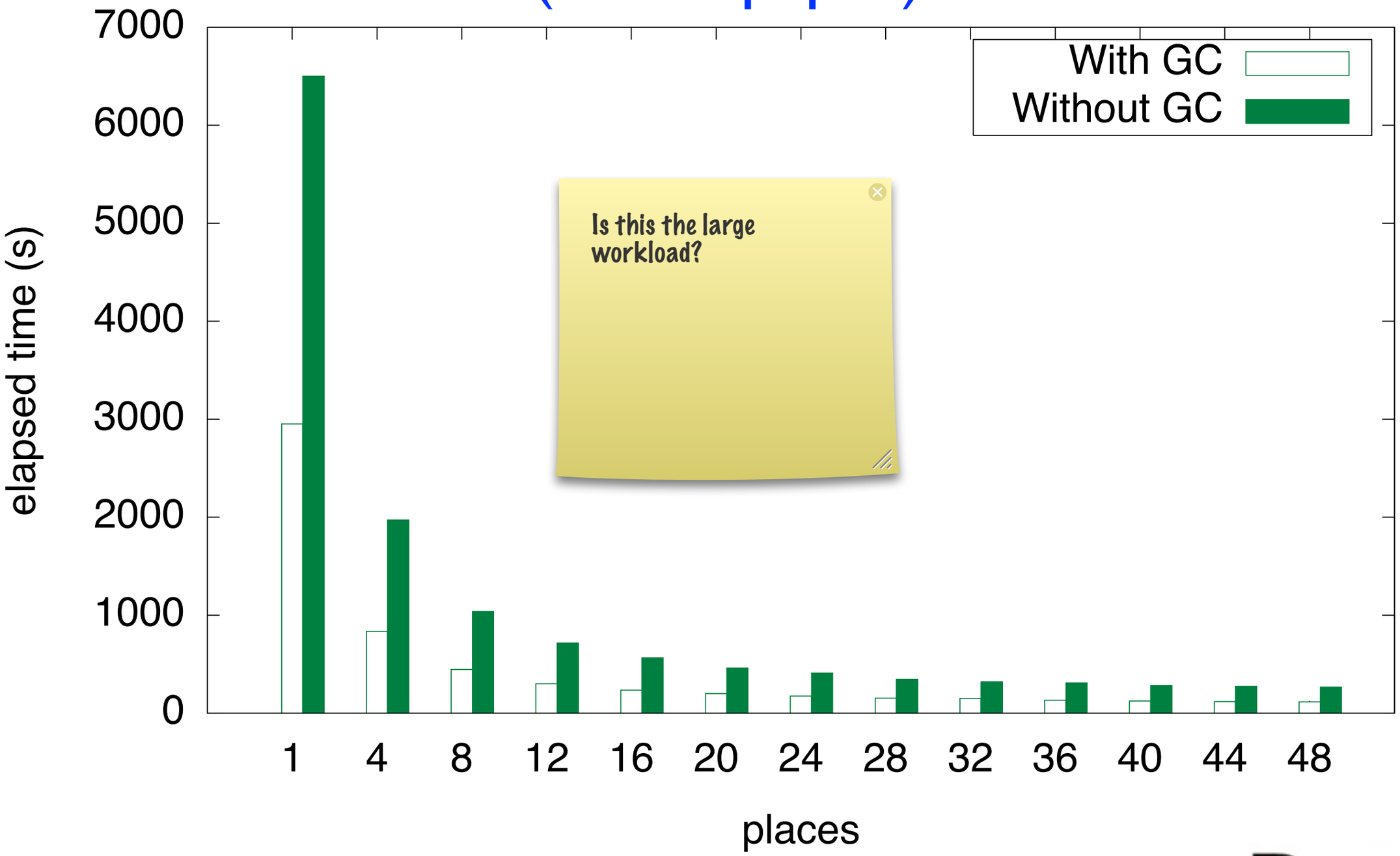
BC with RCCE-X10

(not in paper)



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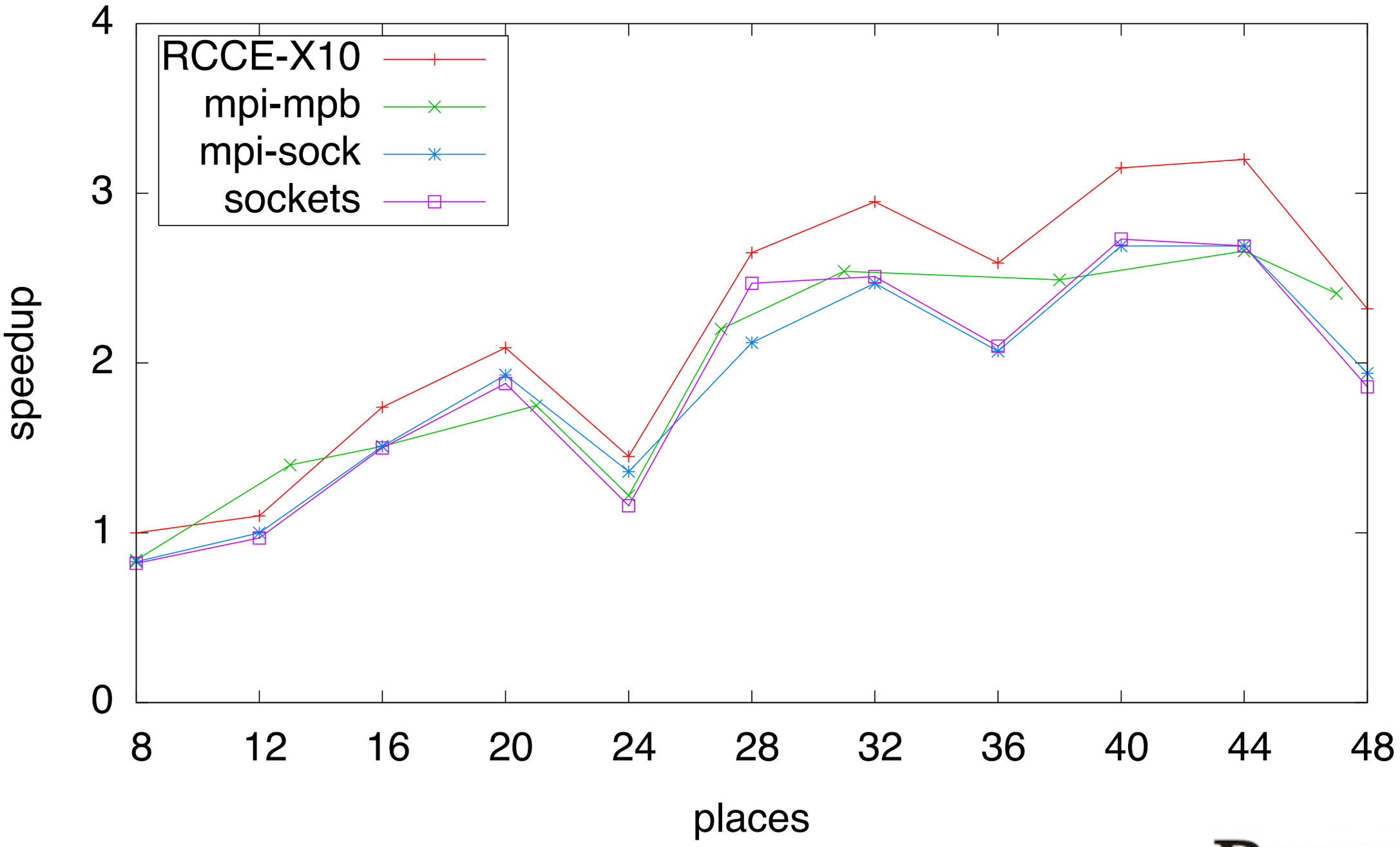
HF static balancing



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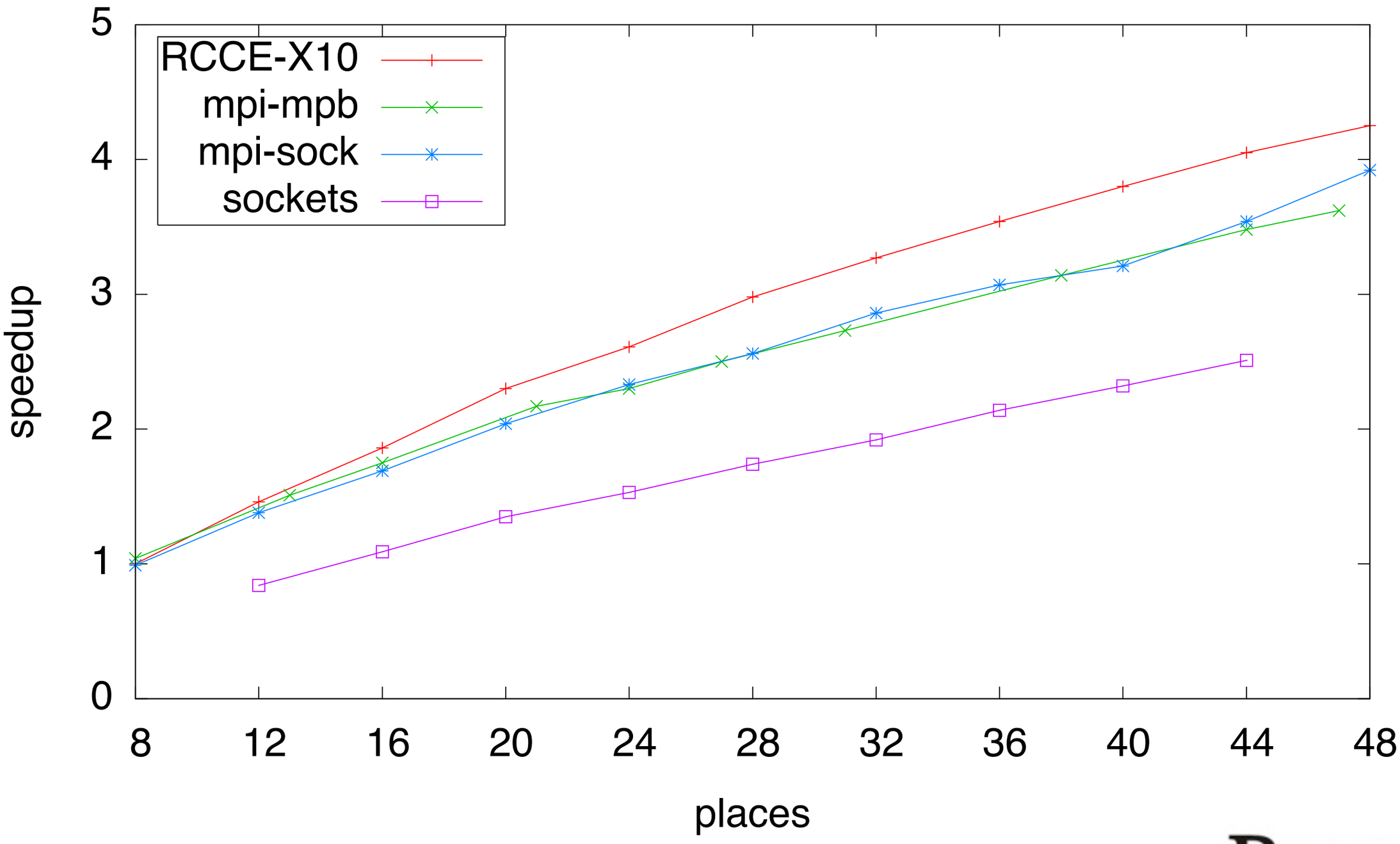

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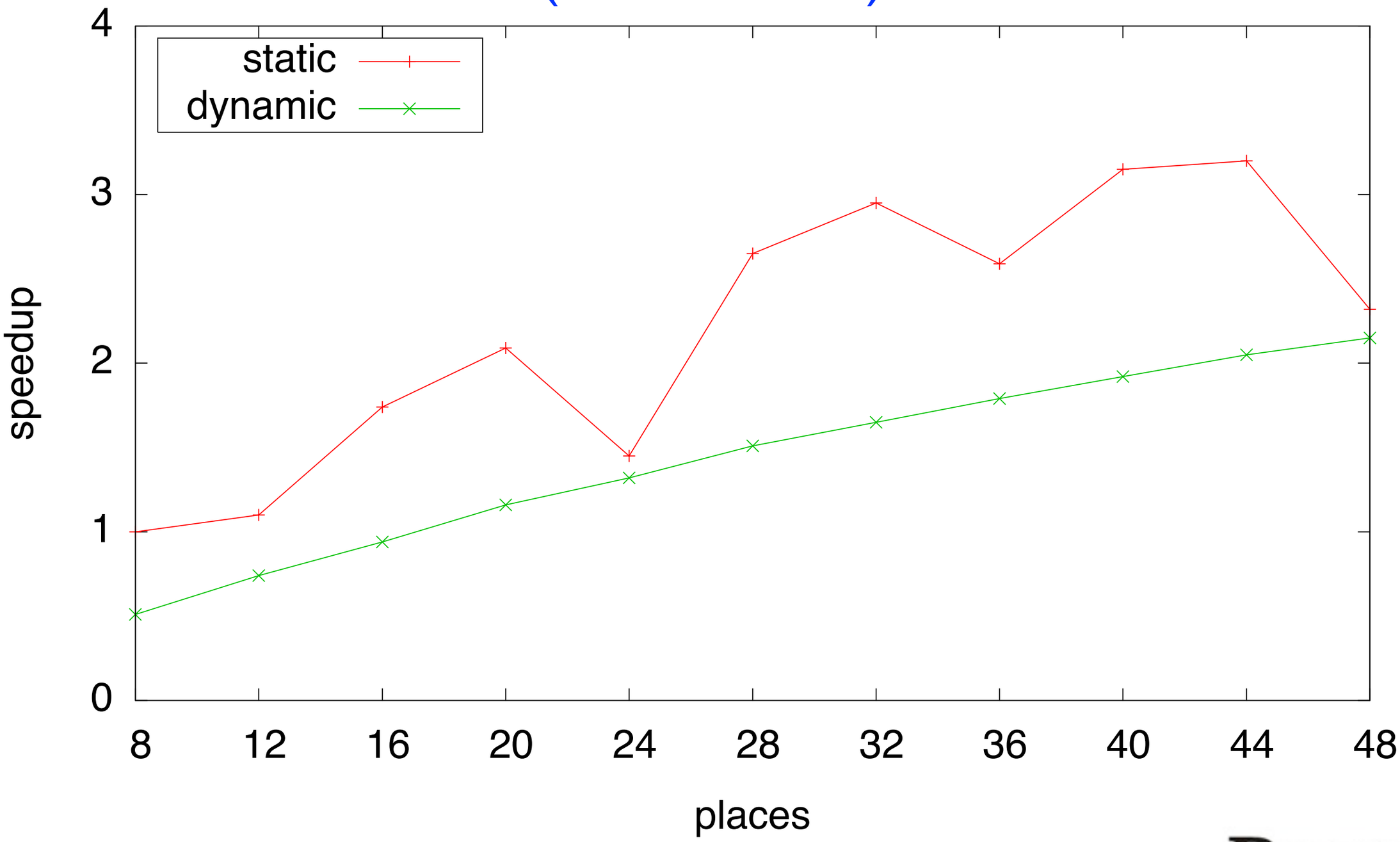
HF dynamic vs static

(RCCE-X10)



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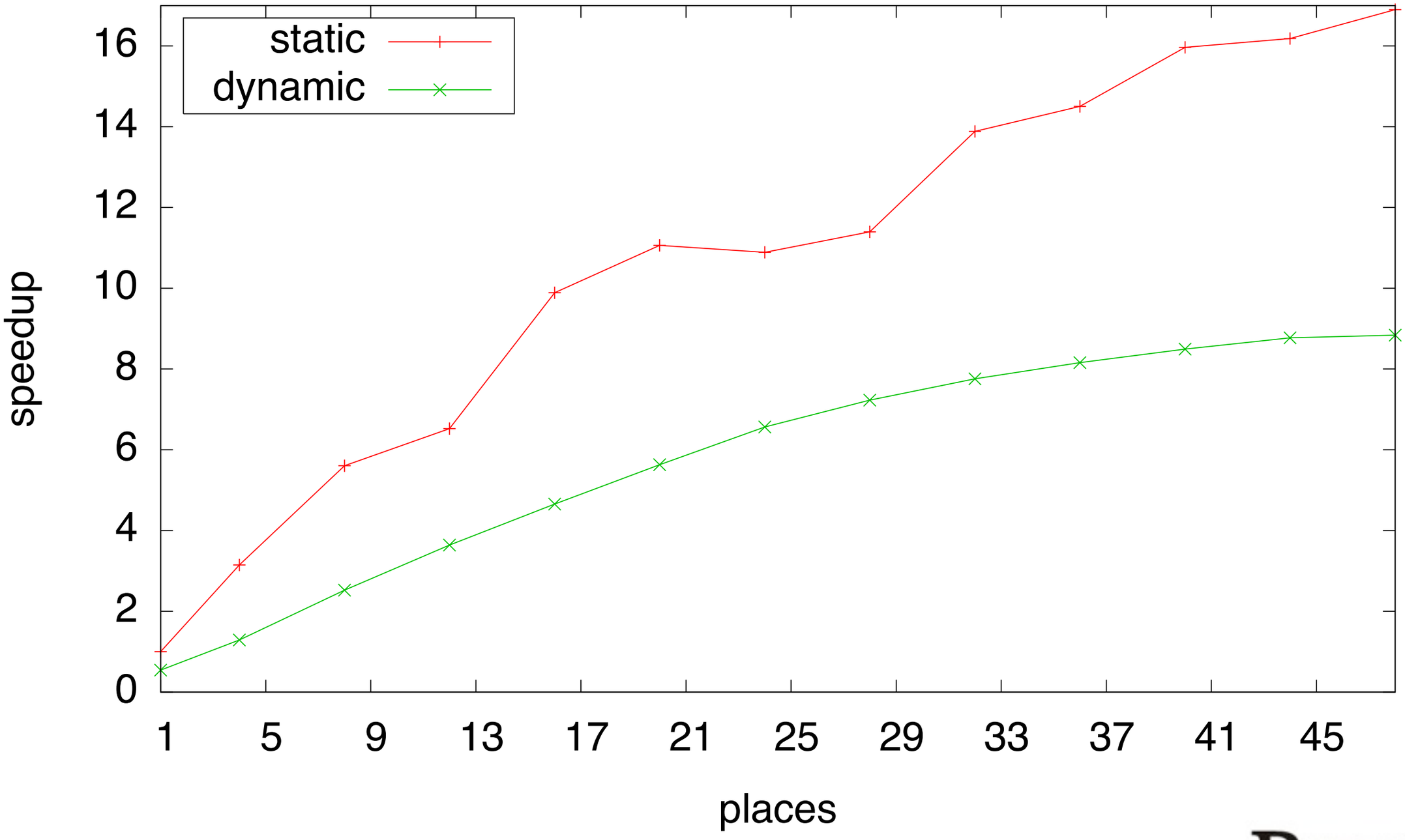
HF with GC

(not in paper)



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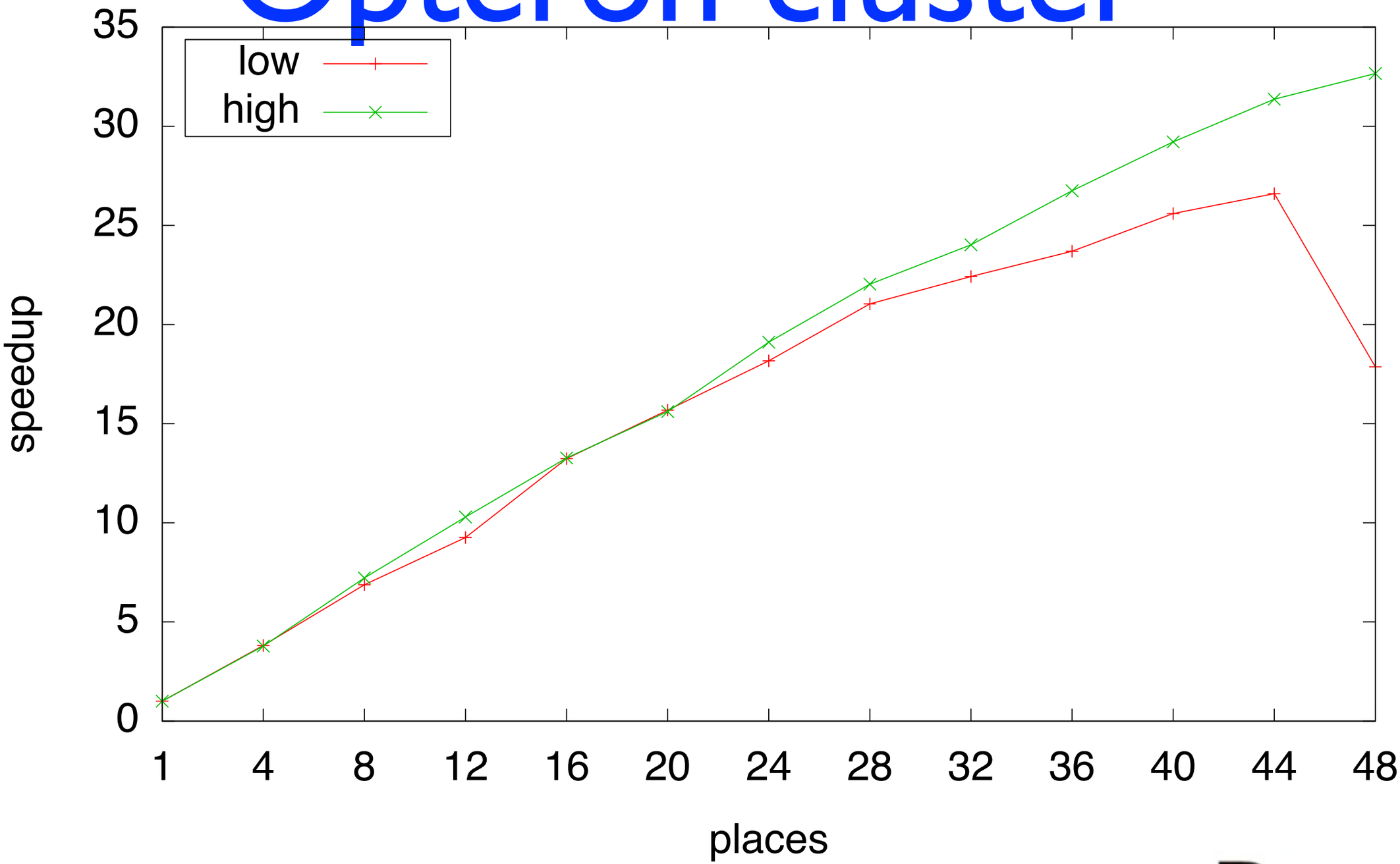
BC with MPI on 3x8x2 Opteron cluster



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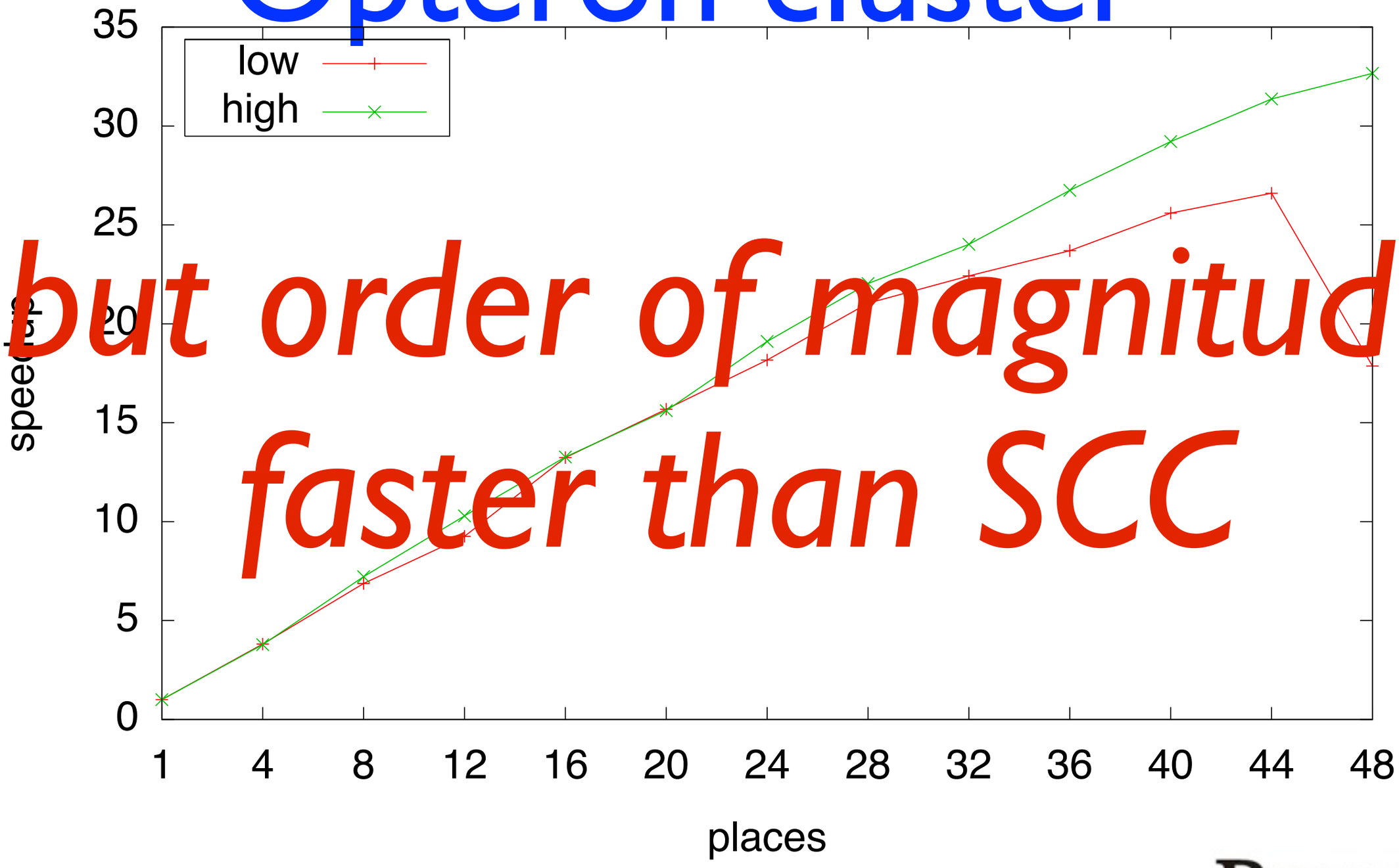

but order of magnitude faster than SCC

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Conclusions

- SCC memory constraints are limiting:
  - tradeoff work vs memory to get scaling
  - running with GC allows larger workloads (and better performance!)
- But, X10 + SCC is a nice match
- X10 benchmarks (can) show good scaling
  - order of magnitude slower than cluster

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