

Microcontroller programs

1) Designing an ALU to perform block data transfer

1) Generating Series 5, 10, 15, 20, 25

Area Example, Code, Readonly

```
ENTRY
MOV R4, #5
MOV R0, #1
MOV R1, #2
MOV R2, #3
MOV R3, #0
LOOP MLA R3, R0, R1, R2
ADD R6, R3
SUBS R4, #1
BNE LOOP
L B L
END
```

2) Generating Series 2, 4, 6, 8, 10

Area Example, Code, Readonly

```
ENTRY
MOV R4, #5
MOV R0, #1
MOV R1, #1
MOV R2, #2
MOV R5, #1
MOV R6, #0
LOOP MLA R3, R0, R1, R2
ADD R6, R3
SUBS R4, #1
BNE LOOP
L B L
END
```

3) Generating Odd numbers

Area Example, Code, Readonly

```
ENTRY
MOV R4, #5
MOV R0, #1
MOV R1, #1
MOV R2, #1
MOV R6, #1
LOOP MLA R3, R0, R1, R2
ADD R6, R3
SUBS R4, #1
BNE LOOP
L B L
END
```

4) Generating factorial of a number

Area FACT, CODE, READONLY

START

```
MOV R0, #5
MOV R1, #01
MOV CMP R0, #0
BEQ STOP
MOV R1, R0
NEXT SUBS R0, #1
CMP R0, #0
BEQ STOP
MUL R2, R1, R0
MOV R1, R2
B NEXT
STOP
NOP
END
```

5) ALP Program to find largest number in an array.

AREA LARGEST, CODE, READONLY

ENTRY

ORG 0000

MOV R0, #30H

MOV R1, #05H

MOV B, #00H

BACK: MOV A, @R0

CJNE A, B, LOOP

LOOP: JC LOOP

MOV B, A

LOOP: INC R0

DJNZ R1, BACK

SJMP \$

END

AREA LARGEST, CODE, READONLY

ENTRY

LDR R0, =VALUE1

LDR R5, [R0], #4

SUBS R5, R5, #1

LDR R2, [R0], #4

LOOP

LDR R4, [R0], #4

CMP R2, R4

BHI LOOP1

MOV R2, R4

LOOP1

SUBS R5, R5, #1

CMP R5, #0

BNE LOOP

LDR R4, =RESULT

STR, R2, [R4]

HERE B HERE

VALUE1 DCD 0x00004, ~~0x00000004~~^{0x44444444}, 0xAAA1025B,
0x11111111, 0xFFFFFFFF

AREA DATA2, DATA, READWRITE

RESULT DCD 0x0

END

✓ List syntax and explain each instructions with example.

a) ~~Shift~~ instructions shift instructions

Syntax: Logical shift left by register. Rm, LSL Rs.

~~Logical shift left by immediate Rm, LSL #shift-imm~~

~~Logical shift left by register Rm, LSL Rs~~

PRE R5=5

R7=8

MOV R7, R5, LSL #2 | $R7 = R5 \ll 2$ ($R5 \ll 2$)

POST R5=5

R7=20 //

b) Arithmetic instructions.

Syntax: <instruction> {<cond>} {S} Rd, Rn, N.

Exp: It implements Arithmetic operations such as Add, Sub, mul, div, etc of 32 bit Signed and Unsigned values.

Ex.

PRE R0 = 0x00000000

R1 = 0x00000002

R2 = 0x00000001

SUB R0, R1, R2

POST R0 = 0x00000001

c) Logical Operators Instructions

Logical instructions perform bitwise logical operations on the two source registers.

Syntax: <Instruction> {<cond>} {S} Rd, Rn, #N

Example:

```
PRE  R0 = 0x00000000
      R1 = 0x02040608
      R2 = 0x10305070
      ORR R0, R1, R2
POST R0 = 0x12345678
```

d) Multiply Instructions. Multiply instructions multiply the contents of a pair of registers and depending upon the instruction, accumulate the results in with another register. The long multiplies accumulate onto a pair of registers representing a 64-bit value.

Syntax: MLA {<cond>} {S} Rd, Rm, Rs, Rn

MUL {<cond>} {S} Rd, Rm, Rs

~~MLA~~

Syntax: <Instruction> {<cond>} {S} RdLo, RdHi, Rm, Rs

Example: PRE R0 = 0x00000000

R1 = 0x00000002

R2 = 0x00000002

MUL R0, R1, R2 ; R0 = R1 * R2

POST

R0 = 0x00000004

R1 = 0x00000002

R2 = 0x00000002

e) Comparison Instructions

The Comparison instructions are used to compare or test a register with a 32-bit value. They update the CPSR flag bits according to the result, but don't affect other registers.

Syntax: <Instruction> {<cond>} Rn, #N

Example:

PRE CPSR = NZCVqifL_USER

R0 = 4

R1 = 4

CMP R0, R1

POST CPSR = NZCVqifL_USER