



Sirish Oruganti

 The University of Texas at Austin

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Experience

Graduate Research Assistant

Circuit Research Lab, The University of Texas at Austin

 August 2021 - Present

 Austin, TX, USA

Area of Research: **Hardware Security** | Advisor: **Prof. Jaydeep P. Kulkarni**

Analog Design Engineering Intern

Cirrus Logic Inc.

 May - August 2022, May 2023 - Present

 Austin, TX, USA

Analog Design Engineer

Texas Instruments India

 July 2018 - May 2021

 Bangalore, India

Visiting Student Researcher

VLSI Design Tools and Technology Laboratory, IIT Delhi

 May 2016 - June 2018

 Delhi, India

Publications and Patents

S. Oruganti*, N. Gupta, S. S. T. Nibhanupudi, M. Wang and J. P. Kulkarni (2023)

Security Robustness of Buried Power Rail Interconnect Technology: Modeling, Analysis and Countermeasures

 In: 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)

Y. Wang, S. Xie, J. Rohan, M. Wang, M. Yang, S. Oruganti*, and J. P. Kulkarni (2023)

A Graph Neural Network Computing-in-Memory Macro and Accelerator with Analog-Digital Hybrid Transformation and CAM-enabled Search-reduce

 In: 2023 IEEE Custom Integrated Circuits Conference (CICC)

S. Xie, M. Yang, S. A. Lanham, Y. Wang, M. Wang, S. Oruganti*, and J. P. Kulkarni (2023)

Snap-SAT: A One-Shot Energy-Performance-Aware All-Digital Compute-in-Memory Solver for Large-Scale Hard Boolean Satisfiability Problems

 In: 2023 IEEE International Solid-State Circuits Conference (ISSCC)

M. Wang*, S. Oruganti*, S. Xie, R. Kumar, S. Mathew and J. P. Kulkarni (2022)

Fine-Grained Electromagnetic Side-Channel Analysis Resilient Secure AES Core with Stacked Voltage Domains and Spatio-temporally Randomized Circuit Blocks

 In: 2022 IEEE European Solid-State Circuits Conference (ESSCIRC)

*Equally Contributing Authors

M. Erdogan, B. Singareddy, S. Vining, S. Rastogi, S. Oruganti, D. Wente (2020)

Low Power Embedded USB2 (eUSB2) Repeater

 USPTO Serial Number 20220206983

S. Oruganti, N. Pandey and R. Pandey (2018)

Electronically Tunable High Gain Current-Mode Instrumentation Amplifier

 AEÜ - International Journal of Electronics and Communications

S. Oruganti, Y. Gilhotra, N. Pandey and R. Pandey (2017)

OTRA Based Piece-Wise Linear VTC Generators and their application in High-Frequency Sinusoid Generation

 Advances in Electrical and Electronic Engineering, Vol. 15, No. 5, 2017

Education

Doctor of Philosophy in Electrical and Computer Engineering

The University of Texas at Austin

 August 2021 - Present

 Austin, Texas, USA

GPA 3.875

Integrated Circuits and Systems

Bachelor of Technology in Electronics and Communication Engineering

Delhi Technological University

(formerly Delhi College of Engineering)

 August 2014 - May 2018

 New Delhi, India

CGPA 9.42/10

Ranked 4th/194 in ECE Dept

Graduated **Summa Cum Laude**

Personal Details

Date of Birth

November 17, 1996

Place of Birth

Visakhapatnam, AP, India

Citizenship

Indian

References

Prof. Jaydeep P. Kulkarni

Prof. Diana Marculescu

Technical Skills

Cadence Virtuoso™

MATLAB™

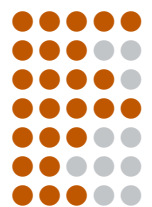
Linux (Ubuntu, Debian, Red Hat)

Productivity Applications

LaTeX, xCircuit

Mentor Graphics Calibre™

NI LabView™ and TestStand™




Positions of Responsibility

Chair - IEEE Graduate Student Chapter

The University of Texas at Austin

 April 2023 - Present

 Austin, Texas, USA

Founder Co-Chair - TI India Pride

Texas Instruments

 January 2020 - May 2021

 Bangalore, India

Head, Research and Development - IEEE DTU

Delhi Technological University

 August 2017 - May 2018

 New Delhi, India

Awards & Scholarships



Commendable Research Award

Delhi Technological University

2018



Prof. P. Kundu Memorial Medal

IEEE DTU

2018



Academic Merit Scholarship

Delhi Technological University

2018