

ER1 revision

ARCHI1

12/10/23

Mips 32

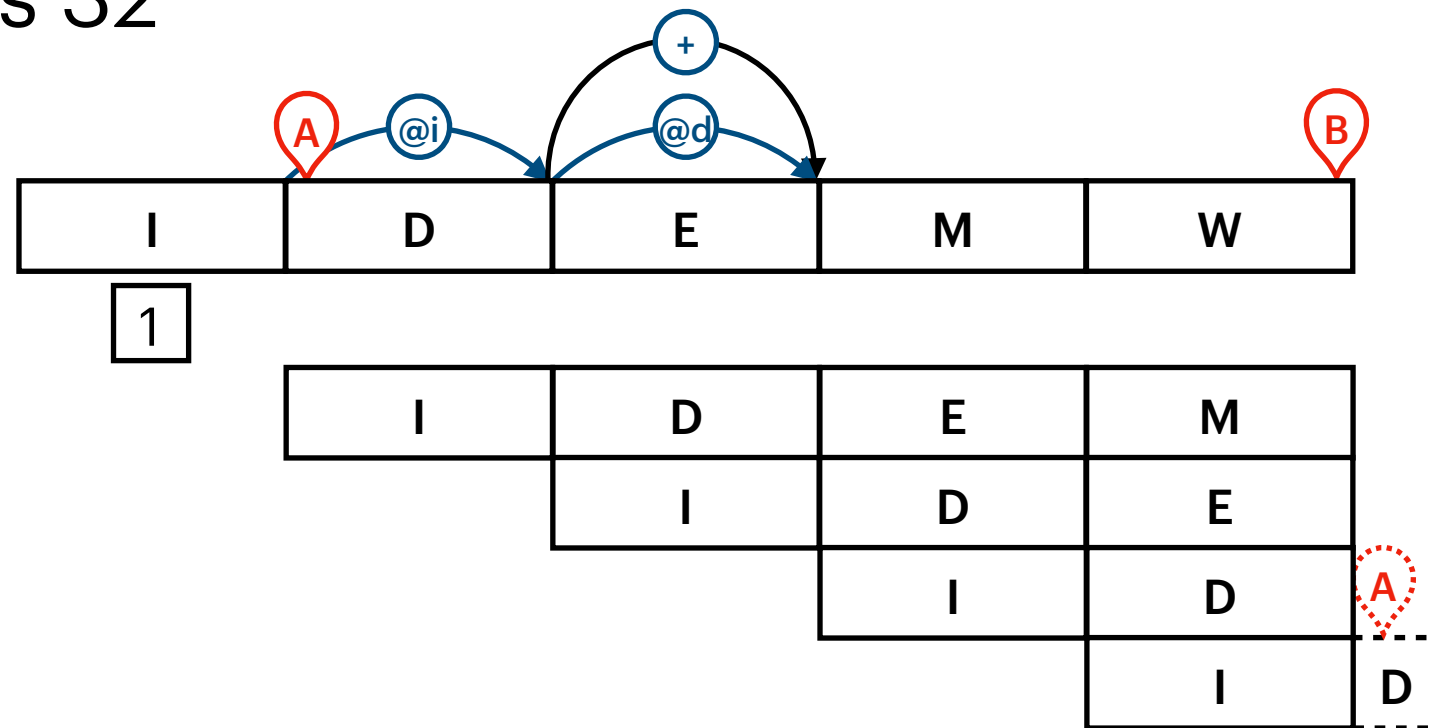
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Mips 32

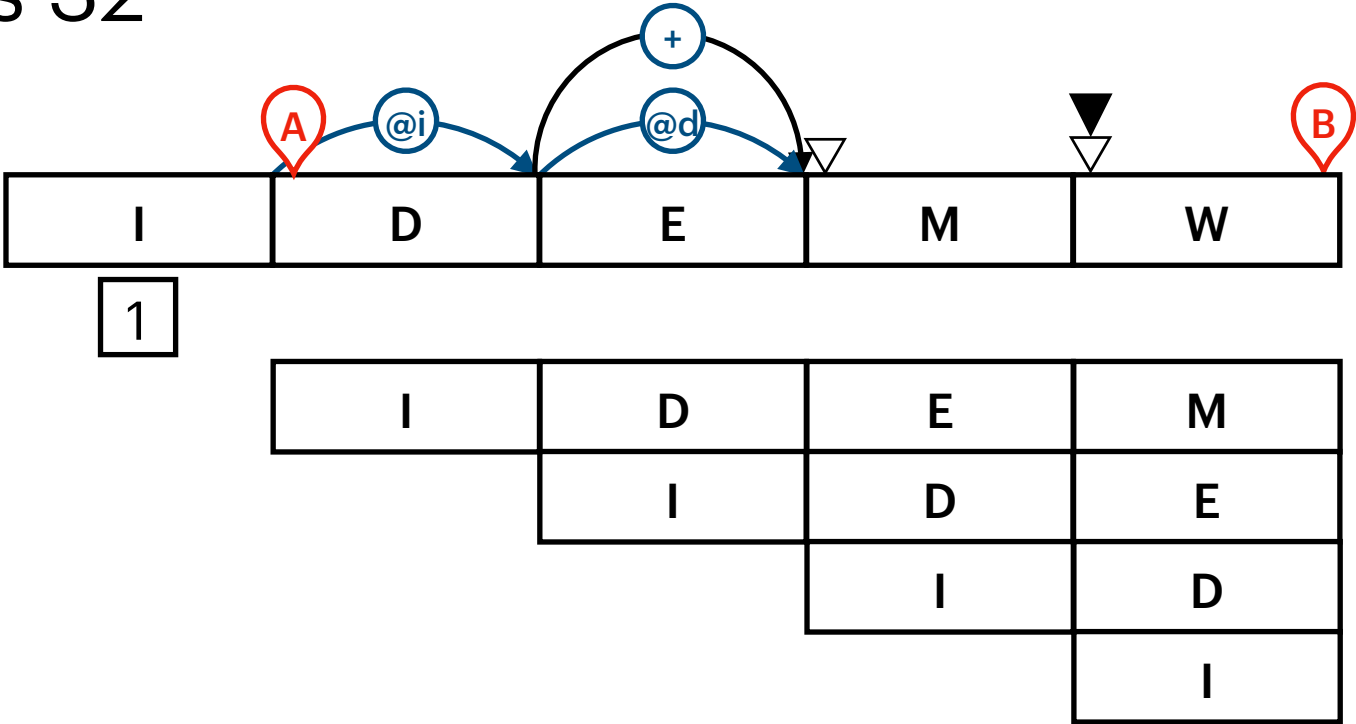
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Processor's point of
view at an instant t

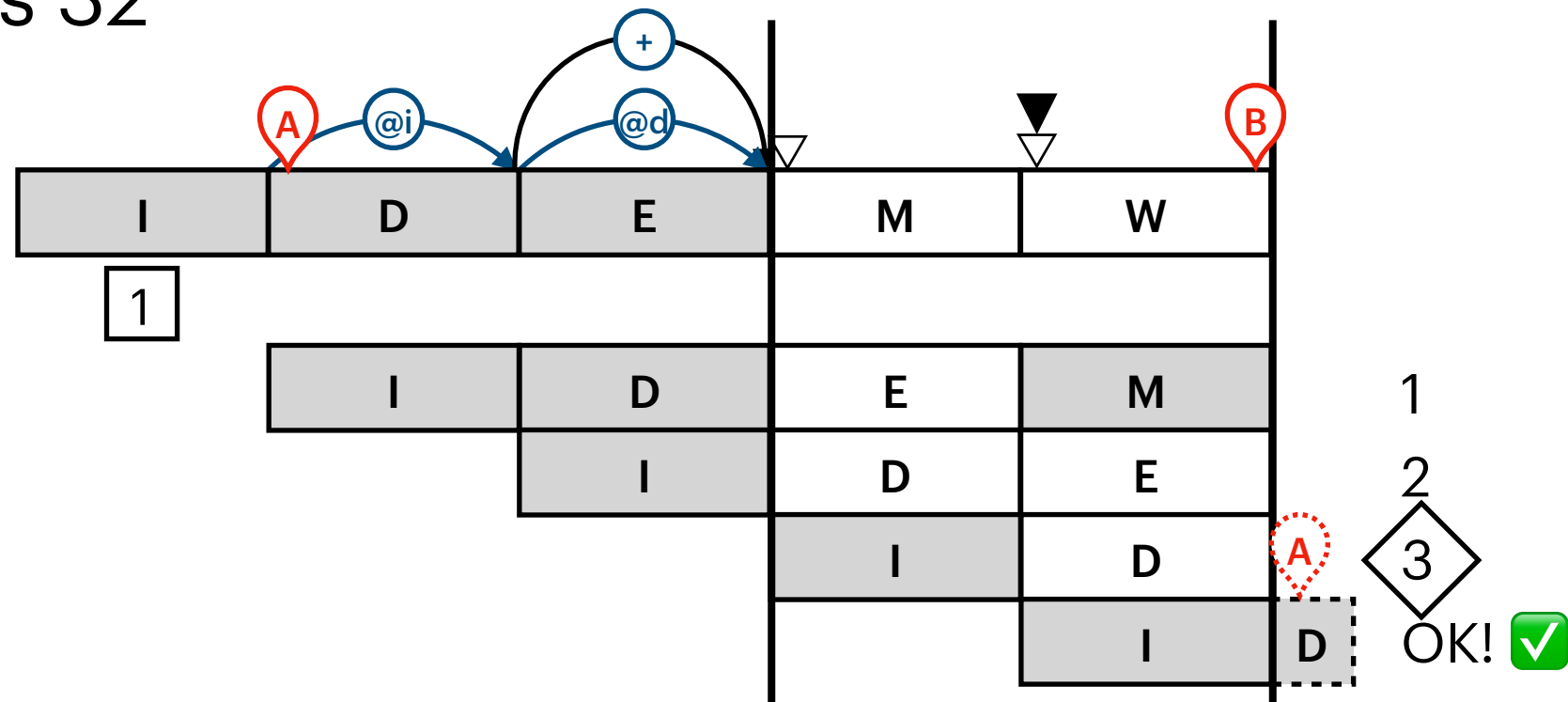
Mips 32



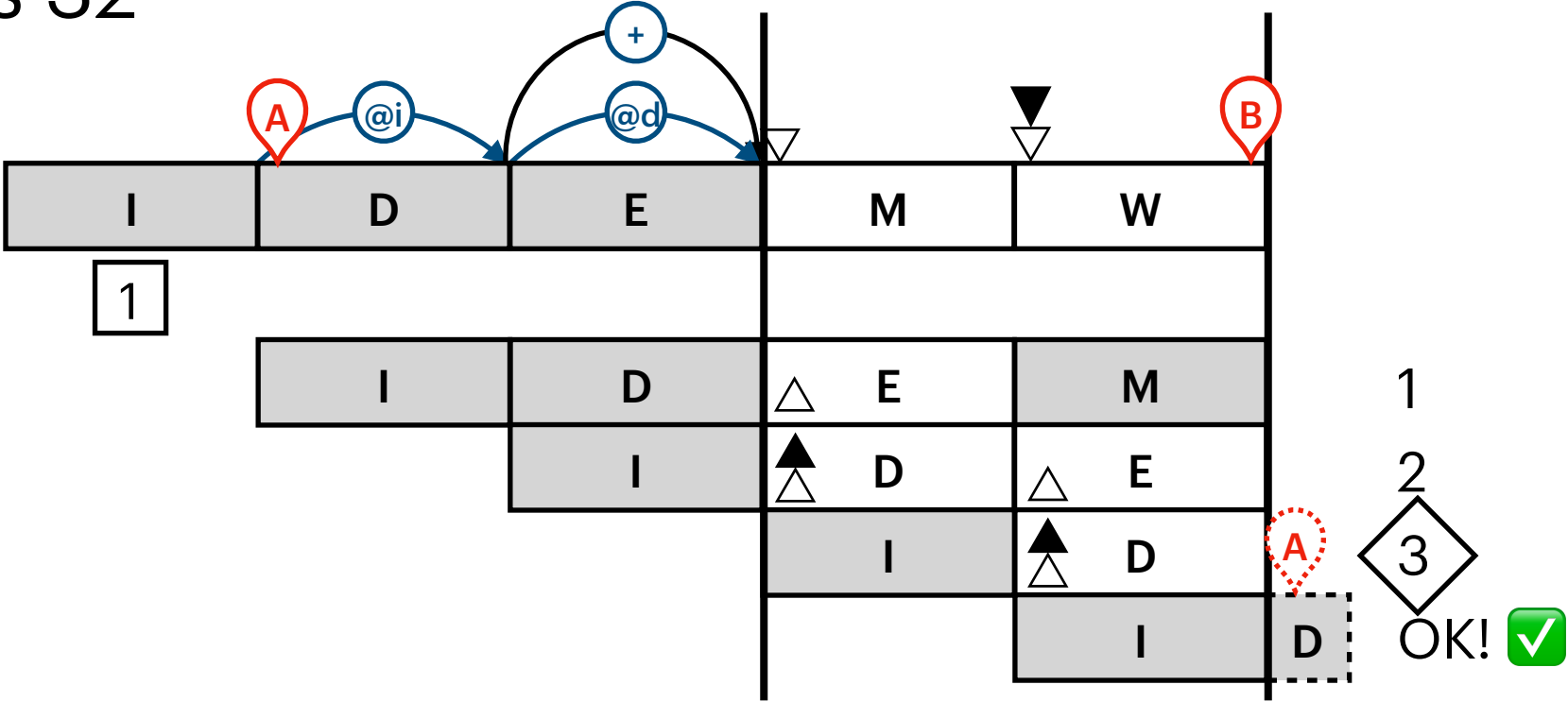
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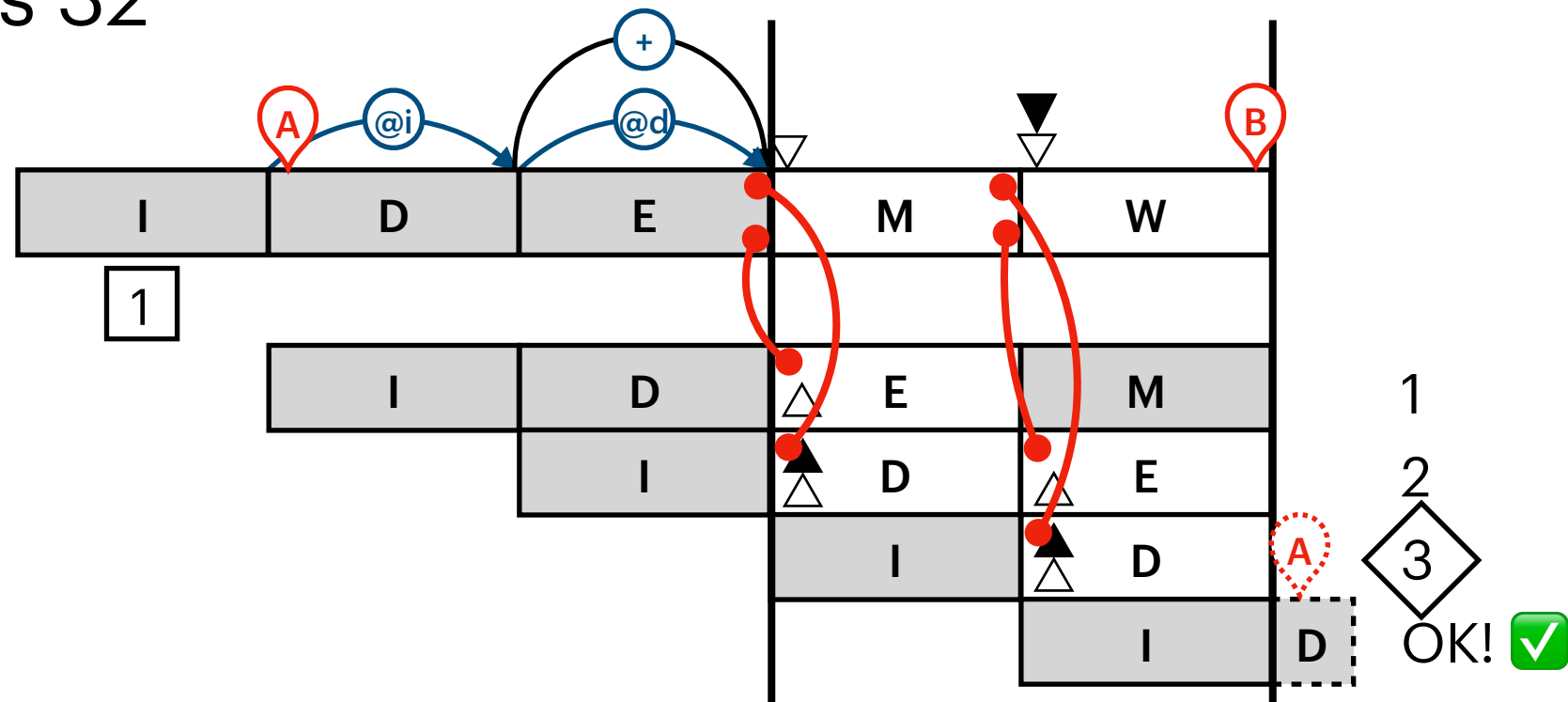
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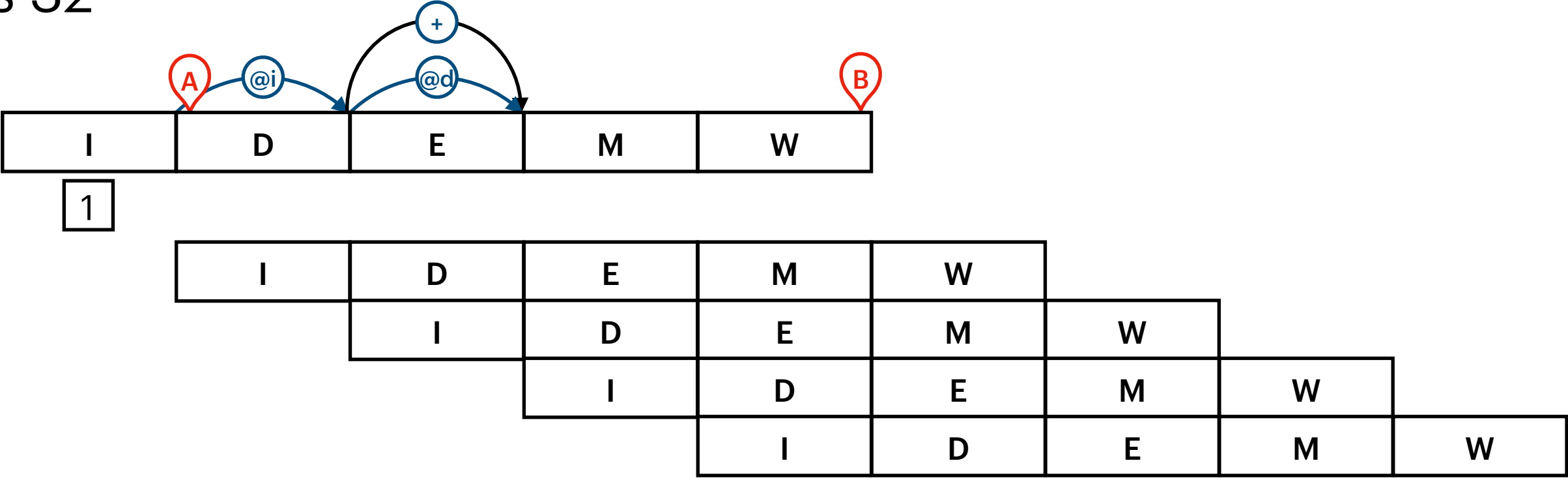
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Mips 32

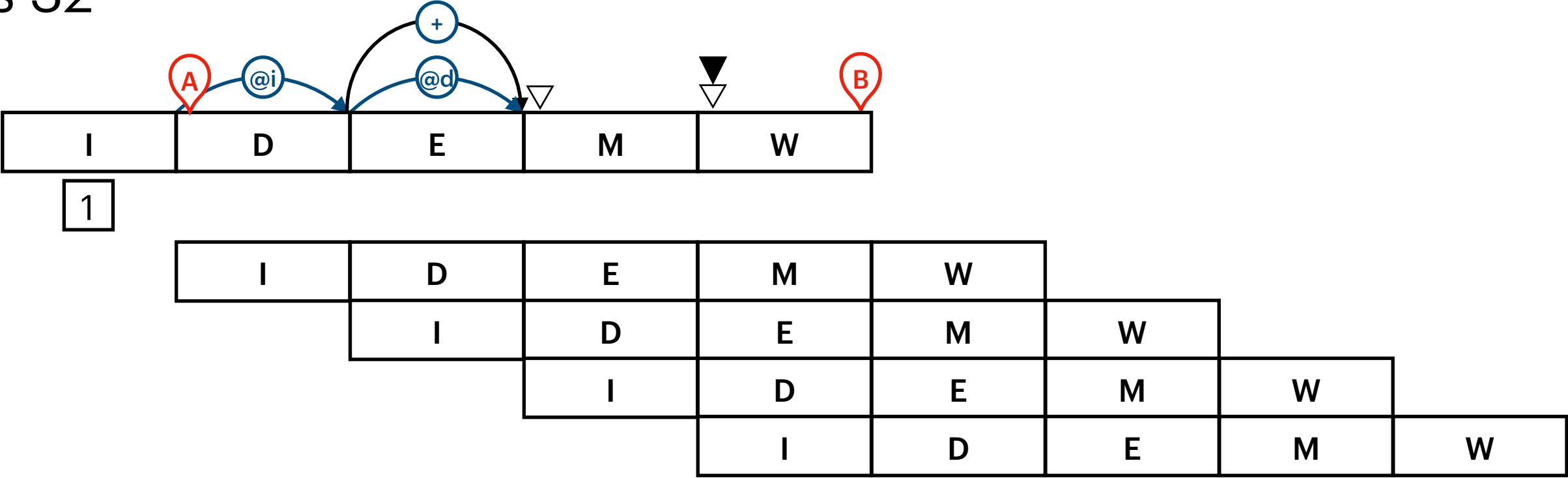
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I	D	E	M	W			
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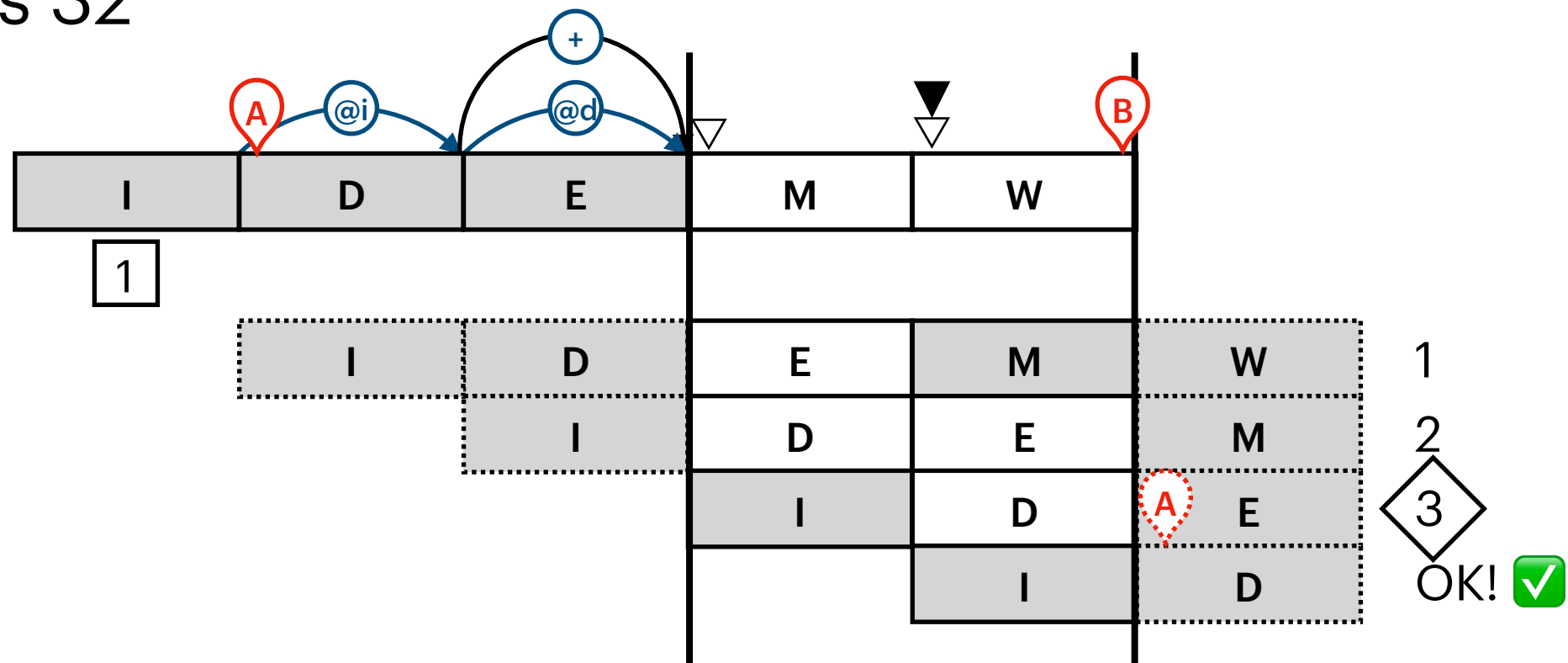
Mips 32



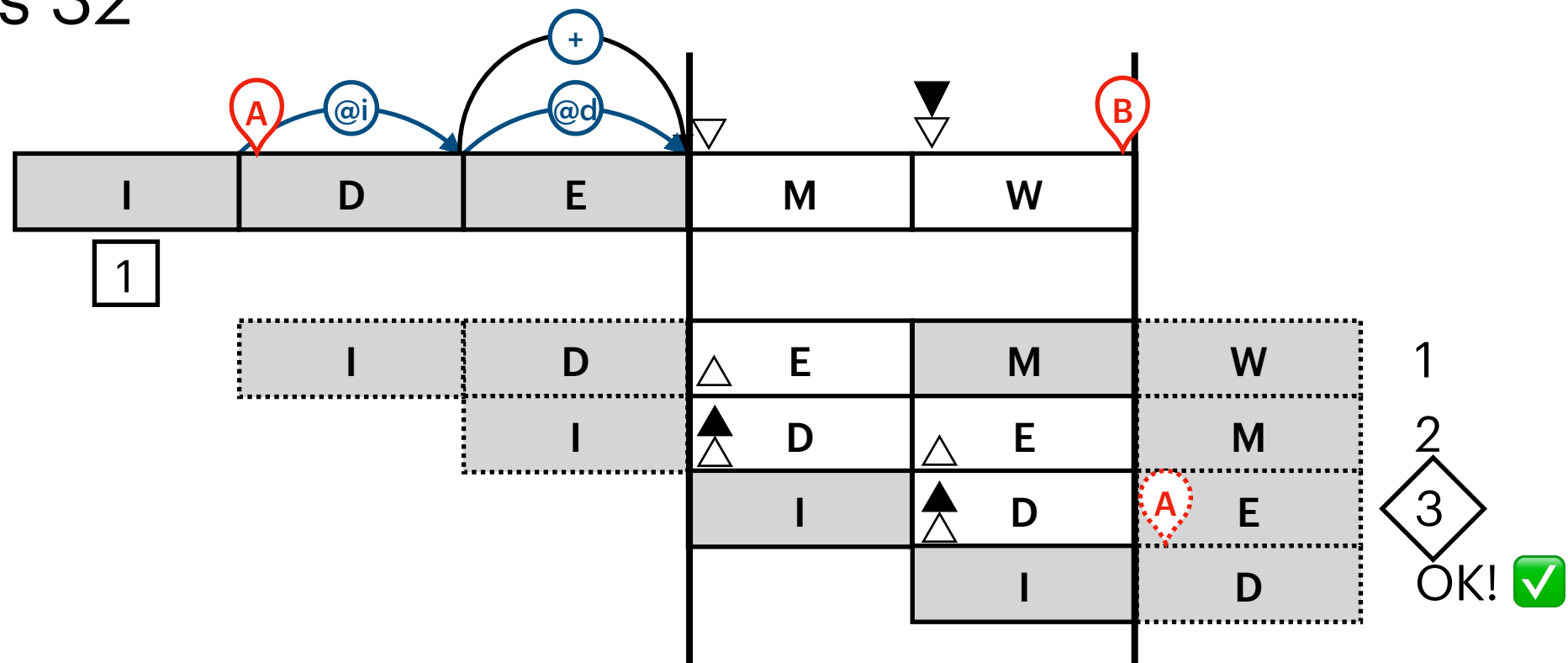
Mips 32



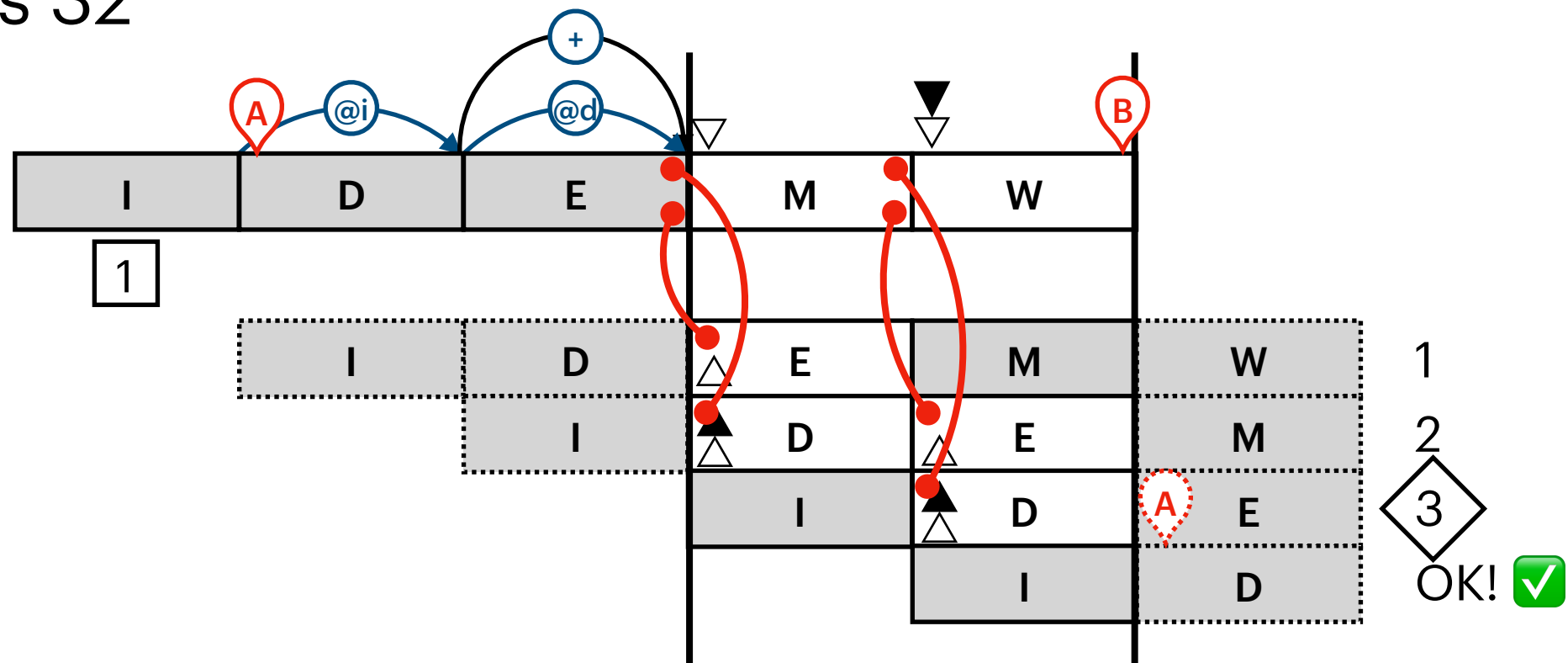
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Mips 32

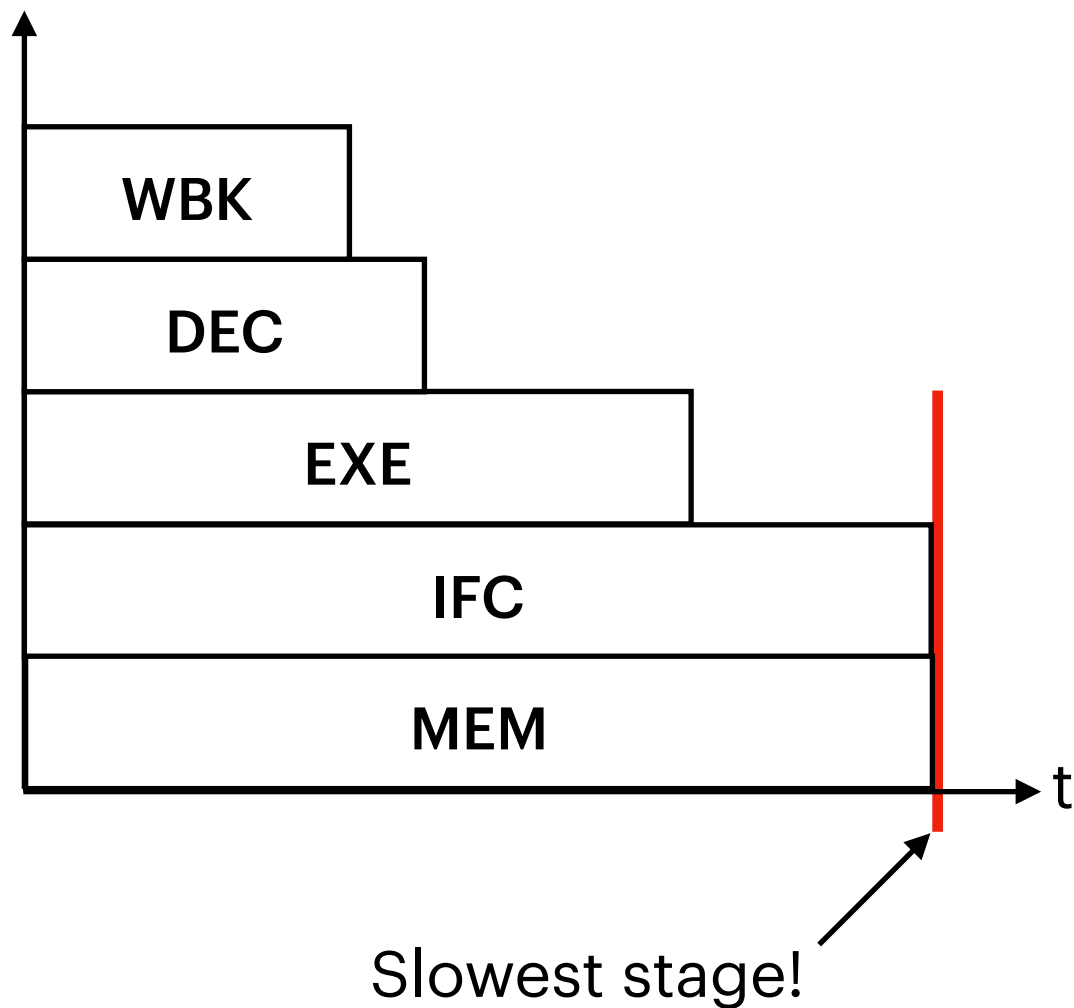


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Critical path

Non-superpipelined processor



Critical path

Superpipelined processor

