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The Design on FPGA-based Correlator in GPS Receiver Using ISE

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***Abstract*—The correlator is on of the key modules in GPS receiver, whose realizing construction could influence the positioning accuracy and real-time performance. The real-time FPGA-based GPS Correlator took the early code, late code and prompt code of local C/A code to correlate with the inputting signal parallel to get pre-detection value for GPS signal acquisition. The modules for generating measurement data were mainly designed, such as the carrier Numerical Controlled Oscillator (NCO) phase, carrier cycle count, code phase and epoch count and so on, and GPS correlator containing this module can be used on the GPS receiver for navigation and survey. In addition, the paper describes the designing project of the whole GPS correlator and the detail of each module in this correlator, and all the designs of GPS correlator were imple-mented in VHDL which were verified in Xilinx Virtex-II Pro development board. The results demonstrate that the GPS correlator can incorporate with microprocessor to realize GPS Receiver Baseband Signal Processing.**

***Index Terms*—GPS, correlator, measurement data, FPGA, ISE**

I. Introduction

The correlator is on of the key modules in GPS receiver and carries out the hardware of signal acquisition, tracking and locking to output original data and measurement data such as accumulated data, carrier, pseudorange code and so on to microprocessor; Microprocessor calculates the 3-dimenstion Position, Velocity and Time (PVT) of receiver whose basis is correlator which outputs all original data. So the correlator is so important that the performance immediately influence the overall performance of GPS receiver. The carrier NCO with high frequency resolution and code NCO contained in the correlator, which could impr-oves the precision of carrier tracking and code tracking. Meanwhile, the correlator for constructing navigation or measurement GPS receiver needs to output various measuring data. In summary, there are quite well study-ing value and practical significance to study correlator. Although it describes the design of carrier NCO, C/A code generator and accumulate and dump and so forth in [1, 2], the design of module for generating measuring data, which is the original data for calculating pseudorange observation and carrier phase observation such as carrier NCO phase, carrier cycles code phase, epoch counting and so forth, has not yet described.

As the advancement of logical source scale and processing velocity of FPGA has offered a quite practical and stable hardware designing platform for digital circuit designer, which could be used to carry out the design function circuit even the system-level circuit's design in practical work. The paper, just based on this way to study the techonogy of correlator in GPS receiver, carried out the GPS correlator on FPGA with ISE.The study in the paper would lay the foundation for the coming ASIC technology to design corresponding GPS special-purpose chip.

II. The Whole Framework Of Gps Receiver

As for the realization, the GPS receiver, implemented by correlator technology, is made up of radio frequency (RF) front end module, correlator module and processor module these three modules which were shown in Fig. 1, and the main task of RF front end is down conversing the frequency of RF analog signal before filtering and gain controlling, then A/D converting and quantifying the analog signal to produce digital intermediate frequency (IF) signal for correlator module whose main task is

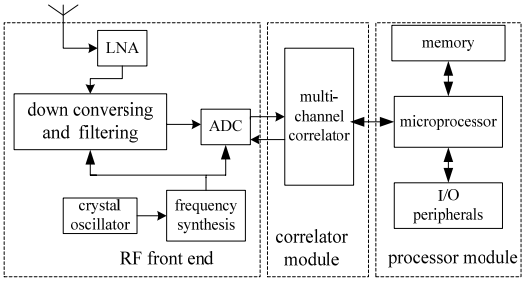

Figure 1. The whole framework of GPS receiver.

producing local carrier and local pseudo-code and making them multiply with the former digital IF signal to implement carrier stripping and code stripping getting integral accumulated value, in addition, the correlator module also outputs measurement data. On the other hand, the main task of processor module is implem-enting the acquisition judgment, code tracking loop contr-olling, carrier tracking loop controlling and decoding the navigation data according the integral accumulated data outputted by correlator, and calculating the pseudorange according to the measurement data from correlator at the same time by which are to realize the position calculation to output the PVT information of the user, where the correlator module is the point of the paper.

III. The Princile Of Gps Signal Correlating Reception

As the GPS signal transmission system is PCM-CDMA-BPSK, the receiver should recover base band signal by dispreading and demodulation while these processions need correlator to carry out. After generating the correlator peak the carrier has been synchronization with pseudocode, and it could dispread and demodulate to output navigation data, whose realizing principle is as follows:

In the paper, the influence of noise and the delay in receiver have been ignored, meanwhile, take convenience for discussion, the signal in paper is noted with continu-ous signal of single satellite signal. So the IF signal[3] outp-utted from RF front end could be noted as:

$$S(t) = \sqrt{2P}D(t-\tau)C(t-\tau)\cos(2\pi f_0 t + \phi) \tag{1}$$

where

P is the total IF signal power,

$C(\cdot)$ is the PRN code sequence,

$D(\cdot)$ is the materialization of the navigation data bits,

τ is the code group delay due to the travel time,

ϕ is the carrier phase of the signal, and

f_0 is the intermediate frequency of the IF signal.

$$\begin{aligned} S_I(t) &= \cos(2\pi \hat{f}_0 t + \hat{\phi}) \\ S_Q(t) &= \sin(2\pi \hat{f}_0 t + \hat{\phi}) \\ S_C(t) &= C(t-\hat{\tau}) \end{aligned} \tag{2}$$

where

$\hat{\tau}$ is the estimated code delay,

$\hat{f}_0$ is the estimated carrier frequency, and

$\hat{\phi}$ is the estimated carrier phase.

This IF signal is divided into two arms to mix with in-phase component $S_I(t)$ and quadrature component $S_Q(t)$ replica of the estimated carrier generated by local carrier NCO to remove the impact of the carrier.After this carrier wipe-off, the signal is then correlated (multiplied and integrated) with a replica of the spreading code $S_C(t)$ generated by local code generator over a period T_I refer-red to as the coherent integration time. This operation results in the output of an in-phase and a quadrature correlation value (I and Q). This process can be represented mathematically, neglecting the effect of the front-end filter, by:

$$I = \frac{1}{T_I}\int_0^{T_I} S(t)S_C(t)S_I(t)dt \tag{3}$$

$$Q = \frac{1}{T_I}\int_0^{T_I} S(t)S_C(t)S_Q(t)dt \tag{4}$$

Assuming a small carrier phase and code delay variation during the integration time, the correlation values can be approximated by:

$$I = \sqrt{\frac{P}{2}}D(t-\tau)R(\varepsilon_\tau)\frac{\sin(\pi\Delta f T_I)}{\pi\Delta f T_I}\cos(\varepsilon_\phi) \tag{5}$$

$$Q = \sqrt{\frac{P}{2}}D(t-\tau)R(\varepsilon_\tau)\frac{\sin(\pi\Delta f T_I)}{\pi\Delta f T_I}\sin(\varepsilon_\phi) \tag{6}$$

where

$R(\cdot)$ is the PRN autocorrelation function,

ε_τ is the code delay estimation error $(\tau - \hat{\tau})$,

Δf is the carrier frequency estimation error $(f_0 - \hat{f}_0)$, and

ε_ϕ is the carrier phase estimation error $(\phi - \hat{\phi})$.

Both I and Q values are then input into a phase discriminator that roughly assesses the carrier phase error. This estimate is then fed into the PLL loop filter for further low-pass filtering. The filter output will finally command the carrier NCO that will generate the updated local carrier replica for the next integration period.When the signal is acquired, tracked and fine adjust, the frequency and phase of local carrier and incoming carrier would be synchronism that $f_0 - \hat{f}_0$, $\phi - \hat{\phi}$, in addition, the phase of local C/A code and received C/A code's would be synchronized that $\tau - \hat{\tau}$. So the quadrature component in (6) would be 0 and in-phase component would be output navigation data bits:

$$I = \sqrt{\frac{P}{2}}D(t-\tau) \tag{7}$$

IV. The Design And Realization Of Gps Correlator's Circuit

There must be 4 satellites at least that the GPS receiver must receive and track at the same time to calculate the PVT while the GPS constellation is distributed for observing 4 to 11 at everywhere and every time. In the paper the GPS correlator which is compatible with GP2010 RF Front end was designed. The GPS correlator whose construction showed in Fig. 2 includes 12 channels

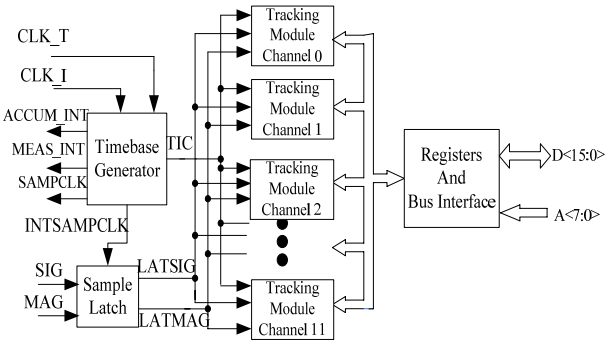

Figure 2. The construction of GPS correlator.

as more received satellite signals, higher precision of PVT; more tracking channels, faster acquiring satellite signal; and the rest channels could be used as redundant channels to acquire and track other satellites. There are 12 independent Tracking Module Channels, Sample Latch, Timebase Generator, Registers, Address Decoder and Bus Interface.

Where the Timebase Generator generates various clock signals: CLK_I and CLK_T are incoming main clocks; ACCUM_INT, an interrupting signal, is used to require microprocessor read the accumulated data of GPS correlator; MEAS_INT, an interrupting signal, is used to require microprocessor read the measurement data of GPS correlator; TIC is also an interrupting signal whose default cycle is 0.1s, but its cycle could also be changed by correcting the control register, which could latch the measurement data of 12 channels and offer observing epoch at same time; SAMPCLK could offer sampling signal to the RF front end; INTSAMPCLK, a internal sampling signal, outputs to Sample Latch whose function is synchronizing the digital IF signal; Registers and Bus Interface is the interface to processor.

What's more, the 12 tracking channels in GPS correlator, which are all same to one another, could independent of one another to control and set the tracked GPS satellite signals, what's shown in Fig. 3 is the module of tracking channel[4] which is made up of local Carrier NCO, Code NCO, Code Generator, Accumulate and Dump, Code Slew, Carrier Cycle Counter, Code Phase Counter and Epoch Counter and so on. The Fig. 3 indicates that, the inputting digital IF signal is divided into two arms to multiply with quadrature component and

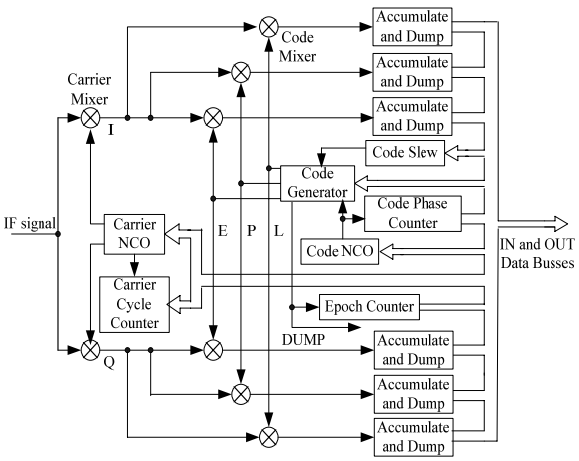

Figure 3. The construction of Tracking Channel.

TABLE I.
MAPPING RELATION BETWEEN CARRIER AND AMPLITUDE

phase	higher 3 bits phase	sin value	cos value
0～π/4	000	1	2
π/4～π/2	001	2	1
π/2～3π/4	010	2	−1
3π/4～π	011	1	−2
π～5π/4	100	−1	−2
5π/4～3π/2	101	−2	−1
3π/2～7π/4	110	−2	1
7π/4～2π	111	−1	2

in-phase component of local carrier, obtaining I and Q two arms of signals. Then the two arms of signal of I and Q carry out the correlation operation with early code, prompt code and late code at the same time obtaining 6 arms of accumulated data which are original data for dispreading, demodulating navigation message, in addition, this modu-le also generates Carrier NCO phase, Carrier cycle count, Code phase, Code NCO phase, Epoch count, which could be processed to obtain carrier phase observation and pseudorange observation. The following are the detail design and realization of every module in tracking channel.

A. Carrier Module

The realization of Carrier Module includes Carrier NCO and Carrier Measurement Data, which shown in Fig. 4.

Carrier NCO, made up of phase accumulator, phase register and phase-amplitude table 3 sections [5], is used to generate local carrier signal and adjust the Doppler shift deviating the nominal value and the frequency error of crystal oscillator. When the phase increment is M, the phase accumulator and phase register are N bits and the inputting reference frequency is f_s, it would outputs a carrier with outputting frequency and frequency resolution at $\frac{f_s \times M}{2^N}$ and $\frac{f_s}{2^N}$ respectively. The main frequency f_s is a clock signal at 40MHz, the phase accumulator and phase register are designed to set to 30 bits, then the frequency resolution is $\frac{40MHz}{2^{30}} \approx 37.25mHz$,

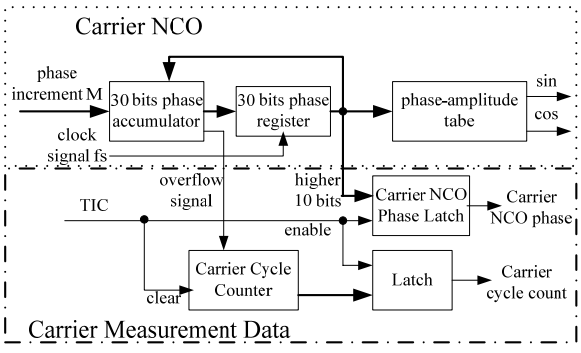

Figure 4. The construction of Carrier Module.

which could track the changing frequency of carrier accurately.

The local carrier generated by Carrier NCO is a signal whose variable quantity is ±1 and ±2 these 4 kinds of value, 8 sampling points. As there are 8 sampling phases, it only needs the higher 3 bits of phase register as the inputting of look-up table. What's shown in Table I is the corresponding relation between phase and amplitude.

The function of Carrier Measurement Data[6] is counting the carrier phase's going forward within certain time; the function of Carrier Cycle Counter is generating the Carr-ier cycle count measurement data which is the number of carrier cycles within 2 kinds of TIC interval, and this counter, which is designed as 22 bits and guarantee that the number of carrier cycles would not exceed the counting range, is droved by overflow signal of phase accumulator in Carrier NCO. The function of Carrier NCO Phase Latch is generating Carrier NCO phase measurement data which is the higher 10 bits outputted by phase register of Carrier NCO at each TIC, so the resolution of Carrier NCO phase is $2\pi/1024$. What's shown in Fig. 5 is principle of counting the forward of carrier within 2 TIC intervals.

$$\Delta Y_1 = 2\pi \times k_1 + (2\pi - PH_0) + PH_1 \qquad (8)$$

Where k_1, Carrier cycle count, is noted as the number of generated carrier cycle within TIC_0 and TIC_1, PH_0 and PH1 are noted as Carrier NCO phase at the time of TIC_0 and TIC_1 respectively, so ΔY_1 is the marched phase within TIC_0 and TIC_1. It could get the carrier phase observation after the value got from (8) processed microprocessor.

B. Code Module

What's shown in Fig. 6 is code module, which is made up of Code NCO, Code Slew, Code Generator and Code Phase Counter and 3-bit shift register[7].

Where the function of Code Phase Counter is generating the Code phase measurement data, in other words, it is used to get the code phase at each TIC, whose realization is similar to the Carrier NCO Phase Latch in Carrier Measurement Data. There are similar construction for Code NCO and Carrier NCO, which is used to compose 2 clock signals that are CLK_CODE which is the same as

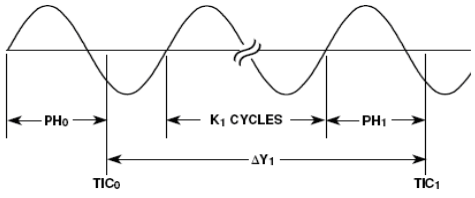

Figure 5. Carrier phase counting.

C/A code piece whose frequency is 1.023MHz and

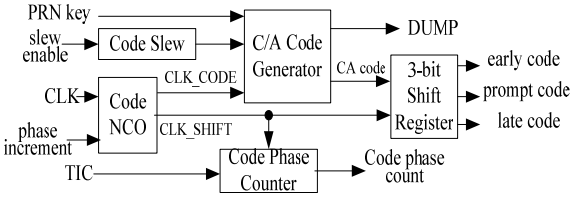

Figure 6. The Code Module construction.

CLK_SHIFT at the frequency of 2 times of C/A code piece. The function of Code Generator module is generating C/A code and also DUMP signal at the same time for other module. The signal CLK_SHIFT outputted by Code NCO could drive the 3-bit Shift Register directly, generating 3 code sequences which differ 1/2 code piece in turn. We may input the outputting signal of Code NCO into 1/2 Frequency Division to generate the signal at 1.023MHz and drive C/A Code Generator to generate corresponding C/A code signal; and then transmit this C/A code signal to 3-bit Shift Division to obtain early code, prompt code and late code these 3 sequences which differ 1/2 code piece in turn for pseudocode's parallel search and tracking loop.

The Code Slew, made up of subtract counter and some other controlling circuit, mainly makes the C/A Code Generator stop working before the subtract counter's coming to 0, and outputs a enable signal to Accumulator and Dump, which is noted as invalid working status while it is counting. The Code Slew outputs an enable signal when it needs to slew code, which stops the C/A Code Generator working, so the local code stop going forward while the received code are going forward all the time, which could change their phases difference. Therefore, the processor could adjust the status of local phase in real time with controlling code slider module.

C. Correlating Accumulator Module

We input IF signal in Tracking Channel to mix with in-phase component and quadrature component of local carrier; and then carry on the correlating operation with local early, prompt and late C/A code to obtain 6 accumulated datas. What's shown in Fig. 7 is the construction of Correlating Accumulator which mainly includes ADDER and REGISTER, Carrier mixer and Code mixer.

The ADDER and REGISTER in this module accumulates the data within an integrated code cycle (1ms) which is generated by the IF signal processed by Carrier mixer and Code mixer[8]. The ADDER and REGISTER are designed as 16-bit to combine 16-bit accumulator whose accumulating result is a correlating accumulating value within a C/A code cycle. As for these correlating accum-ulating values, they must be read before the next DUMP signal or it would be covered, and the data velocity is falling from 5.714MHz to 1kHz at this time which is in the range of later microprocessor's ability.

D. Epoch Counter

The Epoch Counter whose function is generating measurement data of Epoch count includes 1ms Epoch count and 20ms Epoch count[9], which shown in Fig. 8. DUMP, generated at the end of C/A code whose frequency is 1KHz, is taken as driving clock to drive 1ms Epoch Counter which is vicenary counter with the counting range within 0-19, it generates 1ms Epoch count and

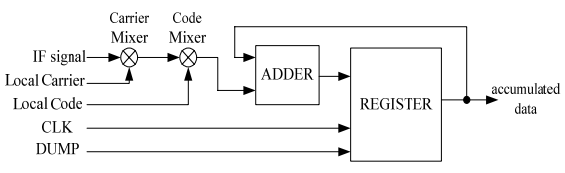

Figure 7. The construction of Correlating Accumulator.

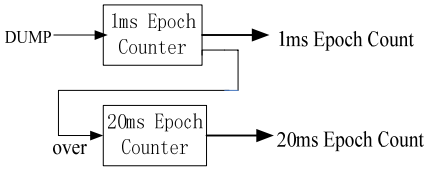

Figure 8. The construction of Epoch Counter.

counting overflow signal 'over' which is taken as driving clock to drive 20ms Epoch Counter which is a five decimal based counter with the counting range from 0-49 and it generates 20ms Epoch count. These two counters register the epochs from 0-999ms together; on the other hand, they could also used to carry out the bit synchronization and frame synchronization, and it could obtain pseudorange observation by processing the Epoch count and Code phase with relative software of processor.

V. Verification Of FPGA Design

The design in the paper is based on FPGA developing tool ISE 9.2i of Xilinx and the FPGA chip on development board, the serial of Xilinx Virtex-II Pro, is XC2VP30 which has abundant logic source with 30618 logic cells, BRAM with 2448kB and 8 digital-clock managers, that is, there are sufficient source to the realization of GPS correlator. The following is the simulation of key module in GPS correlator.

What's shown in Fig. 9 is the simulation of Carrier Module. Where clk is clock signal; rst is a signal to reset system; tic is a TIC signal; fcntrl signal is phase increment; sin and cos are in-phase component and quadrature component of local carrier signal respectively; carcycle is Carrier cycle count; carphase is Carrier NCO phase. In the simulation, the fctrl is set as a hexadecimal of '23FA689', then the outputting carrier's frequency is the central frequency of GPS digital IF at 1.405MHz, and it could combine to the processor through reading and writing the Carrier NCO control register that is read by the correlator circuit to assigned to fctrl, which is used to adjust the frequency between the local carrier and received carrier for synchronization. It could be indicates from the simulation that the carcycle and carphase, the points to latch tic, are set as 9 and 185 while the former are 8 and 370 at the time of latching tic, and the time between these two intervals of tic could be used to calculate the changing phase of the passed carrier.

What's shown in Fig. 10 is the simulation of Code

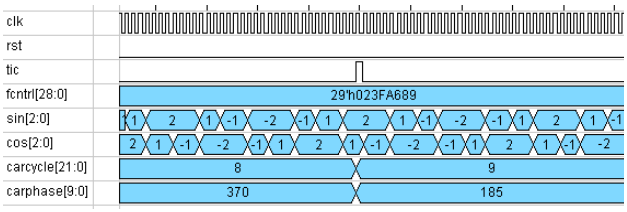

Figure 9. The simulation of Carrier Module.

NCO and C/A Code Generation where the phase increment fctrl is set as a hexadecimal of '1A30552', and the outputting signal clk_shift is 2.046MHz that is taken for 3-bit Shift Register to obtain 3 code sequences of early

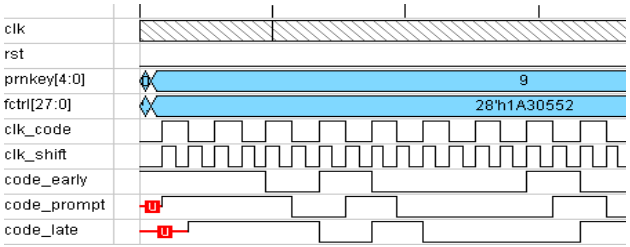

Figure 10. The simulation of Code NCO and C/A Code Generation.

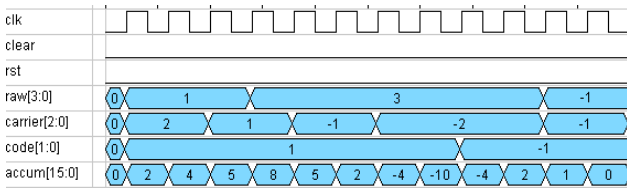

Figure 11. The simulation of Correlating Accumulator.

code, prompt code and late code that differ 1/2 code piece in turn. The clk_code to driver C/A Code Generator is 1.023MHz. It is similar to Carrier NCO that processor could write Code NCO controlling register through bus that is assigned to fctrl to adjust local clock frequency of Code NCO in real time. prnkey is a signal to choose satellite whose range is 0-31 corresponding to the choosing satellites within 1-32. The satellite chose in figure is NO.10 satellite whose former 10 code chip is: 1101000100 which matches the C/A code of satellite, that is, the Prn_key is 9 and the early, prompt and late code these 3 sequences of local C/A code differ half code piece in turn.

What's shown in Fig. 11 is the simulating result of Correlating Accumulator where clk is accumulating clock signal; clear is DUMP signal at the end of code; raw is IF signal output by RF front end; carrier is noted as local carrier; code is noted as local code; accum is noted as accumulated data which is read with bus when connected to microprocessor.

VI. Verification Of FPGA-based Correlator

The correlator is the key section of baseband signal procession which contains signal acquisition, signal tracing and data decoding in GPS receiver. What said before is the detail of correlator designing, and then we would validate whether the performance of correlator, designed in this paper, could process the GPS baseband signal, which was implemented by FPGA, which actes as FPGA-based correlator and DSP that would accomplished the software of signal acquisition, signal tracking and data decoding, and then transmit the result to PC to save as data file for MATLAB in which analyzed.

Fig. 12 shows the 3-D correlation plot of NO.10 satellite. what's shown in the figure that there is a conspicous correlation peak indicates the signal is successfully acquisied. Fig. 13 shows an in-phase /quarature scatter plot that is the prompt-Q Correlation value plotted versus the prompt-I Correlation value of NO.10 satellite. Successful phase lock is achieved once all the signal energy is steered to the channel. Fig. 14 shows a time history of the prompt-I Correlation or the bits of the navigation message.

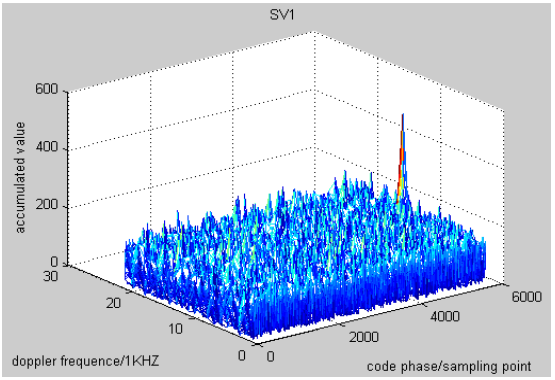

Figure 12. The 3-D correlation peak of NO.10 satellite

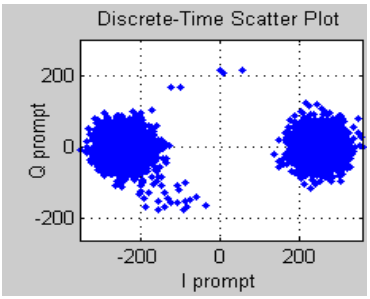

Figure 13. The in-phase / quarature scatter plot.

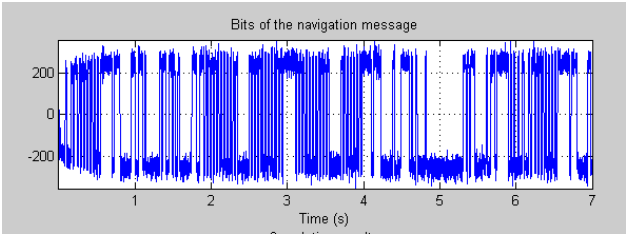

Figure 14. The prompt-I Correlation value

The results of the experiment indicated that the FPGA-based correlator designed in this paper could perform the baseband signal processing collaborating with microprocessor.

VII. Conclusions

The paper describes the design of GPS correlator at first, then studies the realization on Xilinx Virtex-II Pro development board with VHDL language based on ISE 9.2i platform, and reaches successful achievement in FPGA. In addition, the paper offers the designing principle and simulating result of all modules. The results indicate that the GPS correlator developed in the paper could output the accumulated data and measurement data correctly; the Carrier NCO and Code NCO could generate carrier and C/A code clock signal respectively whose frequency and code velocity could be controlled, therefore, it could carry out the acquiring accurately and tracking of carrier and C/A code; and the combination of GPS correlator and microcomputer could accomplish the baseband signal processing of GPS signal. In summary, the GPS correlator studied in the paper could be directly used into the GPS receiver.

Acknowledgment

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