Costas Loop Implementation for Synchronous Detection of Carrier in Radio Receiver

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***Abstract*-**In this paper, a Costas loop based method has been presented for digital receivers. The other most commonly used existing method is PLL but it suffer from the drawback of phase ambiguity. The proposed Costas loop overcomes this drawback of phase ambiguity. The proposed Costas loop has been designed and simulated using Simulink and System Generator Blocksets. The results show that the proposed design in digital receivers for providing high performance solution in wireless communication applications is capable of efficiently removing the phase ambiguity.

***Keywords*-**Costas loop, PLL, Receiver, Simulink, System generator.

1. INTRODUCTION

A carrier recovery system is a circuit used to estimate and compensate for frequency and phase differences between a received signal's carrier wave and the receiver's local oscillator for the purpose of coherent demodulation or Carrier recovery is a technique for extracting the RF carrier from a modulated signal so that it can be reinserted and used to recover the modulating signal [1].

In the transmitter of a communications system, a carrier wave is modulated by a baseband signal. At the receiver the baseband information is extracted from the incoming modulated waveform. In an ideal communications system the carrier frequency oscillators of the transmitter and receiver would be perfectly matched in frequency and phase thereby permitting perfect coherent demodulation of the modulated baseband signal [2]. However, transmitters and receivers rarely share the same carrier frequency oscillator. Communication receiver systems are usually independent of transmitting systems and contain their own oscillators with frequency and phase offsets and instabilities. Doppler shift may also contribute to frequency differences in mobile radio frequency communication systems. All these frequency and phase variations must be estimated using information in the received signal to reproduce or recover the carrier signal at the receiver and permit coherent demodulation [3].

The two common methods for BPSK carrier recovery are:

(1) The conventional PLL

(2) The 180° Costas loop.

The BPSK demodulation using conventional PLL presents 180˚ phase ambiguity whenever the data signal changes its phase from 0˚ to 180˚ and vice versa [4]. Thus the demodulated data signal will be the reverse of the data that is originally transmitted that is not desirable. The solution to overcome this 180˚ phase ambiguity is the Costas Loop. The Costas loop relies on feedback concepts related to the PLL [5]. The Costas loop offers an inherent ability to self-correct the phase (and frequency) of the recovered carrier and, in the end; its implementation is no more complicated than the first technique [6]. Its main disadvantage is involvement of a loop settling time.

2. COSTAS LOOP IN RECEIVER

In digital modulation scheme, an analog carrier is modulated by a digital data bit stream. In BPSK we change the phase of the sinusoidal carrier to represent information bit. The information bit '0' is transmitted by shifting the phase of the sinusoid by 180˚ and information bit '1' is transmitted without any phase change in sinusoid i.e. with a 0˚ phase shift. Binary Phase shift keying is one of the most efficient binary data modulation techniques in terms of noise immunity per unit bandwidth.

The Costas Loop can sense both the 0˚ and 180˚ phases at its input [7]. Thus when the incoming data reverses its phase the loop will not anti lock and still detect the data in the order it was transmitted. Costas loop is a kind of closed loop and auto tracking system that can be applied in tracking the input signal's phase. The Costas loop performs both phase coherent suppressed carrier reconstruction and synchronous data detection within the loop. It is widely used in fields of radio technology and has become an indispensable part of communication, radar, navigation, electronic equipments and other devices. The performances of traditional Costas loop are affected because of the imbalance between in phase branch and Quadrature branch, and there are also some disadvantages such as direct current zero excursion and difficulty to debug. But these problems can be avoided by using all digital Costas loop [8]. This improved carrier recovery loop is implemented by all digital methods. It can not only be integrated into one chip without any analog section, but also consume low thermal power. The classical Costas loop for BPSK demodulation is shown in the Figure 1. The system involves two parallel tracking loops operating simultaneously from the same VCO (Voltage Controlled Oscillator) or NCO (Numerically Controlled Oscillator). The first loop, called the in phase loop (or I arm), uses the VCO as in a PLL (Phase Locked Loop), and the second, called the Quadrature loop (or Q arm) uses a 90 degree shifted VCO. The I and Q mixer outputs are filtered by single pole Butterworth low pass filters. The I and Q arm filter outputs are multiplied together and the product is scaled and filtered to produce the loop error used to control the VCO. The loop error should settle to a value when the loop is locked. A negative loop error decreases the VCO increment resulting in a lower VCO frequency, and similarly, a positive loop error increases the VCO increment resulting in a higher VCO frequency. The low pass filters in each arm must be wide enough to pass the data modulation without distortion [9].

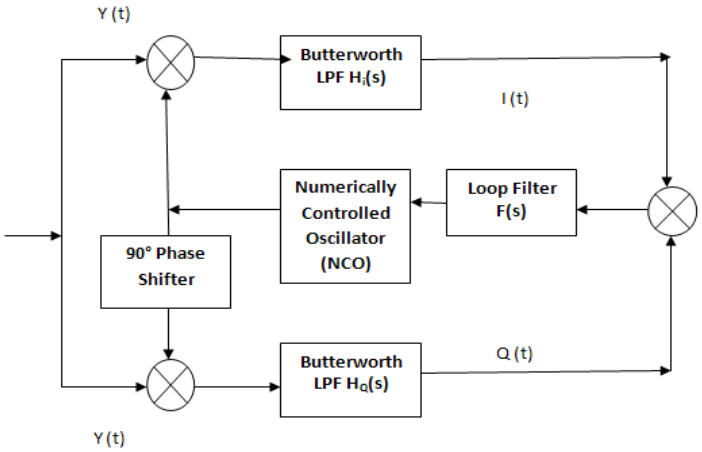

Figure 1: Costas Loop Block Diagram

The input to the Costas loop is the waveform written as

$$Y(t) = m(t) * \sin(w_c t + \Psi(t)) + n(t) \qquad (1.1)$$

Where m (t) is the BPSK modulation and n (t) is a white band pass noise. The in-phase mixer generates

$$I(t) = m(t) * \cos \Psi(t) + n_{mc}(t) \qquad (1.2)$$

While the Quadrature mixer generates

$$Q(t) = m(t) * \sin \Psi(t) + n_{ms}(t) \qquad (1.3)$$

Where the mixer noise $n_{mc}(t)$ and $n_{ms}(t)$ are low pass demodulated noise processes in the carrier noise n (t). The output of the multiplier is then

$$I(t)\,Q(t) = m^2(t) \sin(2\Psi(t))/2 + n_{sq}(t) \qquad (1.4)$$

Where n_{sq} (t) represents all the signal and noise cross-products. The multiplier of the Costas loop can be thought

of as allowing the bit polarity of the in-phase loop to correct the phase error orientation of the tracking loop, thereby removing the modulation [10].

3. PROPOSED COSTAS LOOP

The Proposed Model has been developed using Simulink and Xilinx System Generator Blockset. In the proposed design, a block diagram of the proposed Costas loop for carrier recovery is given in figure 2.

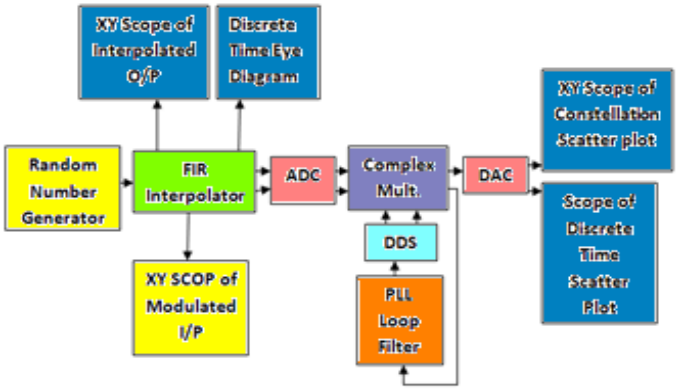

Figure 2: Block diagram of Costas loop.

There are various different blocks in the block diagram of the Costas loop, which is explained one by one.

3.1 Random Number

The Random Number block generates normally distributed random numbers. The seed is reset to the specified value each time a simulation starts. By default, the sequence produced has a mean of 0 and a variance of 1, although any one can vary these parameters. The sequence of numbers is repeatable and can be produced by any Random Number block with the same seed and parameters. To generate a vector of random numbers with the same mean and variance, specify the Seed parameter as a vector.

3.2 FIR Interpolator

The FIR Interpolation block resamples the discrete-time input at a rate *L* times faster than the input sample rate, where the integer *L* is specified by the Interpolation factor parameter. This process consists of two steps:

(1)The block upsamples the input to a higher rate by inserting *L*-1 zeros between samples. (2)The block filters the upsampled data with a direct-form FIR filter.

The FIR Interpolation block implements the above upsampling and FIR filtering steps together using a polyphase filter structure, which is more efficient than straightforward upsample-then-filter algorithms.

The FIR filter coefficients parameter specifies the numerator coefficients of the FIR filter transfer function *H* (*z*). The coefficient vector, [b (1) b (2) ... b (m)], can be generated by one of the Signal Processing Toolbox filter design functions (such as fir1), and should have a length greater than the interpolation factor (*m*>L). The filter should be lowpass with normalized cutoff frequency no greater than 1/*L*. All filter states are internally initialized to zero. The FIR Interpolation block supports real and complex floating-point and fixed-point inputs except for complex unsigned fixed-point inputs. This block supports triggered subsystems when you select Maintain input frame rate for the Framing parameter.

3.3 Scope of Interpolated Out

This block has two scalar inputs. The block plots data in the first input (the *x* direction) against data in the second input (the *y* direction).

This block is useful for examining limit cycles and other two-state data. Data outside the specified range is not displayed.

3.4 Eye Diagram

The Discrete-Time Eye Diagram Scope block displays multiple traces of a modulated signal to produce an eye diagram. The Discrete-Time Eye Diagram Scope block has one input port. The block accepts signal of type double, single, Boolean, base integer, and fixed-point data types for input, but will cast it as double. In sample-based

mode, the input signal must be a scalar value. In frame-based mode, the input must be a column vector or a scalar value.

3.5 PLL Loop Filter

The block commonly called the PLL loop filter (usually a low pass filter) generally has two distinct functions. The primary function is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at startup. Common considerations are the range over which the loop can achieve lock (pull-in range, lock range or capture range), how fast the loop achieves lock (lock time, lock-up time or settling time) and damping behavior.

Depending on the application, this may require one or more of the following: a simple proportion (gain or attenuation), an integral (low pass filter) and/or derivative (high pass filter). Loop parameters commonly examined for this are the loop's gain margin and phase margin. Common concepts in control theory including the PID controller are used to design this function. The second common consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input. This frequency modulates the VCO and produces FM sidebands commonly called "reference spurious". The low pass characteristic of this block can be used to attenuate this energy, but at times a band reject "notch" may also be useful.

3.6 DDS

A Subsystem block represents a subsystem of the system that contains it. The Subsystem block can represent a virtual subsystem or a true (atomic) subsystem, depending on the value of its Treat as atomic unit parameter. An Atomic Subsystem block is a Subsystem block that has its Treat as atomic unit parameter selected by default.

4. SIMULATED RESULTS

The Developed Model has been simulated using Simulink. The Simulated results of the proposed design discussed in the following sections.

4.1 Modulated Input

This is the XY plot which measures the values between X-axis and Y-axis. The range of the value on the x-axis may vary from -1.5,-1,-0.5, 0, 0.5, 1, 1.5 etc. The y-axis has the same range of values. In figure 3, the value of modulated input is more on y-axis as compared to the x-axis.

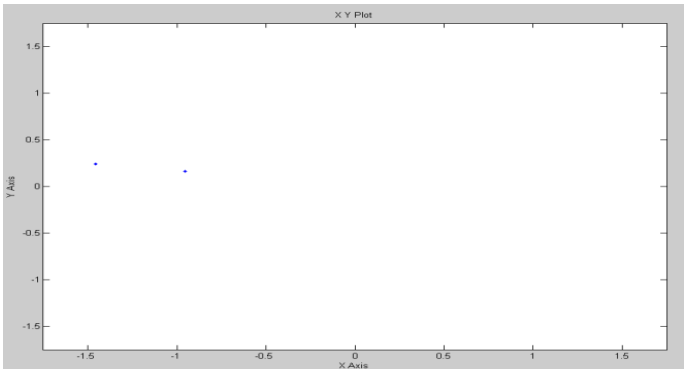

Figure 3: Modulated input

4.2 Eye Diagram

The Eye diagram is the graph between the In-phase versus time and Quadrature versus time. The Inter Symbol Interference (ISI) affects the signal mostly at the In-phase condition. The more is the eye opening in the figure; less will be the affect of ISI on the signal performance.

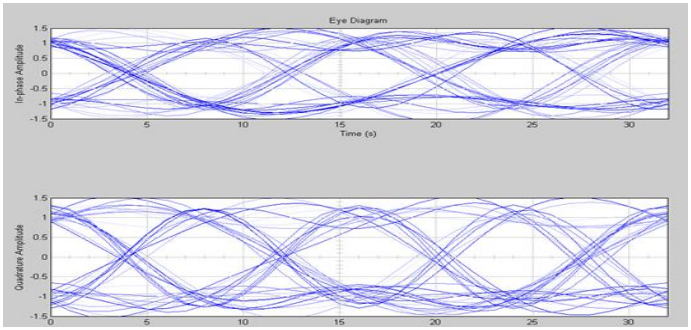

Figure 4: Eye diagram

4.3 XY Scope of Constellation Scatter plot

In the Constellation scatter plot, the values of response will be calculated between the x-axis and y-axis in the XY plot. In this plot Y axis has the minimum value while the x-axis corresponds to minimum and maximum values as shown in figure 5.

4.4 Scope of Discrete time Scatter plot

In the Scope of Discrete time Scatter plot, is the scatter plot between In-phase amplitude and Quadrature amplitude, which shows the symmetrical response about both the in-phase amplitude and Quadrature amplitude as shown in figure 6.

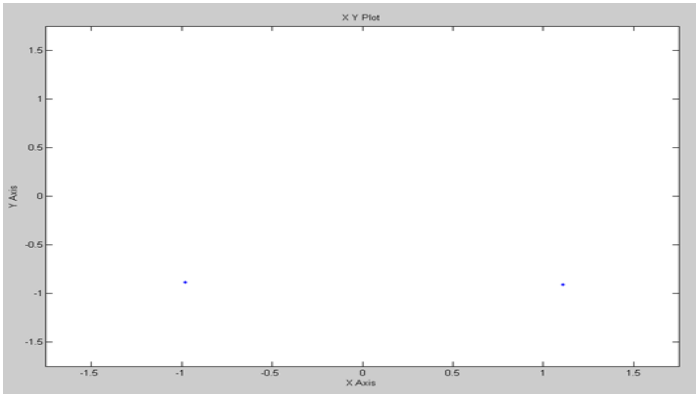

Figure 5: XY Scope of Constellation Scatter plot

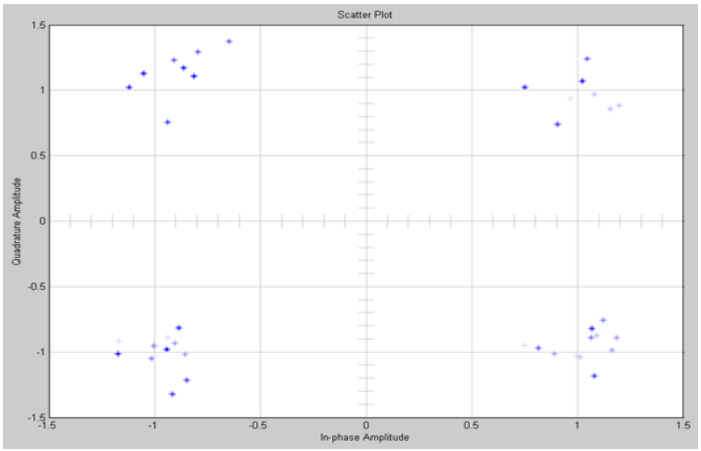

Figure 6: Scope of Discrete time Scatter plot

4.5 Scope of Interpolated output

This block has two scalar inputs. The block plots data in the first input (the *x* direction) against data in the second input (the *y* direction). This block is useful for examining limit cycles. This response is the symmetrical about both the axis.i.e. x-axis and y-axis and have the same values in the x-axis and y-axis as shown in figure 7.

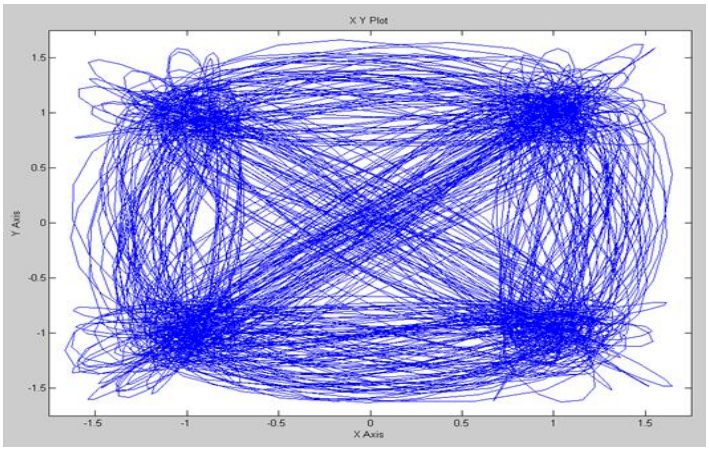

Figure 7: Scope of Interpolated output

5. CONCLUSION

In this paper a digital Costas carrier recovery loop method has been presented to remove phase ambiguity in digital receivers. The PLL based carrier recovery implementation introduces phase ambiguity which can be eliminated with the help of designed Costas loop method. The Costas loop implementation is simple and flexible. The results show phase ambiguity removal using proposed Costas loop design which results in high performance solution for wireless communication applications.

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