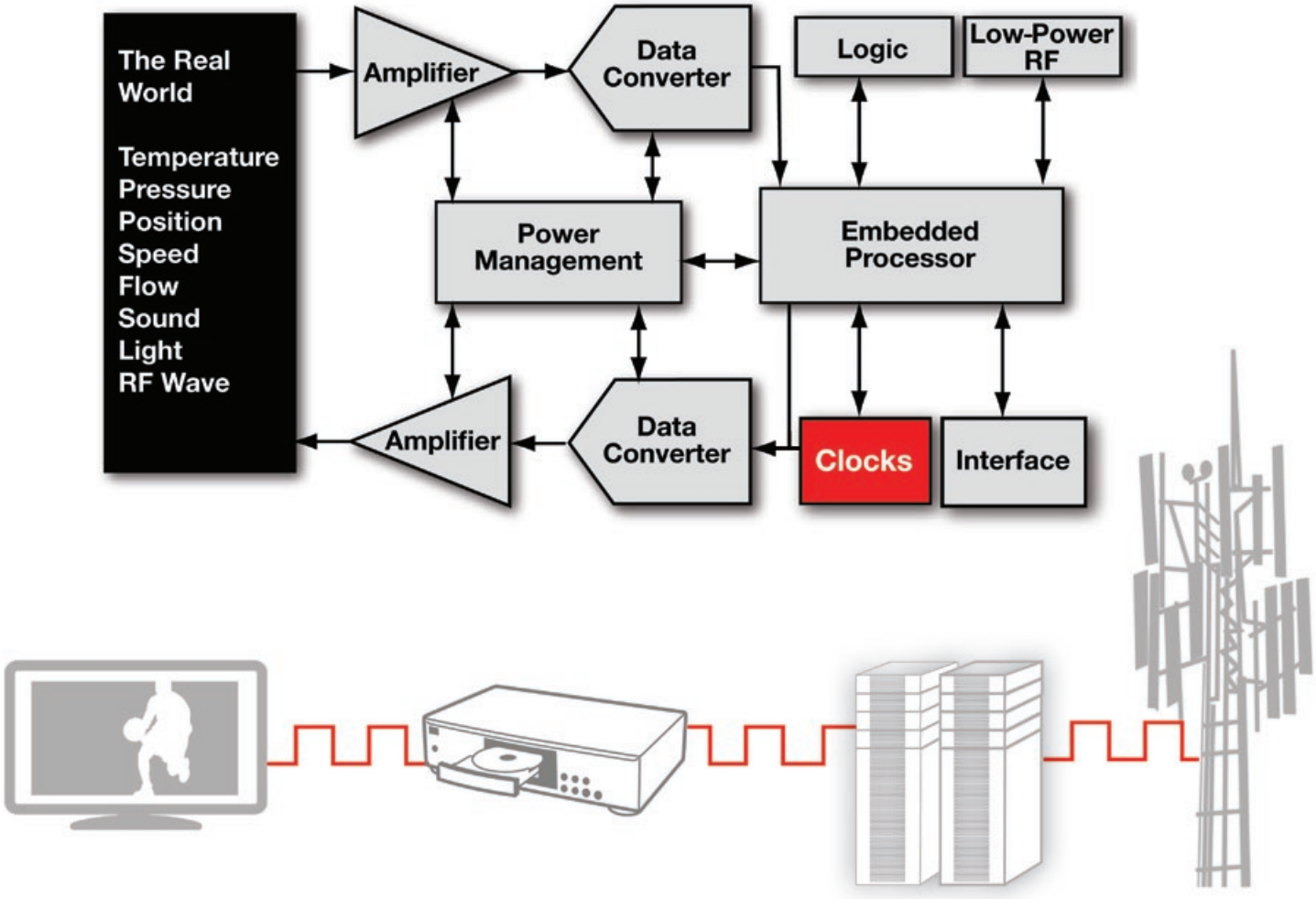
Clocks and Timing Guide

Texas Instruments



www.ti.com/clocks

4Q 2010

Clock Distribution (Fan-Out Clock Buffers, Zero-Delay Buffers)

Clock Distribution
CDCLVC11xx

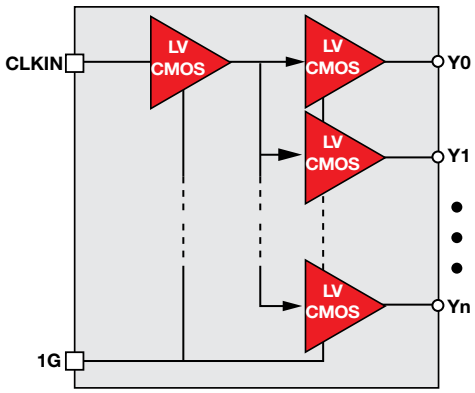
NEW

Get samples and datasheets at: **www.ti.com/sc/device/CDCLVC11xx**

Key Features
- Family of high-performance 1:2/3/4/6/8/10/12 LVCMOS clock Fan-Out buffers
- Very low pin-to-pin skew <50ps
- Very low additive jitter <100fs RMS (12kHz to 20MHz)
- Supply voltage: 3.3V or 2.5V
- fmax = 250MHz for 3.3V
- fmax = 180MHz for 2.5V
- Operating temperature range: –40°C to +85°C
- Available in 8-, 14-, 16-, 20-, 24-pin TSSOP package (all pin-compatible)

Applications
- General purpose communication, Industrial and consumer applications

The **CDCLVC11xx** is a modular, high-performance, low-skew, general-purpose clock buffer family designed with a modular approach in mind. There are 7 different Fan-Out variations, (1:2 to 1:12) available. All of the devices are pin- compatible to each other for easy handling. All family members share the same high-performing characteristics like low additive jitter, low skew and wide operating temperature range. The CDCLVC11xx supports an asynchronous output enable control (1G) that switches the outputs into a low state when 1G is low.



CDCLVC11xx functional block diagram

Clock Distribution
CDCLVD12xx/21xx

NEW

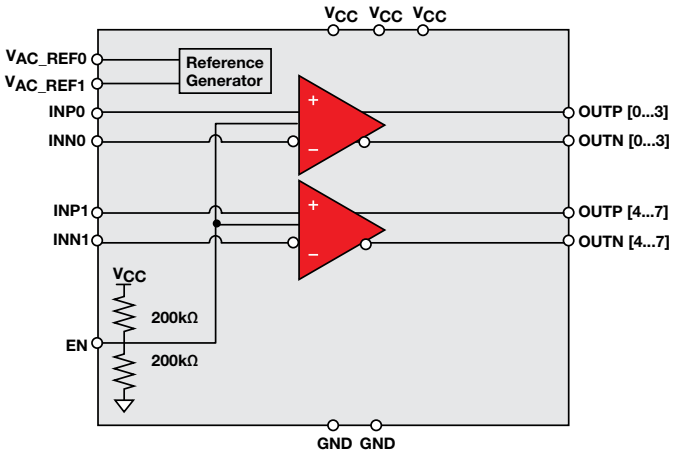
Get samples and datasheets at: **www.ti.com/sc/device/CDCLVD12xx/21xx**

Key Features
- Family of high-performance 2:4/8/12/16 or dual 1:2/4/6/8 universal-to-LVDS clock Fan-Out buffers
- Very low additive jitter <300fs RMS (10kHz-20MHz)
- Low output skew of 20ps (max)
- Universal inputs accept LVDS, LVPECL and LVCMOS
- Selectable clock inputs – control pin
- LVDS outputs, ANSI EAI/TIA-644A standard-compatible
- Clock frequency up to 800MHz
- 2.375V to 2.625V device power supply
- LVDS ref voltage, VAC_REF, available for capacitive coupled inputs
- Industrial temp range: –40°C to +85°C

Applications
- Telecommunications/networking
- Medical imaging
- Test and measurement equipment
- Wireless communications
- General-purpose clocking

The CDCLVD12xx/21xx clock buffers distribute one or two selectable clock inputs, (IN0, IN1), to 4, 8, 12 or 16 pairs of differential LVDS clock outputs (OUT0, OUT3) with minimum skew for clock distribution. The buffers can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL or LVCMOS.

The CDCLVD12xx/21xx are specifically designed for driving 50 transmission lines. When driving the inputs in single-ended mode, the appropriate bias voltage (VAC_REF) should be applied to the unused negative input pin.



CDCLVD12xx/21xx functional block diagram

Clock Distribution (Fan-Out Clock Buffers, Zero Delay Buffers)

Clock Distribution
CDCLVP12xx/21xx

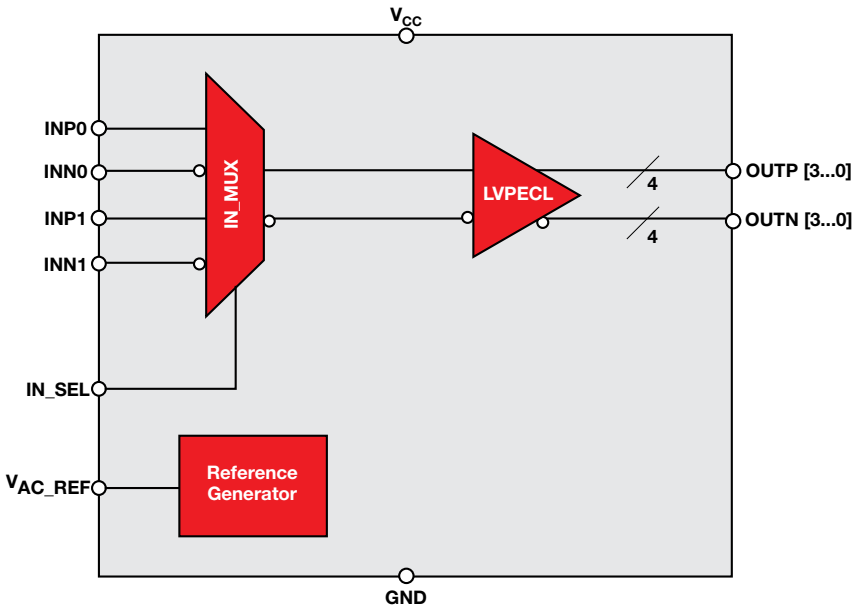
NEW

Get samples and datasheets at: **www.ti.com/sc/device/CDCLVP12xx/21xx**

Key Features
- Family of high-performance 2:4/8/12/16 or dual 1:2/4/6/8 universal-to-LVPECL clock Fan-Out buffers
- Universal inputs accept LVPECL, LVDS and LVCMOS/LVTTL
- Maximum clock frequency: 2GHz
- Very low additive jitter <100fs RMS (10kHz-20MHz)
- 2.375-V to 3.6-V device power supply
- Low output skew of 30ps (max)
- LVPECL reference voltage, V_{AC}_REF
- Available for capacitive-coupled inputs
- Industrial temperature range: –40°C to +85°C

Applications
- Wireless communications
- Telecommunications/networking
- Medical imaging
- Test and measurement equipment

The CDCLVP12xx/21xx are highly versatile, low additive jitter buffers that can generate up to 16 copies of LVPECL clock outputs from one of two selectable LVPECL, LVDS or LVCMOS inputs for a variety of communication applications. The devices have a maximum clock frequency up to 2GHz. The CDCLVP12xx/21xx feature an on-chip multiplexer (MUX) for selecting one of two inputs that can be easily configured solely through a control pin. The overall additive jitter performance is <100fs RMS (10kHz to 20MHz) and overall output skew is as low as 30ps, making the device a perfect choice for use in demanding applications.



CDCLVP12xx/21xx functional block diagram

Clock Distribution (Fan-Out Clock Buffers, Zero-Delay Buffers)

Clock Distribution

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Propagation Delay	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Fan-Out Clock Buffers (Non-PLL)										
Differential-Ended										
CDCLVP1102	Low-Jitter 1:2 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	10ps	–40 to 85	QFN-16	2.50
CDCLVP1204	Low-Jitter, 2-Input Selectable 1:4 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	15ps	–40 to 85	QFN-16	3.30
CDCLVP1208	Low-Jitter, 2-Input Selectable 1:8 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	20ps	–40 to 85	QFN-28	5.00
CDCLVP1212	Low-Jitter, 2-Input Selectable 1:12 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	25ps	–40 to 85	QFN-40	6.50
CDCLVP1216	Low-Jitter, 2-Input Selectable 1:16 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	30ps	–40 to 85	QFN-48	8.50
CDCLVP2102	Low-Jitter, Dual 1:2 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	10ps (within bank)	–40 to 85	QFN-16	3.30
CDCLVP2104	Low-Jitter, Dual 1:4 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	15ps (within bank)	–40 to 85	QFN-28	5.00
CDCLVP2106	Low-Jitter, Dual 1:6 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	20ps (within bank)	–40 to 85	QFN-40	6.50
CDCLVP2108	Low-Jitter, Dual 1:8 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	25ps (within bank)	–40 to 85	QFN-48	8.50
CDCLVD1204	Low-Jitter, 2-Input Selectable 1:4 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	–40 to 85	QFN-16	2.85
CDCLVD1208	Low-Jitter, 2-Input Selectable 1:8 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	–40 to 85	QFN-28	3.85
CDCLVD1212	Low-Jitter, 2-Input Selectable 1:12 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	–40 to 85	QFN-40	4.75
CDCLVD1216	Low-Jitter, 2-Input Selectable 1:16 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	–40 to 85	QFN-48	5.70
CDCLVD2102	Low-Jitter, Dual 1:2 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	–40 to 85	QFN-16	3.00
CDCLVD2104	Low-Jitter, Dual 1:4 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	–40 to 85	QFN-28	4.00
CDCLVD2106	Low-Jitter, Dual 1:6 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	–40 to 85	QFN-40	5.00
CDCLVD2108	Low-Jitter, Dual 1:8 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	–40 to 85	QFN-48	6.00
CDCLVD1213	Low-Jitter, 1:4 Universal-to-LVDS Buffer with Selectable Output Divider	LVPECL/LVDS/CML	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	–40 to 85	QFN-16	4.00
CDCP1803	1:3 LVPECL Clock Buffer with Programmable Divider	LVPECL/LVDS	LVPECL	0 to 800	3.3	320 to 600ps	30ps	–40 to 85	QFN-24	3.15
CDCLVP215	Dual 1:5 High-Speed LVPECL Clock Buffer	LVPECL	LVPECL	DC to 3.5GHz	2.5/3.3	230 to 370ps	30ps	–40 to 85	LQFP-32	5.55
CDCLVP110	1:10 LVPECL Clock Buffer	LVPECL/HSTL	LVPECL	0 to 3.5GHz	2.5/3.3	230 to 370ps	30ps	–40 to 85	LQFP-32	5.50
CDCLVP111	1:10 LVPECL Clock Buffer with Selectable Input	LVPECL	LVPECL	DC to 3.5GHz	2.5/3.3	230 to 370ps	30ps	–40 to 85	LQFP-32/QFN-32	5.55
CDCLVD110A	Programmable 1:10 LVDS Clock Buffer	LVDS	LVDS	0 to 900	2.5	3ns	30ps (typ)	–40 to 85	TQFP-32	5.50
CDCL1810	1:10 LVDS-to-CML Clock Buffer	LVDS	CML	0 to 650	1.8	3ns	64ps	–40 to 85	QFN-48	6.45
SN65EL11	1:2 ECL/PECL Buffer	ECL/PECL	ECL/ PECL	>2.5GHz	5	265ps (typ)	15	–40 to 85	SOIC-8/MSOP-8	1.35
SN65EL16	1:1 ECL/PECL Buffer	ECL/PECL	ECL/ PECL	>2.5GHz	5	250ps (typ)	20	–40 to 85	SOIC-8/MSOP-8	1.35
SN65ELT20	1:1 TTL-to-PECL Buffer	TTL	PECL	400 (Typ)	5	1250ps (max)	—	–40 to 85	SOIC-8/MSOP-8	1.45
SN65ELT21	1:1 PECL-to-TTL Buffer	TTL	PECL	0 to 400	5	3000ps (typ)	—	–40 to 85	SOIC-8/MSOP-8	1.40
SN65ELT22	2:2 TTL-to-PECL Buffer	TTL	PECL	0 to 1GHz	5	1100ps (max)	90	–40 to 85	SOIC-8/MSOP-8	1.45
SN65ELT23	2:2 PECL-to-TTL Buffer	PECL	TTL	0 to 500	5	3500ps (typ)	—	–40 to 85	SOIC-8/MSOP-8	1.40
SN65EPT21	1:1 LVTTL-to-LVPECL Buffer	LVTTL	LVPECL	0 to 600	3.3	1900ps (max)	250	–40 to 85	SOIC-8/MSOP-8	1.80
SN65EPT22	2:2 LVTTL-to-LVPECL Buffer	LVTTL	LVPECL	0 to 4GHz	3.3	420ps (typ)	50	–40 to 85	SOIC-8/MSOP-8	1.80
SN65EPT23	2:2 LVPECL-to-LVTTL Buffer	LVPECL	LVTTL	>300	3.3	1900ps (max)	110	–40 to 85	SOIC-8/MSOP-8	1.80

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Clock Distribution (Fan-Out Clock Buffers, Zero-Delay Buffers)

Clock Distribution (continued)

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Propagation Delay	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Fan-Out Clock Buffers (Non-PLL)										
Differential-Ended										
SN65EPT21	1:1 LVTTL-to-LVPECL Buffer	LVTTL	LVPECL	0 to 600	3.3	1900ps (max)	250	–40 to 85	SOIC-8/MSOP-8	1.80
SN65EPT22	2:2 LVTTL-to-LVPECL Buffer	LVTTL	LVPECL	0 to 4GHz	3.3	420ps (typ)	50	–40 to 85	SOIC-8/MSOP-8	1.80
SN65EPT23	2:2 LVPECL-to-LVTTL Buffer	LVPECL	LVTTL	>300	3.3	1900ps (max)	110	–40 to 85	SOIC-8/MSOP-8	1.80
SN65LVEL11	1:2 ECL/PECL Buffer	ECL/PECL	ECL/ PECL	0 to 1.5GHz	3.3	265ps (typ)	18	–40 to 85	SOIC-8/MSOP-8	1.45
SN65LVELT22	2:2 LVTTL-to-LVPECL Buffer	LVTTL	LVPECL	0 to 3.5GHz	3.3	450ps (typ)	50	–40 to 85	SOIC-8/MSOP-8	1.45
SN65LVELT23	2:2 LVPECL-to-LVTTL Buffer	LVPECL	LVTTL	>180	3.3	2200ps (max)	150	–40 to 85	SOIC-8/MSOP-8 SOIC-8/MSOP-8	2.30
SN65LVEP11	1:2 ECL/PECL Buffer	ECL/PECL	ECL/ PECL	0 to 3GHz	2.5/3.3	240ps (typ)	15	–40 to 85	SOIC-8/MSOP-8	2.20
Single-Ended										
CDC3RL02	1:2 Square/Sine-to-Square Wave Buffer with LDO	SINE/SQUARE	SQUARE	10 to 52	1.8	12ns (typ)	500ps	–40 to 85	DSBGA-8	0.90
CDC3S04	1:4 Sine-to-Sine Wave Buffer with LDO	SINE	SINE	.01 to 52	1.8	3ns (max)	50ps	–30 to 85	DSBGA-20	1.80
CDCLVC1102	Low-Jitter, 1:2 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	–40 to 85	TSSOP-8	0.90
CDCLVC1103	Low-Jitter, 1:3 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	–40 to 85	TSSOP-8	1.05
CDCLVC1104	Low-Jitter, 1:4 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	–40 to 85	TSSOP-8	1.20
CDCLVC1106	Low-Jitter, 1:6 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	–40 to 85	TSSOP-14	1.50
CDCLVC1108	Low-Jitter, 1:8 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	–40 to 85	TSSOP-16	1.80
CDCLVC1110	Low-Jitter, 1:10 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	–40 to 85	TSSOP-20	2.25
CDCLVC1112	Low-Jitter, 1:12 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2 ns	50ps	–40 to 85	TSSOP-24	2.60
CDC318A	1:18 LVTTL Clock Buffer with I^2C Control	LVTTL	LVTTL	0 to 100	3.3	1.2 to 4.5ns	250ps	0 to 70	SSOP-48	2.10
CDC319	1:10 LVTTL Clock Buffer with I^2C Control	LVTTL	LVTTL	0 to 140	3.3	1.2 to 3.6ns	250ps	0 to 70	SSOP-28	1.75
CDCV304	1:4 PCI-X Compliant LVTTL Clock Buffer	LVTTL	LVCMOS	0 to 200	2.5/3.3	1.8 to 3.0ns	100ps	–40 to 85	TSSOP-8	1.20
CDCVF310	1:10 LVTTL Clock Buffer (2 banks of 5 outputs)	LVTTL/LVCMOS	LVTTL/ LVCMOS	0 to 200	2.5/3.3	1.0 to 2.8ns (V_{DD} = 3. V), 1.3 to 4.0ns (V_{DD} = 2.5 V)	150ps at 3.3V, 230ps at 2.5V	–40 to 85	TSSOP-24	2.05
CDCVF2310	1:10 LVTTL Clock Buffer (2 banks of 5 outputs) with 25Ω input resistors	LVTTL/LVCMOS	LVTTL/ LVCMOS	0 to 170 (V_{DD} = 2.5V), 0 to 200 (V_{DD} = 3.3 V)	2.5/3.3	1.3 to 2.8ns (V_{DD} = 3.3 V), 1.5 to 3.5ns (V_{DD} = 2.5 V)	100ps at 3.3V, 170ps at 2.5V	–40 to 85	TSSOP-24	2.05
Mixed: Differential and Single-Ended										
CDCM1804	1:3 LVPECL + 1:1 LVCMOS Buffer with Dividers	LVPECL	LVPECL/ LVCMOS	800	3.3	600ps (LVPECL), 2.6ns (LVCMOS)	30ps (LVPECL), 1.6ns (LVCMOS)	–40 to 85	QFN-24	5.90
CDCM1802	1:1 LVCMOS + 1:1 LVPECL Buffer with Dividers	LVPECL	LVPECL/ LVCMOS	800	3.3	600ps (LVPECL), 2.6ns (LVCMOS)	1.6ns (typ)	–40 to 85	QFN-16	4.70
CDCE18005	3:5 LVPECL/LVDS/LVCMOS Buffer with Dividers	LVPECL/LVDS/ LVCMOS	LVPECL/ LVDS/ LVCMOS	DC to 1.5GHz	3.3	4ns	75ps	–40 to 85	QFN-48	6.00

**Suggested resale price in U.S. dollars in quantities of 1,000.*

*New devices are listed in **bold red.***

Clock Distribution (Fan-Out Clock Buffers, Zero-Delay Buffers)

Clock Distribution (continued)

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Char. Temp. (°C)	Package(s)	Price*
Zero-Delay Buffers (PLL-Based)										
Differential-Ended										
CDCV850	1:10 Differential Clock Driver	SSTL_2/ Universal	SSTL_2	60 to 140	2.5	C-C: ±30ps (100 to 133MHz)	–80/150ps (133MHz)	–40 to 85	TSSOP-48	2.20
CDCV855	1:4 Differential Clock Driver	SSTL_2/LVTTL	SSTL_2	60 to 180	2.5	C-C: ±50ps (100 to 180MHz)	±100ps (100 to 180MHz)	–40 to 85	TSSOP-28	1.15
CDCV857	1:10 PLL Differential Clock Driver for DDR 200/266/333, SSC	SSTL_2/LVTTL	SSTL_2	60 to 200	2.5	C-C: ±75ps (100 to 200MHz)	–150/50ps (200MHz)	0 to 85	TSSOP-48	4.20
CDCV857A	1:10 PLL Differential Clock Driver for DDR 200/266/333, SSC	SSTL_2/LVTTL	SSTL_2	60 to 180	2.5	C-C: ±50ps (100 to 180MHz)	±100ps (100 to 180MHz)	0 to 85	TSSOP-48, µBGA-56	2.90
CDCV857B	1:10 PLL Differential Clock Driver for DDR 200/266/333, SSC	SSTL_2/LVTTL	SSTL_2	60 to 200	2.5	C-C: ±50ps (100 to 200MHz)	±50ps (min/max) (100 to 200MHz)	0 to 70	TSSOP-48, µBGA-56	3.65
CDCV857BI	1:10 PLL Differential Clock Driver for DDR 200/266/333, SSC	SSTL_2/LVTTL	SSTL_2	60 to 200	2.5	C-C: ±50ps (100 to 200MHz)	±50ps (min/max) (100 to 200MHz)	–40 to 85	TSSOP-48, µBGA-56	3.35
CDCVF857	1:10 PLL Differential Clock Driver for DDR 200/266/333/400, SSC	SSTL_2/LVTTL	SSTL_2	60 to 220	2.5	C-C: ±35ps (133 to 200MHz)	±50ps (min/max) (100 to 200MHz)	–40 to 85	TSSOP-48, QFN-48, µBGA-56	3.60
CDCU877	1:10 PLL Differential Clock Driver for DDR2 Applications, SSC	SSTL_18	SSTL_18	10 to 400	1.8	C-C: ±30ps (190 to 340MHz)	±50ps	–40 to 85	µBGA-52, QFN-40	3.05
CDCU877A	1:10 PLL Differential Clock Driver for DDR2 Applications, SSC	SSTL_18	SSTL_18	10 to 400	1.8	C-C: ±30ps (190 to 340MHz)	±50ps	–40 to 85	µBGA-52, QFN-40	3.05
CDCU877B	1:10 PLL Differential Clock Driver for DDR2 400/533, SSC	SSTL_18	SSTL_18	10 to 340	1.8	C-C: ±30ps (190 to 340MHz)	±50ps	–40 to 85	µBGA-52	3.05
CDCUA877	1:10 PLL Differential Clock Driver for DDR2 400~800, SSC, 8-mA Output	SSTL_18	SSTL_18	125 to 410	1.8	C-C: ±40ps (200 to 333MHz)	±50ps	–40 to 85	µBGA-52	3.35
CDCU2A877	1:10 PLL Differential Clock Driver for DDR2 400~800, SSC, 16-mA Output	SSTL_18	SSTL_18	125 to 410	1.8	C-C: ±40ps (160 to 410MHz)	±50ps	0 to 70	µBGA-52	3.05
Single-Ended										
CDCVF2505	1:5 PLL Clock Driver for SDR/ PC133+, SSC	LVTTL	LVTTL	24 to 200	3.3	C-C: l70lps (typ) (66 to 200MHz)	±150ps (66 to 200MHz)	–40 to 85	TSSOP-8, SOIC-8	0.95
CDCVF2509A	1:9 PLL Clock Driver for SDR/ PC133+, SSC	LVTTL	LVTTL	50 to 175	3.3	C-C: l65lps (typ) (100 to 166MHz)	±125ps (66 to 166MHz)	0 to 85	TSSOP-24	3.90
CDCVF2510A	1:10 PLL Clock Driver for SDR/ PC133+, SSC	LVTTL	LVTTL	50 to 175	3.3	C-C: l65lps (typ) (100 to 166MHz)	±125ps (66 to 166MHz)	0 to 85	TSSOP-24	2.60

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Clock Generation (Crystal Oscillator Replacements, Jitter Cleaners)

Clock Generator/Jitter Cleaner with Integrated Dual VCO
CDCE6200x

Get samples and datasheets at: **www.ti.com/sc/device/CDCE6200x**

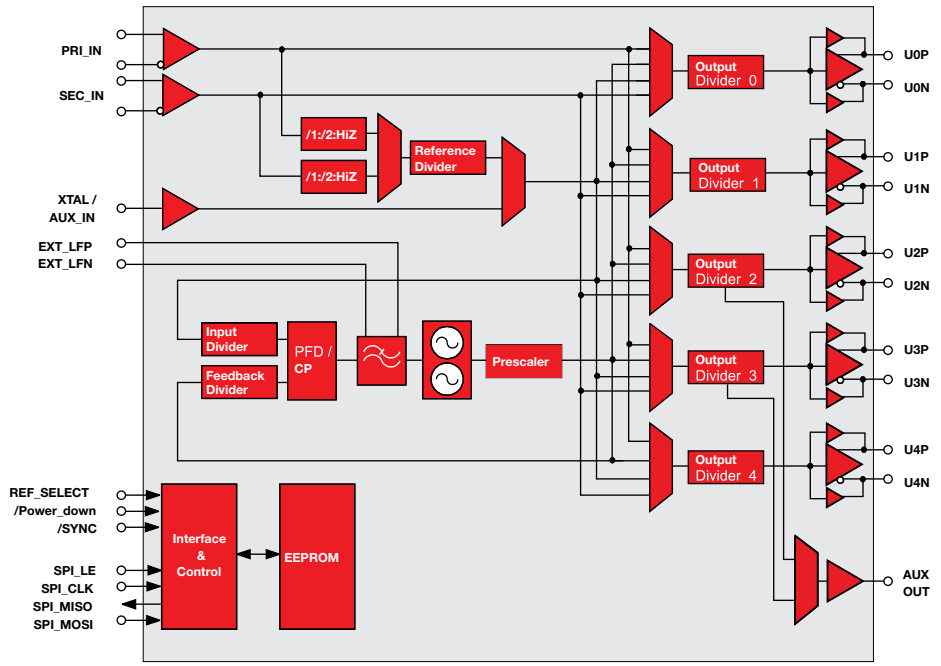
Key Features

- Fully integrated synthesizer – PLL, VCO, partially integrated loop filter
- Two universal (LVPECL/LVDS/LVCMOS inputs), one auxiliary/XTAL input
- Up to 5 fully configurable outputs up to 1.175GHz (LVPECL, LVDS or 2-LVCMOS)
- Integrated RMS jitter <500fs (10kHz-20MHz)
- On-chip EEPROM determines default state at power-up; fully programmable via SPI port

Applications

- Data converter and data aggregation clocking
- Wireless infrastructure
- Switches and routers
- Medical electronics
- Military and aerospace
- Industrial
- Clock generation and jitter cleaning

The CDCE6200x is a high-performance clock generator and distributor featuring low output jitter, a high degree of configurability via a SPI interface and programmable start-up modes determined by on-chip EEPROM. Specifically tailored for clocking data converters and high-speed digital signals, the CDCE6200x achieves jitter performance <1ps RMS jitter (10kHz to 20MHz). It incorporates a synthesizer block with partially integrated loop filter, a clock distribution block including programmable output formats and an input block featuring an innovative smart multiplexer. The clock distribution block includes up to five individually programmable outputs that can be configured to provide different combinations of output formats (LVPECL, LVDS, LVCMOS).



CDCE62005 functional block diagram

Clock Generation (Crystal Oscillator Replacements, Jitter Cleaners)

Clock Oscillator Replacements

CDCE9xx

Get samples and datasheets at: **www.ti.com/sc/device/CDCE9xx**

Key Features

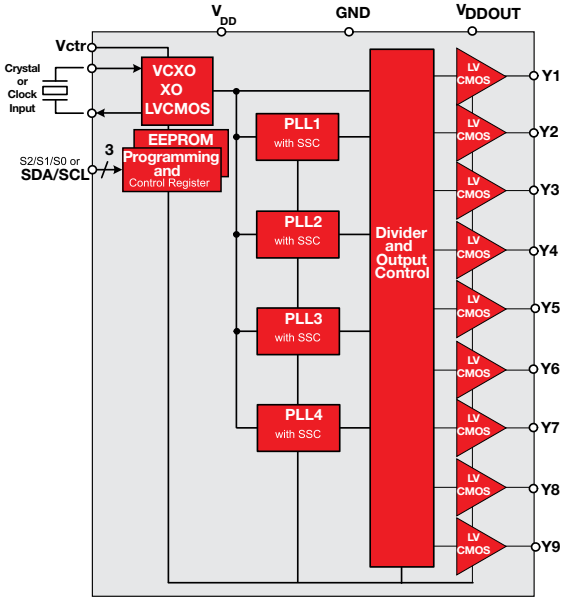
- Fully programmable clock synthesizer with 3.3V/2.5V/1.8V I/Os
- Up to 4 internal fractional PLLs enable 0-PPM clock generation
- Up to 9 low-jitter, low-skew LVCMOS outputs up to 230MHz
- Flexible input clocking concept
  - External crystal: 8MHz to 32MHz
  - On-chip VCXO: pull-range ±150ppm
  - Single-ended LVCMOS up to 160MHz

Applications

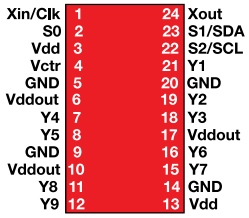
- D-TV, HD-TV, STB, IP-STB, DVD-players, DVD recorders, printers
- General-purpose frequency synthesizing
- DSP, DaVinci™ and OMAP™ attach audio and video clocking

The CDCE(L)9xx are modular PLL-based low-cost, high-performance, programmable clock generators/synthesizers. They generate up to 9 output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230MHz, using up to four independent configurable PLLs.

The CDCE9xx have separate output supply pins for V_{DD}OUT 2.5V and 3.3V, whereas the CDCEL9xx supports 1.8V. The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20pF. Additionally, an on-chip VCXO is selectable, allowing synchronization of the output frequency to an external control (PWM) signal.



CDCE949 functional block diagram



Clock Generation (Crystal Oscillator Replacements, Jitter Cleaners)

Clock Oscillator Replacements

CDCM6100x

Get samples and datasheets at: **www.ti.com/sc/device/CDCM6100x**

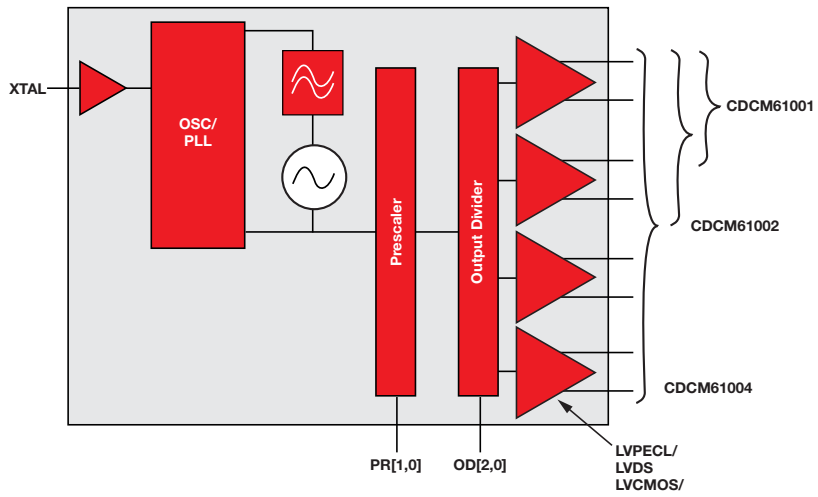
Key Features

- Input frequency range: 21.875MHz to 28.47MHz
- Output frequency range: 43.75MHz to 683.264MHz
- Device settings managed through a control pin structure (prescaler and feedback divider, output divider, output type)
- Supports common frequencies utilized in datacom, telecom and consumer applications
- Low-jitter outputs <1ps RMS (10kHz to 20MHz), ~25ps pk-pk

Applications

- Precision clock generator for:
  - Datacom/telecom/networking
  - Wireless infrastructure
  - High-frequency, high-cost XO replacement

The CDCM6100x is a highly versatile, low-jitter frequency synthesizer that can generate up to four low-jitter clock outputs (selectable between LVPECL, LVDS or LVCMOS outputs) from a low-frequency crystal input for a variety of wireline and data communication applications. The CDCM6100x features an onboard PLL that can be easily configured solely through control pins. The overall output random jitter performance is <1ps RMS (10kHz-20MHz), making this device a perfect choice for use in demanding applications such as SNET, Ethernet, Fibre Channel and SAN.



CDCM6100x functional block diagram

Clock Generation

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Crystal Oscillator (XO) Replacements – Differential-Ended											
CDCE421A	Flexible Low-Jitter Clock Generator, 10MHz to 1.1GHz	Crystal/ LVCMOS	LVDS/LVPECL	11 to 1100	3.3	—	<1ps rms	—	–40 to 85	Die/QFN-24	7.10
CDC421A100	Low-Jitter 100MHz Clock Generator for PCI Express	Crystal/ LVCMOS	LVPECL	100	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00
CDC421A106	Low-Jitter 106.25MHz Clock Generator for Fibre Channel	Crystal/ LVCMOS	LVPECL	106.25	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00
CDC421A125	Low-Jitter 125MHz Clock Generator for Ethernet	Crystal/ LVCMOS	LVPECL	125	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00
CDC421A156	Low-Jitter 156.25MHz Clock Generator for 10G Ethernet	Crystal/ LVCMOS	LVPECL	156.25	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00
CDC421A212	Low-Jitter 212.5MHz Clock Generator for Fibre Channel	Crystal/ LVCMOS	LVPECL	212.5	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00
CDC421A250	Low-Jitter 250MHz Clock Generator for PCI Express	Crystal/ LVCMOS	LVPECL	250	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00
CDC421A312	Low-Jitter 312.5MHz Clock Generator for 10G Ethernet	Crystal/ LVCMOS	LVPECL	312.5	3.3	—	<1ps rms	—	–40 to 85	QFN-24	7.00

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Clock Generation (Crystal Oscillator Replacements, Jitter Cleaners)

Clock Generation (continued)

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Jitter (Peak-to-Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)	Price*
Crystal Oscillator (XO) Replacements - Single Ended											
CDCE913	1.8V Programmable 1-PLL, 3 Output Clock Synthesizer with 2.5/3.3V Outputs	Crystal/ LVCMOS	2.5/3.3V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-14	1.60
CDCEL913	1.8V Programmable 1-PLL, 3 Output Clock Synthesizer with 1.8V Outputs	Crystal/ LVCMOS	1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-14	1.60
CDCE925	1.8V Programmable 2-PLL, 5 Output Clock Synthesizer with 2.5/3.3V Outputs	Crystal/ LVCMOS	2.5/3.3V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-16	1.95
CDCEL925	1.8V Programmable 2-PLL, 5 Output Clock Synthesizer with 1.8V Outputs	Crystal/ LVCMOS	1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-16	1.80
CDCE937	1.8V Programmable 3-PLL, 7 Output Clock Synthesizer with 2.5/3.3V Outputs	Crystal/ LVCMOS	2.5/3.3V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-20	2.15
CDCEL937	1.8V Programmable 3-PLL, 7 Output Clock Synthesizer with 1.8V Outputs	Crystal/ LVCMOS	1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-20	2.15
CDCE949	1.8V Programmable 4-PLL, 9 Output Clock Synthesizer with 2.5/3.3V Outputs	Crystal/ LVCMOS	2.5/3.3V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-24	2.35
CDCEL949	1.8V Programmable 4-PLL, 9 Output Clock Synthesizer with 1.8V Outputs	Crystal/ LVCMOS	1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	—	150	–40 to 85	TSSOP-24	2.35
CDCE706	3.3V Programmable 3-PLL, 6 Output Clock Synthesizer	Crystal/ LVCMOS/ Differential	2.5/3.3V LVCMOS	0 to 300	3.3	60ps (typ)	—	200	–40 to 85	TSSOP-20	3.85
CDCE906	3.3V Programmable 3-PLL, 6 Output Clock Synthesizer	Crystal/ LVCMOS/ Differential	2.5/3.3V LVCMOS	0 to 167	3.3	60ps (typ)	—	200	0 to 70	TSSOP-20	2.20
CDCS501	1:1 Spread Spectrum Clock Generator	LVCMOS	3.3V LVCMOS	40 to 108	3.3	110ps (typ)	—	—	–40 to 85	TSSOP-8	0.45
CDCS502	1:1 Clock Generator with Optional SSC	Crystal	3.3V LVCMOS	8 to 108	3.3	100ps (typ)	—	—	–40 to 85	TSSOP-8	0.95
CDCS503	1:1 Clock Buffer/Multiplier with Optional SSC	LVCMOS	3.3V LVCMOS	8 to 108	3.3	110ps (typ)	—	—	–40 to 85	TSSOP-8	0.50
Mixed: Differential and Single-Ended											
CDCM61001	1:1 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS	LVPECL/ LVDS/2-LVCMOS	43.75 to 683.28; LVCMOS up to 250MHz	3.3	<1ps rms	—	—	–40 to 85	QFN-32	4.20
CDCM61002	1:2 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS	LVPECL/ LVDS/2-LVCMOS	43.75 to 683.28; LVCMOS up to 250MHz	3.3	<1ps rms	—	50	–40 to 85	QFN-32	5.00
CDCM61004	1:4 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS	LVPECL/ LVDS/2-LVCMOS	43.75 to 683.28; LVCMOS up to 250MHz	3.3	<1ps rms	—	60	–40 to 85	QFN-32	6.50
CDCE62002	2:2 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS/ Differential	LVPECL/ LVDS/2-LVCMOS	4.25 to 1175	3.3	<1ps rms	—	75	–40 to 85	QFN-32	6.60
CDCE62005	3:5 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS/ Differential	LVPECL/ LVDS/2-LVCMOS	4.25 to 1175	3.3	<1ps rms	—	75	–40 to 85	QFN-48	7.50
Jitter Cleaners – Internal VCO											
CDCE62002	2:2 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS/ Differential	LVPECL/ LVDS/2-LVCMOS	4.25 to 1175	3.3	<1ps rms	—	75	–40 to 85	QFN-32	6.60
CDCE62005	3:5 Low-Jitter, Integrated VCO Clock Generator	Crystal/ LVCMOS/ Differential	LVPECL/ LVDS/2-LVCMOS	4.25 to 1175	3.3	<1ps rms	—	75	–40 to 85	QFN-48	7.50
CDCL6010	1:10 LVDS-to-CML Jitter Cleaner and Distributor	LVDS	CML	15 to 1250	1.8	<1ps rms	—	64	–40 to 85	QFN-48	8.05
Jitter Cleaners – External VCXO											
CDCM7005	2:5 Ultra-Low-Jitter Clock Synchronizer and Jitter Cleaner	LVCMOS/ LVPECL	LVCMOS/ LVPECL	0 to 1500	3.3	<1ps rms	–200/+100ps	50	–40 to 85	BGA-64/ QFN-48	9.50
CDCE72010	2:10 Ultra-Low-Jitter Clock Synchronizer and Jitter Cleaner	LVPECL/ LVDS/ LVCMOS	LVPECL/ LVDS/ LVCMOS	0 to 1500	3.3	<1ps rms	—	50	–40 to 85	QFN-64	10.95

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