Journal of Systems Engineering and Electronics Vol. 21, No. 1, February 2010, pp.20–26
Available online at www.jseepub.com

# Design and realization of synchronization circuit for GPS software receiver based on FPGA

Xiaolei Yu[1,2,*], Yongrong Sun[1], Jianye Liu[1], and Jianfeng Miao[1,3]

1. Navigation Research Center, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, P. R. China;
2. Faculty of Science and Technology, Deakin University, Geelong VIC 3217, Australia;
3. Department of Land Surveying & Geo-Informatics, Hong Kong Polytechnic University, Hong Kong, P. R. China

**Abstract:** With research on the carrier phase synchronization and symbol synchronization algorithm of demodulation module, a synchronization circuit system is designed for GPS software receiver based on field programmable gate array (FPGA), and a series of experiment is done on the hardware platform. The result shows the all-digital synchronization and demodulation of GPS intermediate frequency (IF) signal can be realized and applied in embedded real-time GPS software receiver system. It is verified that the decision-directed joint tracking algorithm of carrier phase and symbol timing for received signals from GPS is reasonable. In addition, the loop works steadily and can be used for receiving GPS signals using synchronous demodulation. The synchronization circuit for GPS software receiver designed based on FPGA has the features of low cost, miniaturization, low power and real-time. Surely, it will become one of the development directions for GPS and even GNSS embedded real-time software receiver.

**Keywords:** software receiver, synchronization circuit, field programmable gate array, GPS, joint tracking algorithm.

**DOI:** 10.3969/j.issn.1004-4132.2010.01.004

## 1. Introduction

GPS is found widely used in the fields of positioning, navigation, ranging, time service and remote sensing owing to its features of high precision and all-weather service. The international trend is toward the developments in the direction of low cost, miniaturization and low power, which is backed by a research on the software receiver based on software radio theory, and exlensive attention has been given to the problem. The software receiver gains higher flexibility, greater scalability and better compatibility while at the same time maintain the same function as the hardware receiver.

The concept of GPS software receiver was first proposed by American scholar Akos from his paper in 1996 [1]. Ever since 2000 or so, the research literatures on GPS software receiver have been found in various academic journals and conferences, and a new research field in GPS field has been gradually formed [2–7]. Henceforth, the software receiver has made rapid development with such advantages as low cost, open bottom architecture and high flexibility. In recent years, multiple studies, such as the research on the principle prototype of GPS receiver based on software radio technology, the research applied in the acquisition of weak signal and multi-path interference for GPS software receiver, the research on the new algorithm of acquisition and tracking for GPS software receiver, the research on real-time for imbedded GPS software receiver and the research on the seamless integration technology of multiple positioning system based on software receiver, have been done successively by Septentrion Company in Europe, Stanford University in U.S.A., Aalborg University in Denmark and the University of Calgary in Canada [8–11].

The research on GPS software receiver in China started around 2006, which is relatively late. The main research units are colleges associated with national defence, such as Beijing University of Aeronautics and Astronautics, Nanjing University of Aeronautics and Astronautics, National University of Defense Technology and Academy of Equipment Command & Technology etc. The research focuses on modeling and simulation of the basic algorithm for the implementation of principle prototype, still at the primary stage of the research on the GPS software receiver [12–16].

For the traditional GPS receiver, the demodulation unit is implemented by means of analog signal processing with corresponding devices, which greatly affects the real-time performance of the system. With the development of very large scale integration (VLSI), the all-digital modulation and demodulation scheme has become the trend of modern communication system for its convenience in realization

Manuscript received September 12, 2008.
*Corresponding author.
This work was supported in part by the National High Technology Research and Development Program of China (863 Program) (2006AA12A108) and CSC International Scholarship (2008104769).

and debug, high integration and reliability, and low cost.

In this paper, according to the principle of GPS receiver and modern EDA technology, and with deep research and analysis on the carrier phase synchronization and symbol synchronization algorithm in demodulation module, a synchronization circuit system was designed for GPS software receiver based on FPGA, and a series of experiment had been done on the hardware platform. The results show that the all-digital synchronization and demodulation of GPS IF signal with the frequency of 1.25 MHz can be realized and completely applied in embedded real-time GPS software receiver system.

## 2. Compositional principle of synchronization circuit for GPS software receiver

The hardware of GPS software receiver is composed of GPS satellite signal receiving antenna, RF front-end, high-speed analog-to-digital converter (ADC), FPGA chip and interface circuit. The satellite signal from GPS signal receiving antenna is amplified and added to each RF front-end by low noise amplifier (LNA), then the signal is sent to high-speed ADC by the down-conversion module in RF front-end. The functions in navigation computer such as signal synchronization, loop capture and tracking have been completed by FPGA chip. Fig. 1 shows the system composition.

The analog and digital part of demodulator has been defined by ADC, while the degree of digitalization of receiver has been determined by the position of ADC. The so-called all-digital demodulation is referred to all the work such as demodulation, synchronization completed in the digital device after the received GPS signal has been converted from analog to digital by ADC. In the all-digital demodulation, the carrier phase synchronization and timing synchronization for demodulation unit will be entirely finished in digital device, the corresponding digital form for almost all analog demodulation units and devices as digital filter (FIR or IIR), all-digital multiplier and numeric controlled oscillator (NCO) could be found. One of the key technologies of all-digital demodulation is system synchronization including the design of two loops (carrier phase synchronizer and symbol synchronizer). Fig. 2 shows the synchronization circuit for all-digital demodulation.

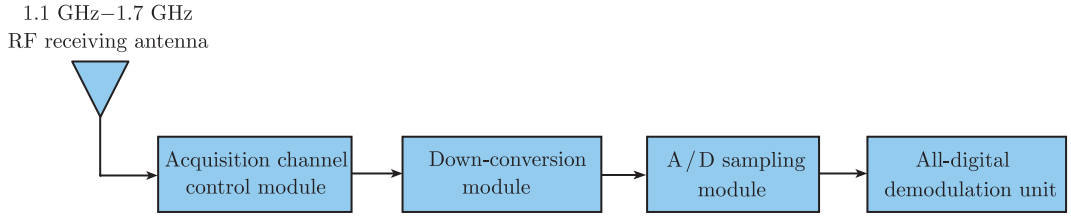



**Fig. 1 The hardware structure of GPS software receiver**

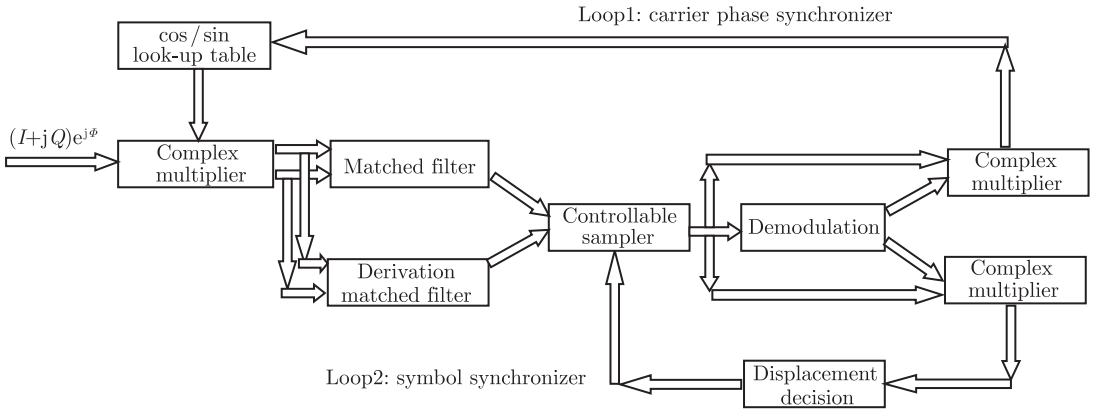



**Fig. 2 Schematic diagram of all-digital synchronization circuit system**

## 3. Carrier phase synchronizer and symbol synchronizer

In the GPS software receiver system, periodically, sampling for the output of demodulation must be done and each symbol should be sampled at every other interval for the resumption of information sending. Since the propagation delay from transmitter to receiver is unknown, the symbol timing must be derived from received signals for the synchronous sampling of demodulator output signal. Moreover, as the carrier phase offset caused by the propagation delay of transmit signal, it must be estimated by the

receiver if the detector is phase-coherent.

The clock of synchronous receiver should be synchronized with symbolic period of input signal. In the early analog demodulator shown in Fig. 3(a), the typical synchronization method is by adjusting the phase of local sampling clock with feedback loop. Usually, one sample point is extracted from each symbol period and thus the information data can be recovered. At present, with the development of VLSI technology, the demodulation is realized in all-digital way. In this demodulation unit shown in Fig. 3(b), the sampling clock is fixed and the sample point is processed for synchronization.

In this paper, clock recovery in digital method is adopted for the synchronization. The frequency source runs at a fixed rate using the crystal oscillator of high stability, while the extraction of synchronization error is computed by certain algorithm. The error signal is no longer fed back to the analog part to control the voltage controlled oscillator (VCO), but it can get the correct data point from the sampling sequence of received signals by self-adjustment and control. The adoptive synchronization module is shown in Fig. 4. The synchronization module is composed of matched filter, digital sampler, clock error extraction circuit, loop filter and controller. It can be seen from the figure that there are eight sample points in each symbol after the I, Q signals passing the matched filter and there is one sample point after passing digital sampler, then the error signal obtained from the clock error extraction circuit is sent to NCO through the loop filter, finally the synchronization is completed by the control digital sampler.

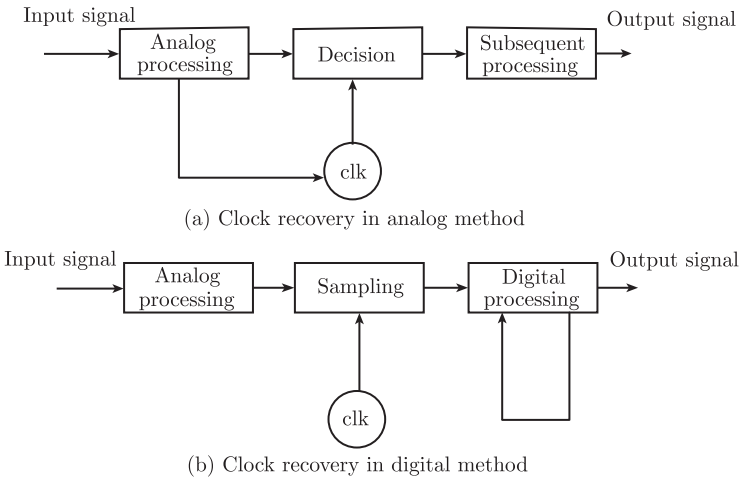



**Fig. 3 Clock recovery circuit**

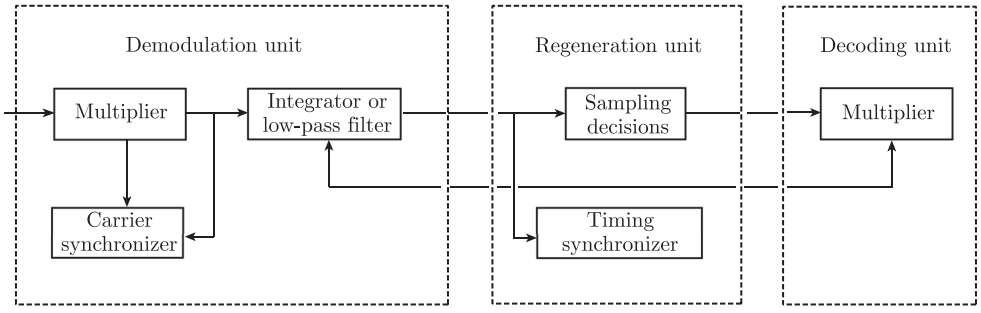



**Fig. 4 Schematic diagram of GPS signal demodulation unit**

There are many carrier recovery methods in digital demodulation, but they can mainly be divided into two types: non-decision-feedback carrier recovery and decision-feedback carrier recovery. The non-decision-feedback carrier recovery methods use square loop, Costas loop etc. For the reason that the performance of decision-feedback carrier recovery is superior to that of non-decision-feedback carrier recovery and that the received signal from GPS requiring the residual carrier phase as small as possible, the decision-feedback method is adopted for carrier recovery in all-digital demodulation. The carrier phase error may still exist after the sampled IF signal is

down-conversed to baseband signal by all-digital demodulation and this error should be eliminated by demodulator. The decision-feedback carrier recovery loop is adopted to eliminate the carrier phase error in this paper.

The estimation of carrier and symbol timing can be implemented respectively or jointly. Maximum likelihood (ML) estimation is the association of two or more signal parameter estimation, and the ML-estimated value is equal or generally even better than that obtained from optimization of each likelihood function. In other word, the variance of signal parameter obtained from the optimization of joint estimation is less than or equal to that obtained from optimization of each likelihood function.

The received signal can be assumed as

$$r(t) = \mathrm{e}^{\mathrm{j}\phi} \sum_n I_n g(t - nT - \tau) \tag{1}$$

Output signal of the correlator is

$$s(t) = \mathrm{e}^{-\mathrm{j}\hat{\phi}} \sum_n I_n g(t - nT - \hat{\tau}) \tag{2}$$

The logarithm of likelihood function of the two parameters can be expressed in equivalent type of low-pass signal as

$$\begin{aligned} \Lambda_L(\phi, \tau) = \mathrm{Re}\left[\frac{1}{N_0}\int_{T_0} r(t)s^*(t)\mathrm{d}t\right] = \\ \mathrm{Re}\left\{\frac{\mathrm{e}^{\mathrm{j}\hat{\phi}}}{N_0}\sum_n [I_n^* y_n(\tau)]\right\} \end{aligned} \tag{3}$$

Here

$$\begin{aligned} y_n(\tau) = \int_{T_0} r(t)g^*(t - nT - \hat{\tau})\mathrm{d}t = \\ I_n \mathrm{e}^{-\mathrm{j}\phi}\frac{A^2}{2}\left\{T_0 + T_0\cos\frac{2\pi}{T_0}(\tau - \hat{\tau})\right\} \end{aligned} \tag{4}$$

$$\begin{aligned} \frac{\partial y_n(\tau)}{\partial \tau} = \int_{T_0} r(t)g'^*(t - \hat{\tau})\mathrm{d}t = \\ I_n \mathrm{e}^{-\mathrm{j}\phi}\frac{A^2\pi}{4}\sin\frac{2\pi}{T}(\tau - \hat{\tau}) \end{aligned} \tag{5}$$

The necessary condition for ML-estimated values of $\phi$ and $\tau$ is

$$\frac{\partial \Lambda_l(\phi, \tau)}{\partial \phi} = 0, \quad \frac{\partial \Lambda_l(\phi, \tau)}{\partial \tau} = 0 \tag{6}$$

We can define the following equation

$$\begin{aligned} A(\tau) + \mathrm{j}B(\tau) = I_n^* y_n(\tau) = \\ |I_n|^2 \mathrm{e}^{-\mathrm{j}\phi}\frac{A^2}{2}\{T_0 + T_0\cos\frac{2\pi}{T_0}(\tau - \hat{\tau})\} \end{aligned} \tag{7}$$

Then

$$\Lambda_L(\phi, \tau) = A(\tau)\cos\phi - B(\tau)\sin\phi \tag{8}$$

The following equations can be obtained according to condition (6) of the joint ML-estimated value.

$$\begin{cases} \dfrac{\partial \Lambda_l(\phi, \tau)}{\partial \phi} = -A(\tau)\sin|\phi - B(\tau)\cos|\phi = 0 \\ \dfrac{\partial \Lambda_l(\phi, \tau)}{\partial \tau} = \dfrac{\partial A(\tau)}{\partial \tau}\cos|\phi - \dfrac{\partial B(\tau)}{\partial \tau}\sin|\phi = 0 \end{cases} \tag{9}$$

Then, for error $\phi$

$$\begin{aligned} e_\phi = |I_n|^2 \frac{A^2}{2} T_0 \sin(\hat{\phi} - \phi) \\ \hat{\phi}_2 = -ke_\phi + \hat{\phi}_1 \end{aligned} \tag{10}$$

For error $\tau$

$$\begin{aligned} e_\tau = |I_n|^2 \frac{A^2\pi}{4}\sin\left[\frac{2\pi}{T}(\tau - \hat{\tau})\right]\cos(\phi - \hat{\phi}) \\ \hat{\tau}_2 = ke_\phi + \hat{\tau}_1 \end{aligned} \tag{11}$$

Fig. 5 shows the decision-directed tracking loop for received signals from GPS which is obtained from the equations above.

## 4. System testing and result analysis

### 4.1 Test platform

In order to verify the functions of synchronization circuit for GPS software receiver, we design a signal transmitting and receiving hardware experimental platform. The main chip that adopted for the platform is Spartan3 XC3S400 (FPGA) chip designed by Xilinx Company, the peripheral chips are AD9236 (A/D), AD9767 (D/A) and RS232 etc, clock of crystal oscillator is 60 MHz. Two identical experimental circuit boards are used in the system, one is the debugging terminal (IF GPS signal simulator), which produces modulation signals, and the other is receiver, which demodulates the signals. The system hardware test platform is shown in Fig. 6. GPS IF signal with the frequency of 20.25 MHz has been generated by the debugging terminal board. After sampled with the frequency of 5 MHz, the frequency of test signal is 1.25 MHz, which will be transmitted to the receiver.

### 4.2 Doppler shift simulation

In the process of transmitting, the GPS signal will interrupted by other signals and noises such as carrier phase offset and Doppler shift. To check whether the loop can work stably, the signals are added Doppler shift and transmitted by D/A in the debugging terminal board. I/Q

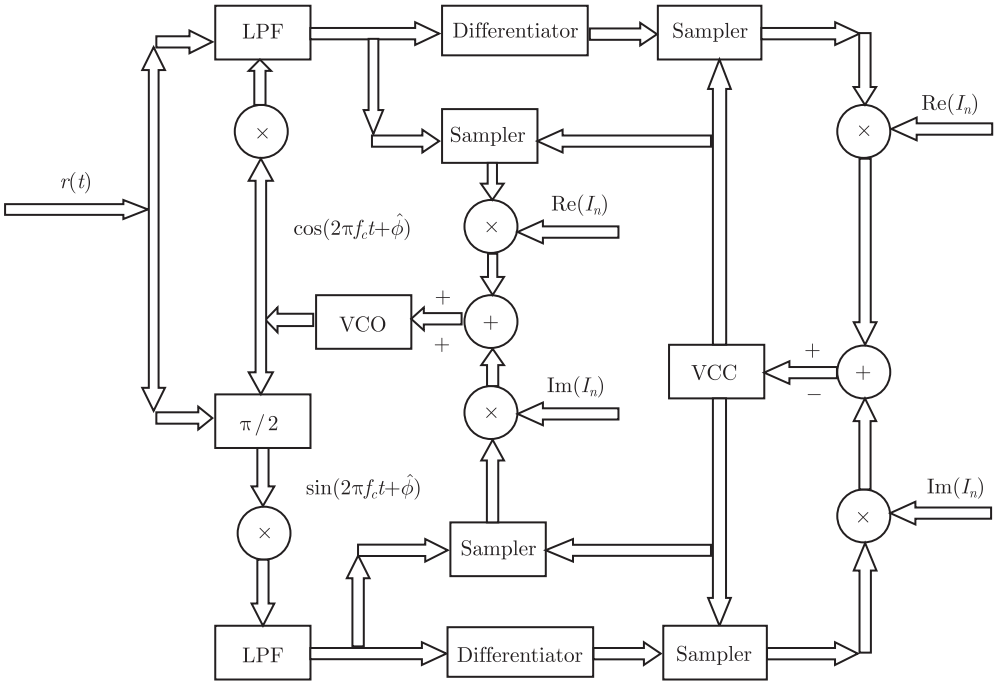



**Fig. 5 Decision-directed joint tracking loop of carrier phase and symbol timing for received signals from GPS**

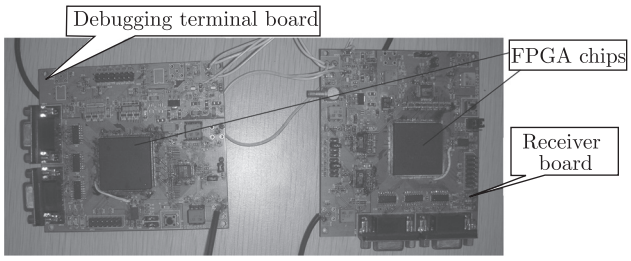
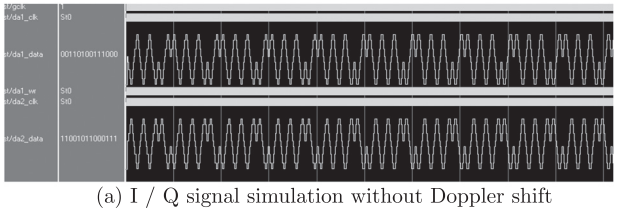
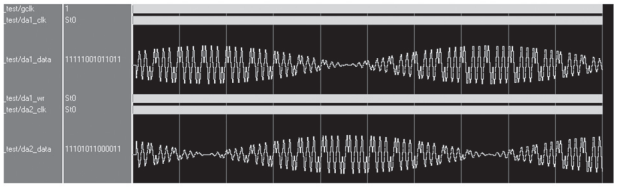



**Fig. 6 Experimental test platform**

signal transmission wave forms are shown in Fig. 7. I/Q signal simulation without Doppler shift is shown in Fig. 7(a), while I/Q signal simulation with Doppler shift is shown in Fig. 7(b).



(a) I / Q signal simulation without Doppler shift



(b) I / Q signal simulation with Doppler shift

**Fig. 7 I/Q signal transmission wave forms**

### 4.3 Simulation results and analysis

The simulation was carried out after compiling. Fig. 8 is the waveform obtained from circuit simulation.

It can be seen from Fig. 8 that it is unsynchronized at the beginning. Symbol synchronization error$\tau$(da1_data signal) is not zero, as time goes on, the sample point is gradually close to the best sample point by loop work and the da1_data signal decreases little by little. It shows the loop has been locked at the best sample point if the da1_data is zero. The phase of input signal has been tracked continuously by phase error $\phi$ (da2_data signal), which is changed between 0 and $2\pi$, thus making the phase of correlator input signal to zero for ensuring the correctness of demodulation.

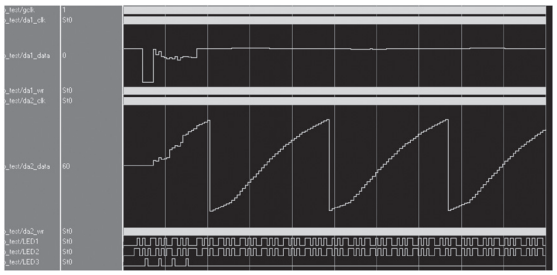


**Fig. 8 Waveform obtained from circuit simulation of synchronization module**

### 4.4 Measurement results and analysis

After the above-mentioned design and simulation, the hardware configuration was added to the design for com-

pilation and synthesis, and finally the produced bit file was downloaded in FPGA for hardware debugging. First, the modulation circuit was downloaded in one experimental board and produced modulation waveform. The output wave can be seen from Fig. 9. The demodulation circuit was downloaded in another experimental board, the modulation waveform was sent to another experimental board acting as a receiver for down-conversion and signal demodulation. The demodulation wave can be observed from Fig. 10.

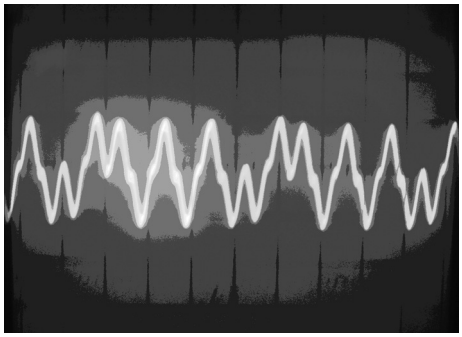


**Fig. 9 Waveform of real input**

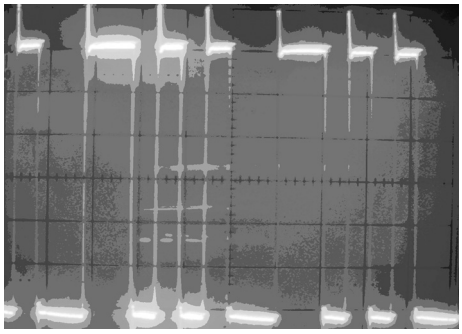


**Fig. 10 Waveform of real demodulation**

The results of experiment show that the synchronization circuit for GPS software receiver (carrier phase synchronizer and symbol synchronizer) can be implemented in FPGA using the all-digital method, and so it lays a good foundation for the realization of embedded real-time GPS software receiver system.

## 5. Conclusions

The GPS software receiver designed in this paper based on FPGA has the features of low cost, miniaturization, low power and strongly real-time. By simulation and measurement, it is verified that the decision-directed joint tracking algorithm of carrier phase and symbol timing for received signals from GPS is reasonable. In addition, the loop works steadily and can be used for receiving GPS signals using synchronous demodulation. Surely, it will become one of the development directions for GPS and even GNSS embedded real-time software receiver.

## References


[1] D. M. Akos, J. B. Tsui. Design and implementation of a direct digitization GPS receiver front end. *IEEE Trans. on Microwave Theory and Techniques*, 1996, 44(12): 2334–2339.

[2] M. L. Psiaki. Block acquisition of weak GPS signals in a software receiver. *Proc. of ION GPS*, Salt Lake City, USA, 2001: 2838–2850.

[3] L. Winternitz, M. Moreau, G. J. Boegner, et al. Navigator GPS receiver for fast acquisition and weak signal space applications. *Proc. of ION GPS*, Long Beach, USA, 2004: 1013–1026.

[4] B. M. Ledvina, M. L. Psiaki, S. P. Powell, et al. Bit-wise parallel algorithms for efficient software correlation applied to a GPS software receiver. *IEEE Trans. on Wireless Communications*, 2004, 3(5): 1469–1473.

[5] N. Kubo, S. Kondo, A. Yasuda. Evaluation of code multipath mitigation using a software GPS receiver. *IEICE Trans. on Communications*, 2005, E88B(11): 4204–4211.

[6] O. V. Korniyenko, M. S. Sharawi. GPS software receiver implementations. *IEEE Potentials*, 2007, 26(3): 42–46.

[7] J. H. Liu, T. Y. Shih. A performance evaluation of the internet based static GPS computation services. *Survey Review*, 2007, 39(304): 166–175.

[8] G. X. Gao, A. Chen, S. Lo, et al. GNSS over China: the compass MEO satellite codes. *Inside GNSS*, 2007 (7/8): 36–43.

[9] W. D. Wilde, F. Boon, J. M. Sleewaegen, et al. More Compass points tracking China's MEO satellite on a hardware receiver. *Inside GNSS*, 2007, (7/8): 44–48.

[10] N. Bertelsen, K. Borre, P. Rinder. GPS code software receiver at Aalborg University. *ESA Workshop on Satellite Navigation*, UK, 2005: 373–380.

[11] D. Lei. *IF GPS signal simulator development and verification*. Thesis of the University of Calgary, Canada, 2003: 30–45.

[12] B. Tang, X. R. Dong, S. S. Liu, et al. Research of software GPS receiver in dynamic environments. *Journal of System Simulation*, 2007, 19(8): 1807–1810.

[13] B. Tang, X. Q. Yu, X. R. Dong, et al. Design intelligent carrier tracking loop based on software GPS receiver. *Journal of Beijing University of Aeronautics and Astronautics*, 2007, 33(7): 807–810.

[14] T. Zhang, X. W. Chen, Z. S. Zhu, et al. Structure of GNSS software receiver and its realization. *Computer Engineering*, 2008, 34(7): 266–268.

[15] K. H. Tang, M. P. Wu, X. P. Hu. Design and validation of GPS software receiver based on RF front-end. *Journal of Chinese Inertial Technology*, 2007, 15(1): 51–54.

[16] L. Zhang. Simulation on C/A codes and analysis of GPS/pseudolite signals acquisition. *Science in China*: *Series E-Technological Sciences*, 2009, 52(5): 1459–1462.



**Xiaolei Yu** was born in 1981. He received the B.E. degree from Nanjing University of Aeronautics and Astronautics in 2000, and received the M.E. degree of communication and information engineering in 2007 from Nanjing University of Aeronautics and Astronautics. He is now pursuing the doctoral degree in the Department of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interest in the area of automatic control and information technology is in combined navigation system and information integration. Supported by Chinese Scholarship Council, he is working as a visiting research scholar in Faculty of Science and Technology, Deakin University, Australia from 2008 to 2010.
E-mail: xiaoleiyu@nuaa.edu.cn

**Yongrong Sun** was born in 1969. He received the M.S. and D.S. degrees from Nanjing University of Aeronautics and Astronautics in 1997 and 2004, respectively. He is now an associate professor in the Department of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interests include intelligent control and navigation, satellite navigation and information integration.

**Jianye Liu** was born in 1957. He received the D.S. degree from Nanjing University of Aeronautics and Astronautics in 1995. He is now a full professor in the Department of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interests include advanced control and navigation, satellite navigation and integrated navigation.

**Jianfeng Miao** was born in 1981. He is now pursuing the doctoral degree in the Department of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interests include design for GPS software receiver and relative algorithms. Now he is working as a visiting research scholar in the Department of Land Surveying & Geo-Informations, Hong Kong Polytechnic University, Hong Kong, China.