GSM Transceiver Front-End Circuits in 0.25-μm CMOS

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***Abstract*—So far, CMOS has been shown to be capable of operating at radio-frequency (RF) frequencies, although the inadequacies of the device-level performance often have to be circumvented by innovations at the architectural level that tend to shift the burden to the circuit building blocks at lower frequencies. The RF front-end circuits presented in this paper show that excellent RF performance is feasible with 0.25-μm CMOS, even in terms of the requirements of the tried-and-true superheterodyne architecture. Design for low-noise and low-current consumption targeted for global system for mobile communication handsets has been given particular attention in this paper. Low-noise amplifiers with sub-2-dB noise figures (NF's) and a double balanced mixer with 12.6-dB single-sideband NF, as well as sub-25-mA current consumption for the RF front end (complete receiver), are among the main achievements.**

I. Introduction

THE quest for miniaturized cellular telephone handsets has resulted in the development of commercial transceiver IC's of increasing integration levels in the last decade. The more traditional radio-frequency (RF) front ends comprising a single low-noise amplifier (LNA) or LNA-mixer combination, though they still have a strong presence in the market, are expected to give way slowly to the more highly integrated front ends that combine the RF mixer, or even the LNA, with the intermediate-frequency (IF)-strip and baseband demodulators [1]–[5] in the receiver. So far, the dominant technology for commercial RF front ends has been advanced bipolar junction transistors (BJT).

The last five years have also seen CMOS, traditionally confined to the digital and baseband part of radio transceivers, make successful inroads into the RF sections. At the research level, highly integrated CMOS RF transceivers have been reported for wireless local-area network and cordless telephones [6], [7] that are highly innovative in terms of architecture design. For cellular applications, where weight, size, and standby requirements of the handset are much more demanding and the radio network environment more complex (less restricted in terms of possible interfering signals) and hostile, CMOS implementations of RF front ends have still fallen far short of the BJT performance, especially in terms of current consumption [6], [8]. Compared to the typical current consumption of 50 mA in highly integrated BJT receivers, CMOS receivers published so far typically consume 100 mA, which makes them an unattractive alternative to BJT solutions because of the corresponding drop in standby time or increase in battery size and weight.

In this work, we report a low-power CMOS RF front end that is part of our ongoing effort to develop a complete RF transceiver in deep submicrometer CMOS, and which not only meets the more stringent requirements of cellular telephony but is also competitive to BJT implementations in terms of current consumption. Instead of simultaneously taking on the difficulties of both a novel architecture development and low-power implementation of RF circuits using CMOS, we have opted the path of first gaining experience in the latter. The receiver architecture for our RF front end is therefore the well-established and widely used superheterodyne receiver. Since more than 70% of the power in a typical receiver is consumed by the building blocks that operate at the RF frequencies, our initial work has concentrated on the LNA and mixer for the receiver and the preamplifier for the transmitter, which we report in this paper. The IF strip plus the baseband circuits will form another chip that will be the subject of another report [9]. The ultimate goal of this work is to combine the complete receiver and transmitter into a single IC that meets at least the performance required for small mobile stations (MS's).

This paper is organized as follows. Section II provides a general description of the transceiver chip architecture and required performance. Design considerations of the LNA and mixer, including the many tradeoffs involved, are presented in Sections III and IV, before the transmitter preamp design is described in Section V. Sections VI and VII conclude the paper with discussions on the achieved power consumption and measured performance, respectively.

II. Transceiver Architecture and Relevant GSM Specifications [10]

Receiver planning typically consists of tradeoffs, such as the number of IF's, the exact frequency of each IF, the distribution of gain, linearity, and noise figure (NF) to each block in the chain, etc. In addition to the minimum performance for type approval, many other important parameters such as size, complexity, power consumption, and cost must be carefully taken into consideration.

In our case, the partners at the system-design level have specified the single-IF superhet architecture shown by the block diagram in Fig. 1. The relatively high IF of 71 MHz was primarily dictated by image-rejection requirements and the availability of low-cost commercial filters. Realizing high gain at such a high frequency had raised concerns over the power consumption and stability of the IF amplifier, with automatic

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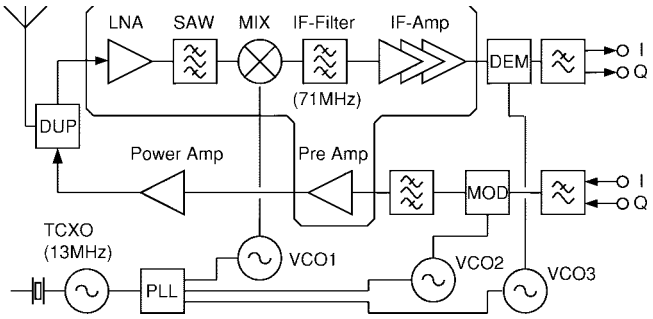

Fig. 1. Transceiver block diagram: single-IF superhet receiver, direct up-conversion transmitter.

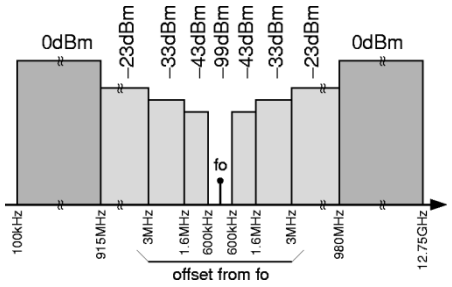

Fig. 2. Template of blocking signal levels specified by the GSM standard.

gain control (AGC). Those concerns were addressed when an earlier test chip [11] we implemented showed that with a good design, a relatively low-power IF amplifier is feasible at 71 MHz. Since complete channel filtering at the 71-MHz IF is not possible without using high-quality filters whose price is not justified for this application, intermodulation performance of the IF amp is critical, adding further complexity to its design. To limit these problems and achieve a feasible design, 32 dB of the total gain was allocated to baseband, and the maximum gain of the IF amplifier was limited to 60 dB. An AGC range of 80 dB is implemented in the IF amp that is digitally programmable from -20 to $+60$ dB in 2-dB steps.

The large dynamic range (-102 dBm to -15 dBm) of the input signal as specified in global system for mobile communication (GSM) standards, for which a bit error rate (BER) of $<10^{-3}$ must be maintained, requires at least 87 dB of AGC range for the receiver to avoid saturating the baseband analog-to-digital (A/D) converters, in addition to the necessary linearity. Allowing for a 10–15-dB margin, the receiver needs to be designed with 100-dB AGC range. Since the IF amplifier is programmable over an 80-dB range, the additional 20 dB is implemented in the LNA with a bypass switch.

The gains for the LNA and the RF mixer require another tradeoff in receiver planning. The main parameters to be taken into consideration are sensitivity, intermodulation, and blocking performance, as well as power consumption. Using high gain in the LNA helps reduce the noise figure by compensating the insertion loss of the interstage filter and scaling down the noise contribution of the mixer. This is done at the expense, however, of higher power consumption and with the risk of early overloading of both the LNA output stage and the mixer.

The blocking signal levels that may overload the LNA are depicted in Fig. 2, as prescribed by GSM testing for type approval. At 20 MHz away from the MS receive bands, 0 dBm can be expected at the receiver front end. After 25–30-dB attenuation by a typical RF filter or duplexer, the blocking signal at the output of a 15-dB LNA can still be as high as -10 dBm. For 5–10-mA output current, the -1-dB compression point cannot be expected to be much higher than -5 dBm in a 50-Ω environment at the output of the LNA. If we expect the LNA to operate with blocking signals some 6 dB below its compression point, then its gain must be limited to 15 dB. Since 3–4-dB loss is expected to come from the interstage filter after the LNA, the noise power of the mixer is only divided by 16 before it is added to the input noise of the LNA. If the overall NF specification is tight, both the LNA and the mixer must also have low NF.

In digital wireless communication, the noise figure of the receiver is a particularly critical parameter, because at the boundary between very low and very high BER, the transition can be effected by just 1–2 dB of signal-to-noise ratio. A low noise figure enables satisfactory reception even for low levels of received signal power, which, in turn, allows lower power transmission from the base station and lower levels of interference in the radio environment in general.

For GSM type approval, a reference sensitivity of -102 dBm is specified for small mobile stations. This means that for static additive white Gaussian noise (AWGN) channel conditions, BER $< 10^{-4}$ must be achieved when the input signal power $P_i = -102$ dBm. For the Gaussian minimum-shift keying (GMSK) modulation scheme used in GSM, an SNR of about 9 dB is required to reach such a BER, assuming an optimum maximum-likelihood sequence estimation (MLSE). If a suboptimal minimum-shift keying (MSK) type detector is assumed, an SNR of 10 dB is required [12]. The simplicity of the MSK type is of interest here as it makes the latter well suited for low-power implementation while offering essentially the same performance as MLSE, especially under conditions more realistic than a static AWGN channel. Bearing in mind that the (antenna) source noise power density at 290 K is -174 dBm/Hz, a noise power $P_n = -121$ dBm results for a 200-kHz channel. The required NF after the antenna can therefore be calculated (in dB) as NF $= P_i - P_n -$ SNR $= 9$ dB.

Between the antenna and the LNA an RF filter, or often a duplexer, is required to attenuate blocking interferers. Its passband loss, however, translates directly into a serious NF degradation for the receiver. A typical duplexer [13] that we intend to use, for example, has an insertion loss of 3.2 dB for the receive (RX) path [1.2 dB for the transmit (TX) path]. This leaves an overall NF of less than 6 dB at the LNA input.

A typical RX image-reject, interstage filter has an insertion loss of 3–4 dB (3.8 dB in [13]), which degrades the NF at the mixer input by the same amount. As a result, even if the NF's of the LNA and mixer are as low as 2 and 12 dB [single sideband (SSB)], respectively, the overall NF will still be 7.6 dB, leaving only a small margin for gain tolerances, insertion loss of the IF filter, noise contribution from the IF amp, and the imperfect rejection of the LNA's noise at the

image frequency. To prevent excessive NF contributions from the IF strip, a gain of 10 dB is specified for the mixer. If we restrict the NF of the IF strip (including the IF filter's insertion loss) to 15 dB, the overall NF is just under 8 dB. The 15-dB limit can be met, for example, by an IF AGC with 8-dB NF [11] combined with an IF filter with 5.1-dB insertion loss [13]. Or a cheaper IF filter with 11.3-dB loss [13] could be tolerated with a better AGC design with a 4-dB NF, which is more difficult. Should the gain of the LNA drop to 14 dB due to component variations, the overall NF becomes 8.5 dB, which is still within specifications. The NF's are therefore specified as 2- and 12-dB SSB for the LNA and the mixer, respectively, both tough values even for BJT or GaAs technologies.

To save the interstage filter and eliminate the adverse effect of its insertion loss on NF, image-reject mixers can be used as an alternative. By operating two mixers in quadrature, the image is usually attenuated by 30–35 dB, which is sufficient to prevent noise at the image frequency from contributing to the total NF excessively. Having two mixers operating at 900 MHz and a phase shifter in both local oscillator (LO) and IF paths, however, will result in roughly three to four times higher power than that of one conventional mixer. Such high power consumption was considered unacceptable.

Compared to the receiver, the transmitter requirements are relatively simple, with the most difficult one being perhaps meeting the -36-dBm spurious signal emission limit.

Without any IF or image frequency, a direct upconversion transmitter is less likely to generate spurious signals. The filtering requirements to eliminate leakage are therefore greatly simplified. Power consumption, one of the disadvantages of direct conversion, is not as critical here, since it will be dominated by the power amp ($\sim$5-W average input power during the transmit time slot). The direct upconversion architecture, shown in Fig. 1, is therefore preferred.

Since the local oscillator will be integrated on the same chip as the transmitter, oscillator pulling may be an issue. Using an offset local oscillator will solve this problem, at the expense of an extra external filter.

The integrated part of the transmitter consists of a vector modulator, driving a preamp via an external interstage surface-acoustic wave (SAW) filter [13]. In the present front end, only the transmitter preamp has been integrated to test the ability of CMOS to deliver 2 mW of power, which is typically required by commercial power amplifiers. Thanks to the constant envelope modulation, linearity is not too critical, and the preamp can be driven at the compression point for better efficiency. The nominal gain of the preamp is 23 dB.

III. Low-Noise Amplifier

In addition to the gain and noise figures, which have been discussed in the previous section, the requirements of the LNA include 50-Ω matching at both the input and the output, small signal linearity, which is described by the third-order intercept point (IP3), and large signal linearity, which is described by the -1-dB compression point (CP). In addition, these performance parameters must be relatively insensitive to the variations of process parameters and values of passive components such as the matching inductor and capacitors [14].

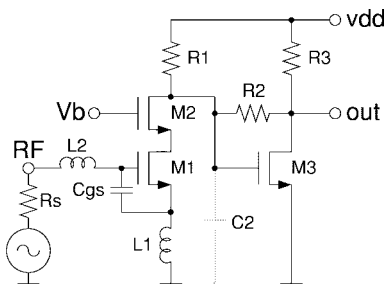

Fig. 3. Common-source LNA with transimpedance output stage.

A. Input Stage

The most important factor that determines our choice of the LNA configuration is the achievable noise figure. Although noise figures of 3 dB and above are usually quite easy to achieve given sufficient current, even in GaAs and BJT technologies integrated LNA's do not often have sub-2-dB noise figures. This apparent barrier can be partially explained by the definition of the noise figure itself, which dictates a law of diminishing returns.

Since the input-referred noise of an MOS transistor is given by $4\gamma kT/g_m$, $\gamma \geq 2/3$, the noise factor of a common-gate (C-G) amplifier is given by $1+\gamma$. The minimum NF achievable by a C-G amplifier is therefore 2.2 dB for $\gamma = 2/3$. With additional noise contributions of pads, substrate, and the output stage, the achievable NF is more like 3 dB, which is too high for our application.

For a common-source configuration, as shown in Fig. 3, the real part of the input impedance required for 50-Ω matching is generated by the inductive degeneration [14]–[16]. The matching network formed by L_1, L_2, and the gate capacitance $C_{\rm gs}$ has a voltage gain between the LNA input (marked RF) and the gate source of transistor $M1$ that is equal to the quality factor Q of the matching network at resonance

$$Q = \frac{1}{g_m \omega_o L_1}. \tag{1}$$

If Q is greater than one, this gain may help reduce the contribution of the thermal noise of $M1$'s channel I_n^c, and of those noise sources from the LNA's output stage to the overall LNA noise figure. For example, the NF contribution of I_n^c alone is given under matching conditions by

$$\text{NF} = 1 + \gamma \frac{\omega_o L_1}{Q \cdot R_s} = 1 + \gamma \frac{1}{Q^2 \cdot g_m R_s} \tag{2}$$

where $\gamma = 2/3$ for long channel devices. Even if the transconductance is set to only 20 mS, as in the case of the C-G configuration, the voltage gain Q can still reduce the noise contribution from I_n^c to very low levels. Indeed, this well-defined contribution reduces to such insignificant levels even with moderate values of Q and g_m that the NF of common-source LNA's, typically 1.5–3 dB even if integrated in GaAs and BJT technologies, must be dominated by other, less well-defined noise sources. This latter category of noise sources

includes the contribution of substrate resistance through capacitances under bonding pads, gate-induced noise current [15], and the back-gating effect of the substrate resistance under the MOS transistor [17].

A more important reason to use $Q>1$ to achieve some voltage gain is to reduce the required current level for a given overall transconductance of the input stage. Under matching conditions and neglecting the parasitic capacitances associated with input pads, the ratio between the output current of the input stage and the input voltage of the LNA is exactly the inverse of L_1's impedance, independent of the transconductance g_m of $M1$

$$|G_m| = \frac{1}{\omega_o L_1}. \tag{3}$$

The overall voltage gain of the LNA is then given by the product of G_m and the load (trans)impedance of the output stage. The latter impedance is constrained by the output matching requirement to the order of 50 Ω. For 15-dB LNA gain, $G_m \sim 120$ mS, so that at 1 GHz the value of L_1 lies around 1 nH. This happens to be the value of a typical bondwire, so that no board-level inductor is necessary for L_1's implementation.

Once this overall G_m or bondwire impedance is determined, the transconductance g_m of $M1$ is related to Q by (1). If we use the simple formula $g_m = \sqrt{2\mu C'_{\rm ox} W \cdot I/L}$ to estimate the current consumption, and bear in mind one of the conditions for impedance matching

$$g_m L_1 = C_{\rm gs} R_s \tag{4}$$

then we see that the bias current I is inversely proportional to Q. This is important for a CMOS LNA design, for without this voltage gain $(Q=1)$, 10 mA would be needed for a G_m of 120 mS even for a 0.25-μm gate length.

While a high Q matching network allows the current consumption of the LNA input stage to be low, the level of reactance associated with the network inductors and capacitor becomes high. Although the nominal capacitive and inductive reactance should cancel each other if designed for 50-Ω matching, the same 10% deviation from the nominal values results in higher residual (uncancelled) reactance for higher Q. The variability of the input reflection coefficient S_{11} is therefore also worse. One of the serious effects of the increase in S_{11} and deviation from 50-Ω input resistance is the worsening of the RF filter performance [14].

Measurements of a commercial duplexer [13] in Fig. 4 show that for $|S_{11}| = -6$ dB, not only can the filter's passband loss increase by 0.5 dB, causing a corresponding increase in overall noise figure, but also the stopband attenuation can degrade by as much as 6 dB at 20 MHz away from the passband, where 0-dBm blocking signals are expected.

In our design, a fairly low quality factor of 2.5 is used for the input matching network, so that for the 10–20% tolerance expected of L_1, L_2, and $C_{\rm gs}$, the variability of S_{11} is still very low. On the other hand, the bias current of the first stage is reduced to 4 mA, which is sufficiently low in the context of the target current consumption of 25–50 mA for the complete RF receiver.

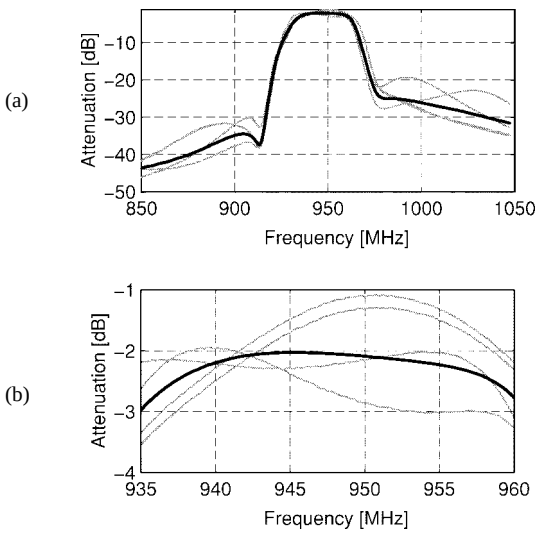

Fig. 4. Measured duplexer characteristics. The thick curve is with exact 50-Ω matching. The other four were measured with imperfect S_{11}: $|S_{11}| = -6$ dB, phase of $S_{11} = 45°, 135°, 225°$, and $315°$. (a) Overall transfer function and (b) closeup of passband.

Without the cascode transistor $M2$, the influence of $M1$'s Miller capacitance can add to that of the pad capacitance to cause the design to deviate from the ideal situations described by (1)–(4) quite significantly. The bias current of $M1$, for example, increases from 4 to 6 mA. The cascode transistor, on the other hand, may contribute some of its own noise to the amplifier because $M1$'s output impedance is low due to the very short channel length and high current.

Having scaled down the contribution of the thermal noise of $M1$'s channel by the Q of the matching network, the design of the LNA input stage for a low noise figure must then concentrate on parasitic noise sources that are not so well defined as I_n^c. Characterizing the transistors for NF before using them for the LNA, as is often done in traditional microwave LNA designs, is beyond our resources, because this entails fabricating arrays of transistors of anticipated range of dimensions and bias currents, with anticipated layout. Since such devices are not designed to match the 50-Ω test environment, deembedding the influence of pads and other test fixtures and measuring the intrinsic noise figure at 1 GHz is quite a major undertaking. Minimum noise figure measurements from the CMOS process provider that typically come from transistors with a specific W/L ratio and layout, and biased at unrealistically high currents such as 40–50 mA, do not provide us much information either. In the absence of accurate RF models of MOS transistors backed by reliable experimental verification, the design for low NF for our LNA's had to combine general care in noise minimization with some specific, controlled experiments that were conceived to extract some data on the relative importance of certain parasitic noise sources in the overall noise figure.

One such source is the induced gate current [18], [19]. At higher microwave frequencies, this noise source is important. Recently, a detailed analysis has been published [15] that not only argues that induced gate noise current is also important for CMOS at the low gigahertz frequency range but also

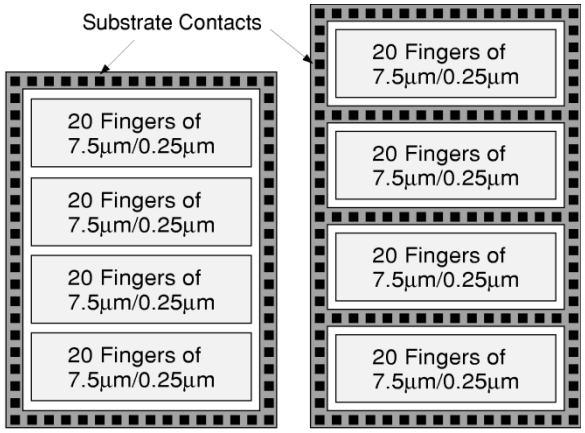

Fig. 5. Layout of transistor $M1$: (a) LNA-1 and (b) LNA-2.

proposes ways of optimizing the LNA design parameters, such as the matching network Q, to achieve minimum noise figure. Unfortunately, the predicted optimal NF was not borne out by their experimental results, which leaves the subject still wide open.

Another important source of noise reported recently [17] for CMOS LNA's is the backgating effect of the resistive substrate under the transistor channel. In the case of the 0.25-μm CMOS we used, the substrate resistivity has a fairly high value of 5 Ω-cm, which could have an even higher influence. The experimental data given in [17], however, reported an NF difference of 1 dB between a layout with good substrate contacts to ground and a layout with less contacts, at a high level of 6–7-dB overall noise figure. The important question for us was whether there will be much difference for LNA's already having low noise figures.

In the initial stage of our development, we had succeeded in realizing a 0.25-μm CMOS LNA, which we refer to as LNA-1, for which care was taken in pad design, fingered gate layout, etc., so that the measured noise figure was as low as 2 dB. The substrate around the gate of $M1$ was already well grounded by rows of contacts surrounding the periphery of the 600-μm gate that is formed by 80 7.5 by 0.25-μm^2 fingers, as shown in Fig. 5(a). The input stage of LNA-1 did not use the cascode transistor $M2$, so that the bias current was 6 mA and the actual matching network Q was close to one due the influence of Miller capacitance.

To investigate the influence of substrate resistance on achievable NF, we integrated a second LNA, LNA-2, that is nominally exactly the same as LNA-1, except that the layout of the gate of $M1$ was changed to allow more substrate contacts to be placed, as shown in Fig. 5(b). The original LNA-1 was integrated again in the same run as a reference to avoid confusing NF variation from run to run with the NF improvement due to difference in layout.

Realizing that $M1$'s Miller capacitance is causing a significant deviation of the matching network gain from that given in (1), which results in 6 mA instead of 4 mA in the input stage, we also introduced the cascode transistor $M2$ at this stage. In doing so, the effective matching network Q increases from one to two, which allows the bias current to reduce to 4 mA. This has been implemented as LNA-3 in the same run as LNA-1 and LNA-2. Although the change in Q as a result of going from a noncascode configuration to a cascode one is not exactly the same as designing for different matching network Q's for the same LNA configuration, we believe that if the matching network Q indeed has as strong an influence on the LNA NF as [15] seems to suggest, then we should see some evidence of this by comparing LNA-2 and LNA-3. The gate of $M1$ in these two amplifiers has exactly the same layout. All three amplifiers should have noise figures less than or equal to 2 dB.

B. Output Stage

Since the overall transconductance G_m of the input stage is of the order of 100–200 mS, an effective load impedance between 50 and 100 Ω is needed to realize 15-dB gain. In the CMOS technologies to date, however, the relatively high level of parasitic capacitance (C_2) tends to limit the achievable cutoff frequency. To broadband the load impedance, the shunt feedback of the output stage transimpedance amplifier in Fig. 3 is one of the most commonly used methods [1], [20]. The loop gain of the shunt-feedback, approximately given by $g_{m3}R_L$, scales down the input resistance of the output stage so that the parasitic capacitance C_2 does not cutoff the amplifier's frequency response as early as before. The impedance R_L is the parallel combination of the output impedance of $M3$, the bias resistance $R3$ and the 50 Ω input impedance of the interstage filter.

If the loop gain is sufficiently large, then the transimpedance of the output stage in Fig. 3 is approximately given by the feedback resistance R_2, and the overall LNA gain is simply G_mR_2. In practice, the limitation of $M3$'s transconductance g_{m3} by current, IP3, and gate capacitance considerations means that only moderate loop gain is achievable with an R_L that is dominated by the 50-Ω load. The LNA gain must be designed on the basis of the more accurate design equation

$$A_{\rm VE} = \frac{1}{\omega_o L_1}\left[\frac{R2+R_L}{1+g_{m3}R_L}||R1||Z_{d12}\right] \cdot \frac{R_L}{R_L+R2}(1-g_{m3}R2) \tag{5}$$

where Z_{d12} is the output impedance of $M1$ or the $M1$–$M2$ cascode.

Because of the higher parasitics associated with PMOS transistors, the latter are unsuitable for biasing purposes, and resistors $R1$ and $R3$ are used instead. The lack of voltage headroom combined with high bias currents constrain the values of $R1$ and $R3$ to a couple of hundred ohms. In addition to (5), the choice of $R1, R2$, and $R3$, as well as g_{m3}, are constrained by two other important requirements—realizing a 50-Ω output resistance and providing a -1-dB compression point (CP) that is sufficiently high. The latter is limited by the maximum output voltage for a given bias current I_3

$$\begin{aligned} V_o^{\max} &= I_3 \cdot Z_3 = I_3 \cdot [(R2+R1||Z_{d12})||R_L] \\ &= I_3 \cdot [(R2+R1||Z_{d12})||R3||Z_{d3}||R_{50}] \end{aligned} \tag{6}$$

TABLE I
SUMMARY OF THE IMPLEMENTED LNA'S AND THEIR KEY DESIGN PARAMETERS

	I(M1) (mA)	I(M3) (mA)	M1 (μm)	M2 (μm)	M3 (μm)	R1 (Ω)	R2 (Ω)	R3 (Ω)	Sub. contact
LNA1	6	12	600	-	100	235	120	105	Fig.5a
LNA2	6	12	600	-	100	235	120	105	Fig.5b
LNA3	4	12	600	600	100	400	120	105	Fig.5b
LNA4	4	6	600	600	300	400	120	255	Fig.5b

where Z_3 describes the impedance seen by the drain terminal of $M3$. Because of the 50-Ω input impedance of the interstage filter, $R_{50}, |Z_3|$ is less than 50 Ω. This means that for a CP requirement of 0 dBm (300 mVp), the bias current I_3 must be no less than 6 mA. In practice, $R1$ and $R3$ cannot be very high because of both the voltage headroom and the need to implement the 50-Ω output impedance for the LNA. In the worst case, $|Z_3|$ can be as low as 25 Ω, and twice as much current is needed. The constraint on $R1, R2$, and $R3$ in terms of 50-Ω output impedance can be expressed as

$$Z_0 = \left(\frac{R2 + R1||Z_{d12}}{1 + g_{m3}(R1||Z_{d12})}\right)||R3||Z_{d3} = 50\ \Omega \qquad (7)$$

where it can be seen that in the absence of $M3$'s transconductance g_{m3}, the 50-Ω output impedance would have to be implemented completely by $R1, R2$, and $R3$, in which case $|Z_3|$ in (6) would be as low as 25 Ω. The design for the output stage is therefore primarily a tradeoff of resistance values to satisfy (5)–(7) and minimize the required output current, while ensuring that $M3$'s gate overdrive is sufficiently high to maintain a high IP3. The latter requirement sets a limit to $M3$'s gate width.

For LNA-1, a higher CP was aimed at, which led to higher output current. With the absence of the cascode, the current of the input stage is also higher, resulting in lower values of $R1, R2$, and $R3$. This leads to an output bias current of 12 mA that gave us a measured output CP of −4 dBm. This output stage design has been left unchanged for LNA-2 and LNA-3, so that only one thing is different between the two successive designs. Further optimization of the output stage, which took advantage of the lower bias current of the input stage, allows the levels of $R1, R2$, and $R3$ to be somewhat higher than before, so that only half the bias current is needed for the output stage with only a slight drop in output compression point (oCP). The increase of resistance levels is also expected to result in lower equivalent noise referred to the drain of $M2$, so that the overall noise figure will be slightly lower. This design is referred to as LNA-4. The differences between the four designs and the key parameters of each design are summarized in Table I.

IV. SINGLE- AND DOUBLE-BALANCED MIXER

The chief requirements of an RF mixer in a superhet receiver such as ours are 50-Ω matching to the interstage filter, low noise figure, high IP3, and a moderate gain to reduce the noise contribution of subsequent stages to the receiver front end. To satisfy all of the requirements, single- or double-balanced mixers (SBM's and DBM's, respectively) based on the Gilbert cell are practically left as the only choice, as evidenced by the fact that they are found in virtually every BJT RF front-end IC.

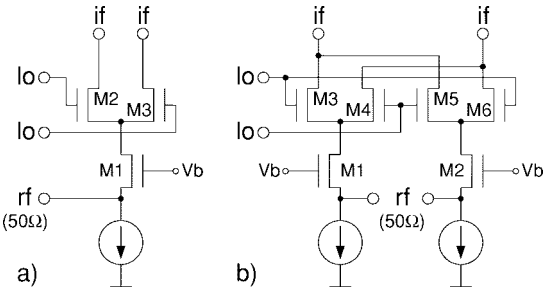

Fig. 6. Schematic diagram of (a) single-balanced mixer and (b) double-balanced mixer.

In a single- or double-balanced mixer, shown in Fig. 6 in CMOS form, the transconductor $(g_{\rm mi})$ implemented by the (input) RF transistor(s) is followed by commutating switches that perform the function of frequency translation. The effective conversion transconductance of the mixer is $g_{\rm mi}/\pi$ for the single-balanced configuration and $2g_{\rm mi}/\pi$ for the double-balanced configuration, assuming ideal switching. Thus, even in the ideal case, the switches introduce a loss of $1/\pi$ (−9.9 dB) for the SBM case and $2/\pi$ (−3.9 dB) for the DBM case. With sinusoidal LO signals, the switching is much less than ideal and the loss is more like −12 dB for the SBM case and −6 dB for the DBM case. Because of this loss, the influence of noise current introduced by the switching transistors during the time when each pair of switches remains in the on-state simultaneously, for example, dominates that of the RF input transistor(s). Combined with the inherent 3-dB NF degradation due to aliasing of the noise in the image sideband, the noise figure is therefore usually high for Gilbert mixers—15 dB, for example, for BJT implementations.

Because the expected NF is high for mixers, whether the input transistors contribute 2 or 3 dB to the overall NF therefore is not very critical. This justifies the use of the common-gate configuration for the input stage, which can be designed to provide a resistive 50-Ω input matching to the filter without any external components. The g_m of the input transistors is therefore 20 mS for the SBM case and 40 mS for the DBM case.

In cellular applications, neighboring base stations often generate strong interfering signals in channels adjacent to one's own receiving channel. Since such interferers cannot be filtered by the RF or interstage filters and will be amplified by the LNA, the small signal linearity IP3 of the mixer must be sufficiently high to prevent intermodulation from degrading the bit error rate. The type-approval requirement for GSM stipulates that the BER for reference sensitivity must be met in the presence of two −49-dBm interferers at 800 and 1600 kHz away, respectively, from the desired signal, when the latter's power is −99 dBm. The mixer's IP3 requirement is directly linked to the combined receiver front-end gain $A_{\rm VF}$ before the mixer. If we assume again that 10-dB SNR is required to achieve the desired BER, then the required IP3 (in dBm) is

bound by the following inequality:

$$-99 + A_{\mathrm{VF}} - 3 \cdot (-49 + A_{\mathrm{VF}}) - 9 + 2 \cdot IP3 \geq 10 \quad (8)$$

or

$$IP3 \geq A_{\mathrm{VF}} - 14.5. \quad (9)$$

Considering that within the passband of each filter the gain for the signal could be 1 dB different from that of the interferers due to passband ripple, the combined gain A_{VF} could be 2–3-dB worse than the nominal value. The latter, assuming -3-dB passband loss for each filter and 15 dB for the LNA, is 9 dB. Thus the required IP3 assuming worst case gain combinations for the signal and interference should be -3 to -2 dBm. Taking a 3-dB margin, the required IP3 for a small mobile station is of the order of 0 dBm. For a standard mobile station, the desired signal is 2 dB weaker (-101 dBm) and the interferences are 4 dB (-45 dBm) stronger, so that the IP3 requirement can be as high as 7 dBm.

In BJT implementations, such IP3's can only be achieved with some linearization technique such as emitter degeneration. In a CMOS mixer, as long as the transistor has sufficient overdrive so that it stays in strong inversion, achieving more than 0 dBm IP3 is not a problem [14]. For a given input transconductance as required by impedance matching, however, it imposes a minimum current requirement. In our designs, 4 mA was required for the single-balanced mixer and 6 mA for the double-balanced mixer, so that the transistor is biased halfway between weak and strong inversion.

Although the single-balanced mixer consumes less power, it provides less conversion transconductance, lower linearity, and a higher noise figure. The local oscillator signal is not suppressed by the mixer proper, so that it feeds through to the output. In a superhet receiver, however, this LO feedthrough is suppressed by the IF filter. Since a typical 71-MHz IF filter requires a matching load resistor on each port to its 330-Ω characteristic impedance, the RF mixer sees a 165-Ω load at its output. Even in the ideal case, the conversion transconductance is 6.4 mS for the SBM and 12.7 mS for the DBM, which is not enough to provide 10 dB conversion gain. A simple inductance–capacitance network is therefore required to transform the load impedance to the desired level in any case, and the 6 dB difference between the conversion g_m's of single- and double-balanced mixers is not critical as far as gain is concerned.

Because of the (6 dB) higher loss due to the switches, the SBM is expected to have a higher NF than the DBM. Assuming that the noise current of the switches dominates the mixer noise figure, and taking into consideration that the DBM has twice as many switches that generate twice the noise power, the input-referred noise figure of SBM is expected to be about 3 dB higher than the DBM.

Although we favor the DBM for its expected higher performance, we have also implemented the SBM to compare if the difference in NF is indeed as large as expected to justify 50% higher current of the DBM.

The design of the switches in the mixer is primarily a trade-off among having high W/L ratios to reduce the overlapping period in which both switches in each pair remain on, having low thermal noise current during this period, and limiting the pole introduced by the switches into the RF path outside the period for a given current. In our design, the final switch sizes are similar to those of the input RF transistors, 300 by 0.25 μm^2.

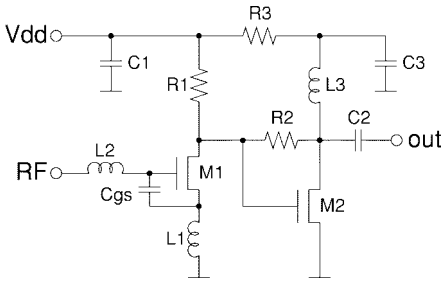

Fig. 7. Schematic diagram of the TX preamplifier.

V. The Transmitter Preamplifier

Most modern GSM power amplifiers (PA's) are constructed in a hybrid technology, using bipolar or power MOS transistors. They require 2 mW of driving power and a supply voltage of 4.8 V (sometimes 6 V). The mandatory power control is implemented in the PA, and the output power can be varied by adjusting the dc voltage applied to a control pin. The peak power of a class-4 PA is as high as 2 W. Although its average transmitted power can be much lower because the average distance between the mobile and the base station is much less than the maximum radius of the cells in the network, the average power consumption of a mobile station is still high, judging by the low talk-time advertised for current commercial handsets. Given that power consumption is dominated by the PA, the power consumption of the preamp and modulator is not as critical as in the receiver case. However, attention is paid to low-power design in the preamp so that the design will also be suitable for mobile stations with lower classes of PA's.

In this work, the TX SAW filter required to remove the harmonics of the carrier and out-of-band noise is placed between the upconversion mixers and the preamplifier. Since the loss of the filter precedes the preamp, the latter is only required to deliver 3 dBm power to the PA instead of 7.5 dBm. This will ease the problems of delivering a substantial amount of power using CMOS, including efficiency and substrate coupling.

Since the efficiency for the preamp is not as critical as the PA, a class-C approach requiring another expensive and lossy external filter before the PA is neither necessary nor saves power. Due to the lack of good PMOS transistors, a class-B, push–pull approach is also unavailable. If the preamp output harmonics that could degrade the PA efficiency are kept low, a class-A amplifier can drive the PA without the external filter. The primary requirements for our preamp, a two-stage class-A implementation as shown in Fig. 7, are thus 50-Ω matching at both the input and the output, a high gain of 23 dB, and a high power output (for CMOS) of 3 dBm with sufficient linearity.

The first stage, comprising $M1$, its biasing, and the matching network, is similar to the input stage of the LNA; therefore, the same design equations hold. The main difference here is the relatively high input level of -18 dBm. Since IM3 is inversely proportional to the overdrive of a MOS transistor, a relatively small transistor, biased at 11 mA, has been used for $M1$. Because of the relatively large overdrive of $M1$ that leaves little voltage headroom under a 2.5 V supply, no cascode transistor has been used in this design to ensure that $M1$ stays in saturation.

The second stage is a transimpedance amplifier, biased at 16 mA as required to deliver 2 mW into the 50-Ω load with sufficient linearity. The relationship between the required output compression point and the required bias current is similar to that of the LNA. Unlike the LNA, a resistive load is ruled out by bias-voltage considerations; otherwise, $R3 \sim 60\ \Omega$ will be needed, which will make high gain very difficult to achieve. With inductive loading used instead, the RF choke L_3 resonates with the drain capacitance of $M2$ at 900 MHz so that the path to $V_{\rm DD}$ appears open-circuit, and the formula for output compression point [(6)] and the output impedance [(7)] can be used with $R3$ set to infinity. In fact, L_3 and the coupling capacitance C_2 could also be used as an impedance matching network at the same time, so that the impedance seen by the drain of $M2$ could be higher, which allows higher power to be delivered for a given current. Due to the low supply voltage (2.5 V) of the 0.25-μm CMOS technology, this option cannot be used in our design because impedance scaling by the matching network also scales up the voltage swing of the drain of $M2$. Another way of achieving higher output power in traditional preamp designs is to combine such a matching network with biasing the drain of $M2$ at $V_{\rm dd}$, which doubles the allowable voltage swing. Since the margin between the breakdown voltage and the actual supply voltage is small compared to the output swing in our 0.25-μm CMOS case, this option (which entails swinging the drain of $M2$ substantially above $V_{\rm dd}$) was also ruled out on reliability grounds. To bias $M2$ in the midsupply, resistor $R3$ ($\sim$60 Ω) is inserted before L_3 and ac-bypassed by C_3 as shown. At dc, $R3$ also helps stabilize the bias condition through $R2$.

In many bipolar transceivers [3], [5], a buffer capable of delivering 2 mW into 50 Ω has been implemented, frequently as an emitter follower biased at about 10 mA to achieve high IP3. Implementing a 20-mS (50-Ω) buffer in 0.25-μm CMOS, however, is not possible because of the large voltage swing required at the gate. Delivering 2 mW to 50 Ω corresponds to having a voltage swing of 900 mVpp at the transistor's source and 1.8 Vpp at the gate. Adding the threshold voltage (400 mV) and some overdrive (200 mV) results in a peak voltage of 2.4 V, which is already higher than the specified minimum supply voltage. To reduce the swing, a lower impedance buffer followed by a matching network could be used, but this would result in an excessive increase of current consumption.

In our class-A implementation, the total current consumption is only 27 mA. Such a current level, required by linearity, is insignificant compared to that of the final PA.

VI. Power Consumption

Before describing the experimental results, it is perhaps appropriate to briefly revisit the subject of power consumption of the transceiver. Earlier, we stated that for CMOS technologies to be seriously considered as a contender for RF front end in cellular applications and as a competitor to BJT technologies, one must a) prove that the complete set of performance specifications can be met and b) do so with a current consumption comparable to today's commercial solutions. In this section, we wish to highlight the current-consumption aspect.

Low-power consumption is most important in the receive mode, as this defines the standby time, while in transmit mode, power consumption will be dominated by the high-power PA. As the dominant reason to purchase a mobile phone shifts from business to private use, the call charge serves as a natural barrier to reduce the occurrences of private users' overrunning the, say, 4-h talk time before the next recharge of the battery. Business and private users alike, however, may find 40- or even 72-h standby time inappropriate.

The designs reported here show that by combining LNA-4 and the double-balanced mixer, the nominal supply current of the front-end chip can be as low as 16 mA. Ongoing design and experimental work on the remaining part of the receiver gives us good reasons to believe that the IF strip plus the demodulator will consume no more than 6 mA, which shows that the front end is indeed the dominant consumer of power ($>$70%) of the receiver. Even if we add the voltage-controlled oscillator and the prescaler, which dominate the current consumption in a synthesizer (3 mA in RX mode), the total nominal current consumption will only be 25 mA, or 60-mW power consumption. This compares very favorably with existing chipsets to date, such as those reported in [2] (51 mA in paper, 46 mA total in datasheet), [3] (57 mA), and even [4] (33 mA), for example. The latter reference derives its high performance from an advanced 25-GHz bipolar technology.

VII. Measured Results

All measurements were performed using bare chips assembled on a printed circuit board (PCB) with all the needed external surface-mounted-device components. The die were directly glued on the PCB ground plane, which provides an excellent ground connection to the chip substrate. Some care was taken with the length of the bondwire to the source of $M1$ in each LNA and the preamplifier so that correct matching is achieved. No external trimming was performed. The supply voltage was set to its nominal value of 2.5 V. Among the chips measured, one is a combination of LNA-1, the SBM mixer, and an early version of the IF-AGC amplifier [11]. Fig. 8 shows its micrograph. The measured parameters of the implemented LNA's, mixers, and transmit preamplifier, as well as the particular receiver front end, are summarized in Table II.

For the low noise amplifiers, we are particularly interested in the noise figures, as well as the influences of the different refinements on the NF in our controlled experiments. The reference amplifier LNA-1 achieves again a low NF of 2 dB, while providing the expected gain, input, and output

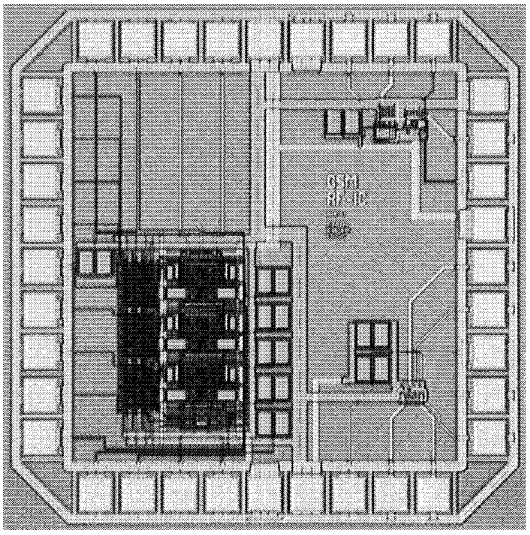

Fig. 8. Photomicrograph of front-end IC.

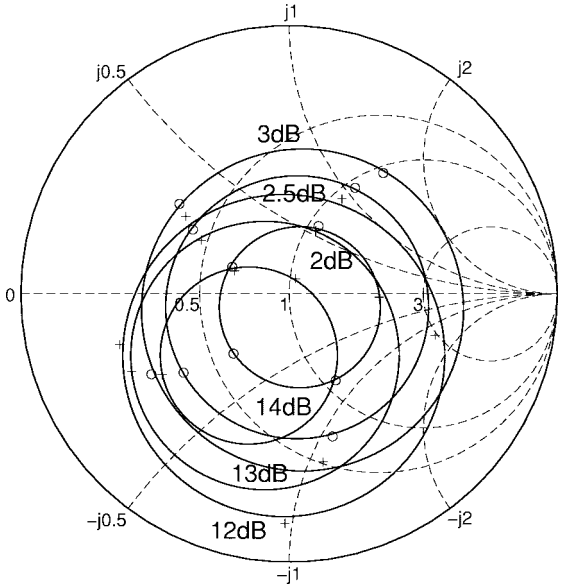

Fig. 9. Constant NF and gain circle measurements.

TABLE II
SUMMARY OF MEASURED FRONT-END CIRCUIT PERFORMANCES

	LNA1	LNA2	LNA3	LNA4	SBM	DBM	TX-PRE	RX-FE
Gain (dB)	13.8	14.3	14.3	16.4			21.1	85 max
Conv gm (mS)					4.9	8.5		
SSB NF (dB)	2.0	1.74	1.97	1.6	15.9	12.6		
iIP3 (dBm)	-2.0	-2.8		-7.3		9.0		
iCP (dBm)		-17		-20	-4	-4	-14.6	
S11 (dB)	-5.6	-6.8	-4.0	-8.0	<-15	-11	-6.6	
S22 (dB)	-8	-22	-11	-12			-8.5	
S12 (dB)	<-30	<-30	<-40	<-40				
Idd (mA)	18.3	18.1	16.6	10.8	3.5	6.0	27.2	25

impedances and excellent linearity. The fact that 2-dB NF has been achieved over consecutive runs shows that the design is suitable for manufacturing. With merely an increase in the number of substrate contacts (from a transistor that already has many contacts), LNA-2 shows a significant improvement in noise figure, to 1.74 dB. This demonstrates the significant contribution of back-gate resistance to overall NF, at least for the 5-Ω-cm substrate of the technology we used. The main influence of the cascode transistor in the input stage (LNA-3) is a 30% reduction in current consumption in the first stage due to the higher Q and lower transconductance (gm) needed, and a 10-dB improvement in reverse isolation. The price paid is a slight worsening of noise figure, which we believe to be due to the additional contribution of $M2$. No rapid improvement of NF, as predicted for the particular 0.35-μm LNA in [15] for a similar change of Q, is observed here. The last amplifier, LNA-4, achieves the best performance tradeoff for our application in terms of gain, noise figure, and power consumption thanks to a better designed output stage. The measured -5-dBm output compression point has only decreased slightly (1 dB) from that of the other three LNA's despite saving half of the output stage current. A very low noise figure of 1.6 dB is measured near the optimum noise match. This is the best result reported to date for an integrated CMOS implementation. In Fig. 9, starting with the minimum noise figure at close to the center of the Smith chart, constant NF and gain circles have been measured in terms of the source impedance seen from the noise-matched LNA. Thanks to the low Q design, these circles are big and widely separated for small increments of gain and NF. This means that variations of matching network impedance due to component tolerances in production will not cause drastic degradation of gain and NF. Indeed, in 50-Ω power-matched conditions, the measurements of LNA-4 in Fig. 10 show that 15-dB gain, -8 dB S_{11}, and 1.9-dB NF can be simultaneously achieved. Due to the effect of the bond pad, the protection diode, and the PCB parasitic capacitances at both sides of L_2, the actual 50 Ω power-match conditions of the LNA are slightly different from the ideal equations [including (2) in this paper] normally described in recent publications [14]–[16].

Turning our attention to linearity, Fig. 11 shows the measured input-referred compression point (iCP) and input-referred, third-order intercept point (iIP3) of LNA-2 and LNA-4. High IP3 values far exceeding requirements have been measured, confirming the intrinsic high linearity of MOS devices. The measured compression points meet the requirements of blocking test and are 3–4 dB below the limit set by the output current, as expected.

The measurements of the SB and DB mixers have been performed using a -1.5-dBm LO power with 50-Ω termination at the LO ports. The measured conversion gm's are 4.9 and 8.5 mS for the SB and DB mixer, respectively. They are about 30% lower than the theoretical maximum due to imperfect switching, which is expected. Although the measured NF of 15.9 dB for the SB mixer is higher than we would like it to be, it is in line with most reported mixers with gain at this frequency, including BJT implementations [1], [3]. The measured 12.6-dB SSB NF for the DB mixer, on the other hand, is one of the best reported to date for fully integrated mixers and facilitates the use of RF and interstage filters with moderate specs (hence price) in superhet GSM receivers. The S_{11} measurements are shown in Fig. 12. The common gate

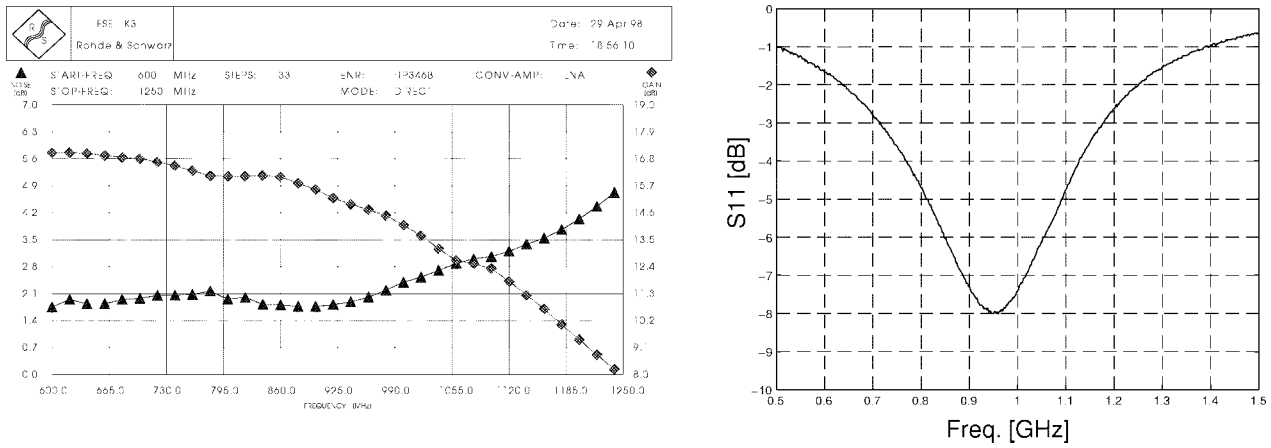

Fig. 10. Gain, NF, and S_{11} of impedance-matched LNA-4.

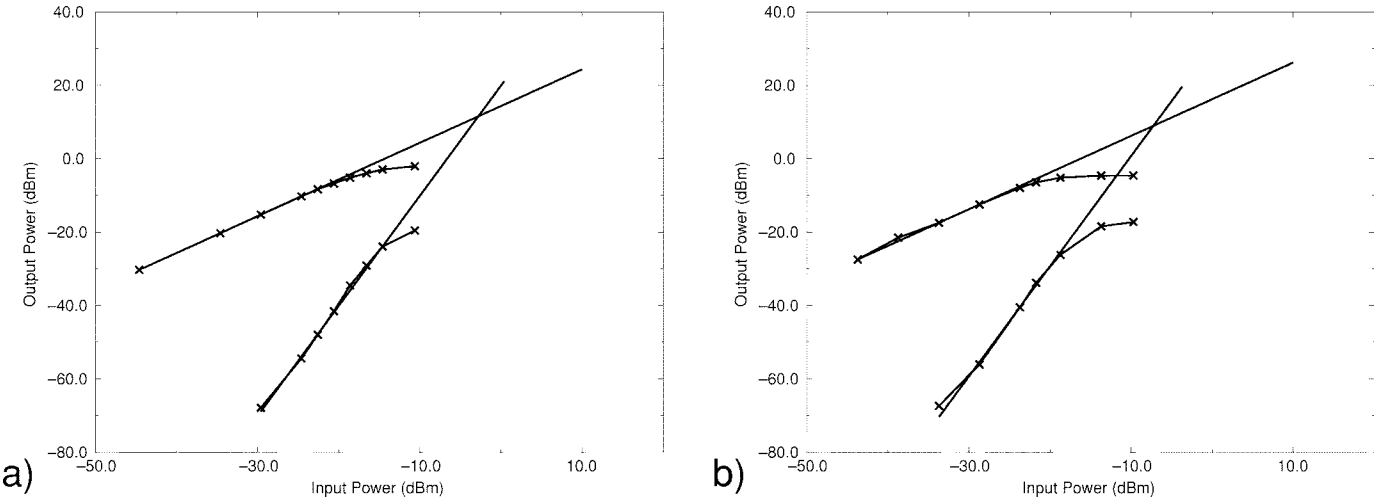

Fig. 11. Measured, input-referred, third-order intercept point iIP3 and -1-dB compression point iCP for (a) LNA-2 and (b) LNA-4, respectively.

input guarantees excellent input matching with a broadband characteristic for both mixers. Indeed, the measured S_{11} is limited by the balun needed to match the DB mixer, which nevertheless stays under -10 dB at all frequencies below 1.2 GHz. The S_{11} degradation at higher frequencies is due to the increasing influence of parasitic capacitances. Fig. 13 shows that the measured iIP3 is as high as 9 dBm, and iCP -4 dBm, for the DB mixer, which meet specs outlined earlier by a comfortable margin. This has been achieved, without source degeneration, by the right choice of the gm/I ratio of the CMOS devices and differential implementation.

The measurements of the transmitting preamplifier show that high gain and adequate input and output impedances, as well as good linearity, can be achieved even if a relatively high amount of power must be delivered. Fig. 14 shows the measured frequency response of the TX preamplifier. The measured iCP of the preamp is -14.6 dBm, which corresponds to $+5.8$ dBm oCP. This translates into more than 3.5-mW power delivered to the 50-Ω load at compression.

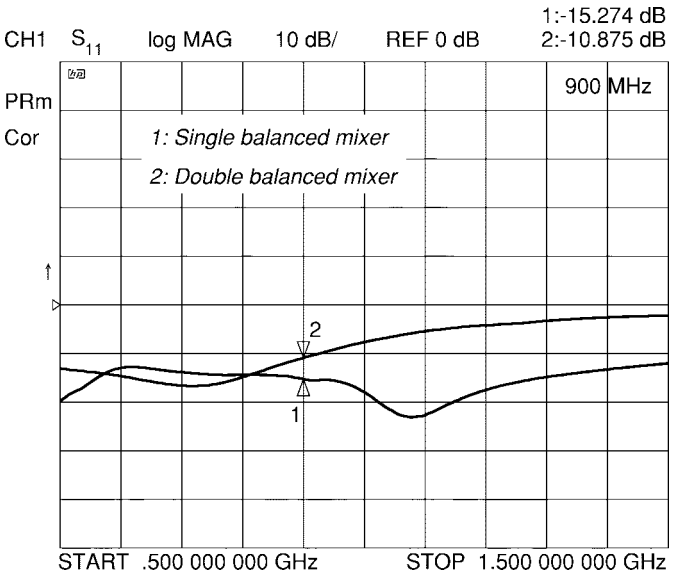

Fig. 12. Measured S_{11} for single- and double-balanced mixer.

VIII. Conclusions

Power consumption is more important than the cost of chips in today's cellular phones. To prove that CMOS is feasible and competitive with BJT's for implementing the RF front end of a GSM receiver, circuits operating at RF frequencies must show competitive current consumption while

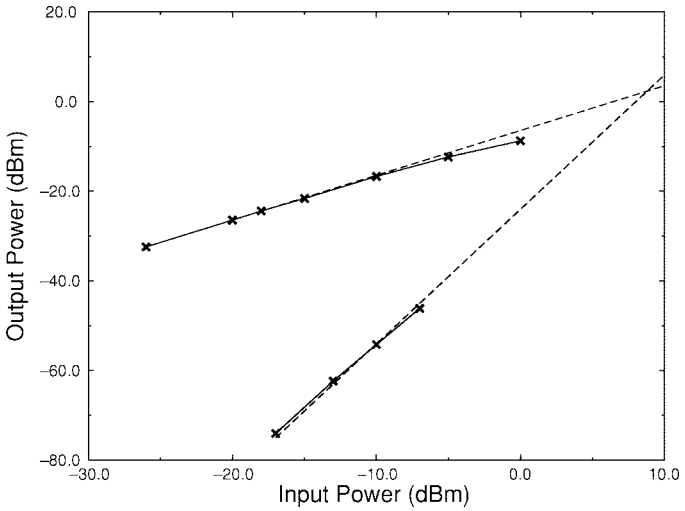

Fig. 13. Measured, input-referred, third-order intercept point iIP3 and −1-dB compression point iCP, respectively, for the double-balanced mixer.

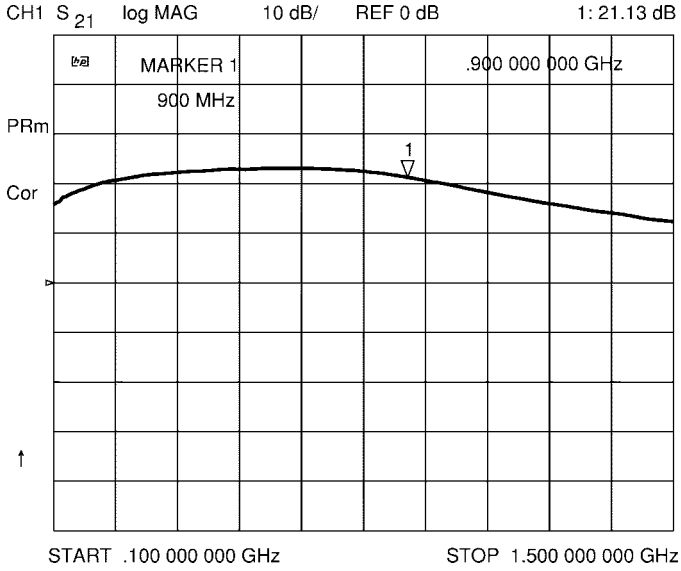

Fig. 14. Measured frequency response of the TX preamplifier.

meeting all specs required by type-approval. Type-approval requirements have been discussed and translated into circuit specs where necessary, and measurements of the front-end integrated circuits reported in this paper show that they are indeed met. We have shown that current consumption lower than today's BJT implementations is indeed feasible by optimizing the front-end design carefully. Excellent noise figures are also shown to be reproducibly obtained for CMOS LNA's and mixers. Controlled experiments also confirm that backgating by substrate resistance can degrade the NF, and as many contacts as possible should be used to ground the substrate.

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