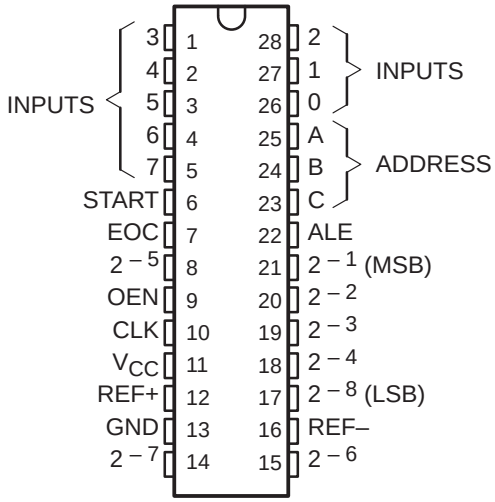
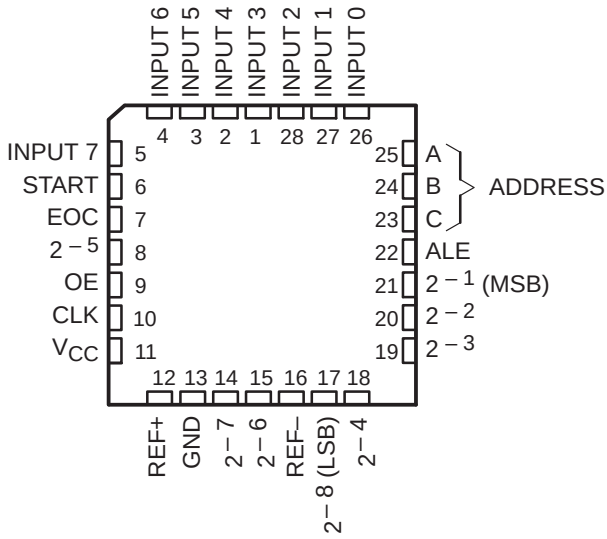
- **Total Unadjusted Error . . . ± 0.75 LSB Max**
- **Resolution of 8 Bits**
- **100-μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonous Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy interface With Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-V Supply**
- **Low Power Consumption**
- **Designed to Be Interchangeable With National Semiconductor ADC0808CJ**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The ADC0808M is a monolithic CMOS device with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched capacitor array, a sample-and-hold, and a successive- approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-V supply and low power requirements make the ADC0808M especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808M is characterized for operation over the full military temperature range of –55°C to 125°C.

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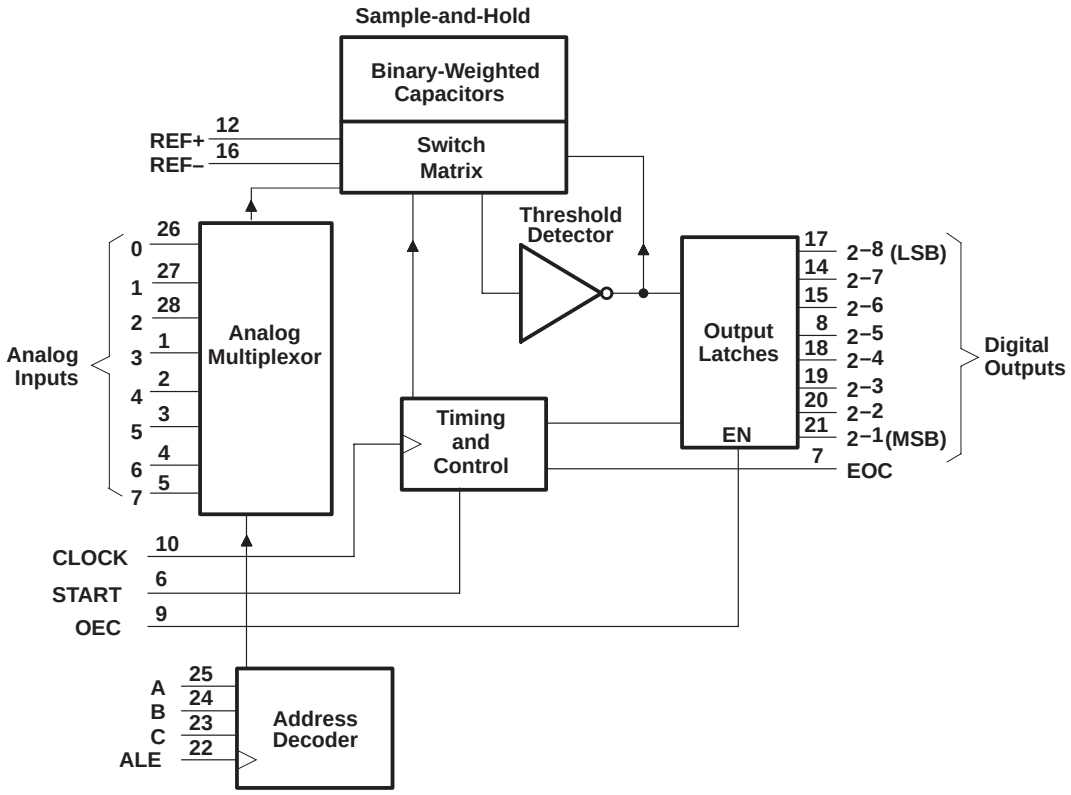
functional block diagram (positive logic)

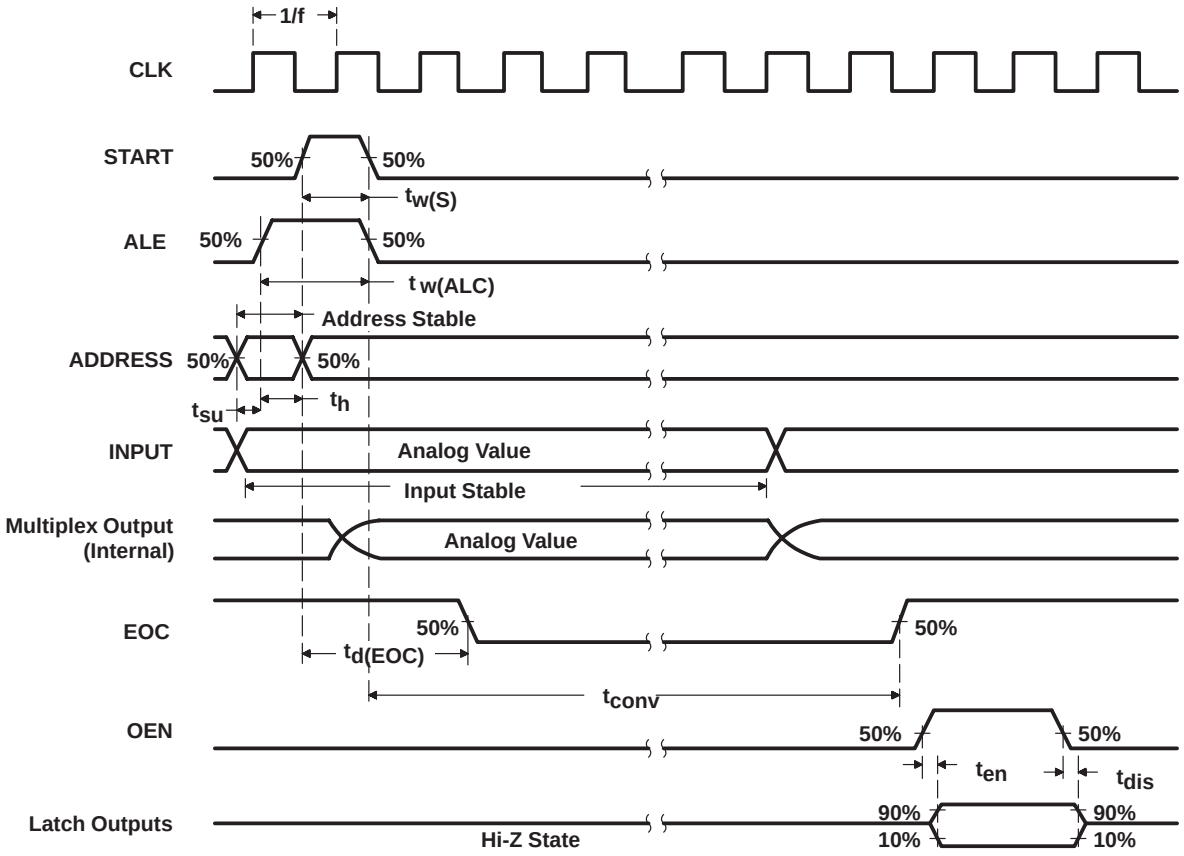


MULTIPLEXER FUNCTION TABLE

INPUTS			SELECTED
ADDRESS			ADDRESS STROBE	ANALOG CHANNEL
C	B	A		
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: Control inputs . . . . . –0.3 V to 15 V
All other inputs . . . . . –0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-}		0	–0.1	V
Differential reference voltage, $V_{ref+}-V_{ref-}$		5		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$			V
Low-level input voltage, V_{IL}			1.5	V
Start pulse duration, $t_{w(S)}$	200			ns
Address load control pulse duration, $t_{w(ALC)}$	200			ns
Address setup time, t_{su}	50			ns
Address hold time, t_h	50			ns
Clock frequency, f_{clock}	10	640	1280	kHz
Operating free-air temperature, T_A	–55		125	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V to 5.5 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = –360 µA	V_{CC}–0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			3	µA
			V_O = 0			–3	
I_I	Control input current at maiximum input voltage		V_I = 15 V			1	µA
I_{IL}	Low-level control input current		V_I = 0			–1	µA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10		pF
C_o	Output capacitance, data outputs		T_A = 25°C		10		pF
	Resistance from REF+ to REF –				1000		kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	V_I = V_{CC},	f_{clock} = 640 kHz			2	µA
		V_I = 0,	f_{clock} = 640 kHz			–2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		–10	–200	
		V_{CC} = 5 V	V_I = 5 V			1	µA
			V_I = 0			–1	

† Typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

timing characteristics, V_{CC} = V_{ref+} = 5 V, $V_{ref–}$ = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		10	640	1280	kHz
t_{conv}	Conversion time	See Notes 4 and 5 and Figure 1	90	100	116	µs
t_{enH}	Enable time, high	See Figure 1		150	360	ns
t_{enL}	Enable time, low	See FIgure 1		90	25	ns
t_{dis}	Output disable time	See Figure 1		200	405	ns
$t_{w(s)}$	Pulse duration, START		200			ns
$t_{w(ALE)}$	Pulse duration, ALE		200			ns
t_{su}	Setup time, ADDRESS		50			ns
t_h	Hold time, ADDRESS		50			ns
$t_{d(EOC)}$	Delay time, EOC	See Notes 4 and 6 and Figure 1	0		14.5	µs

NOTES: 4. Refer to the operating sequence diagram
5. For clock frequencies other than 640 kHz, t_{conv} is 57 clock cycles minimum and 74 clock cycles maximum.
6. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock cycles plus 2 µs.

operating characteristics, T_A = 25°C, V_{CC} = V_{ref+} = 5 V, V_{ref-} = 0 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 4.5 V to 5.5 V, T_A = – 55°C to 125 °C, See Note 7		±0.05		%/V
	Linearity error (see Note 8)			±0.25		LSB
	Zero error (see Note 9)			±0.25		LSB
	Total unadjusted error (see Note 10)	T_A = 25°C		±0.25	±0.5	LSB
		T_A = –55°C to 125°C			±0.75	

† Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V, and all are at T_A = 25°C.

NOTES: 7. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
8. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
9. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
10. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

PARAMETER MEASUREMENT INFORMATION

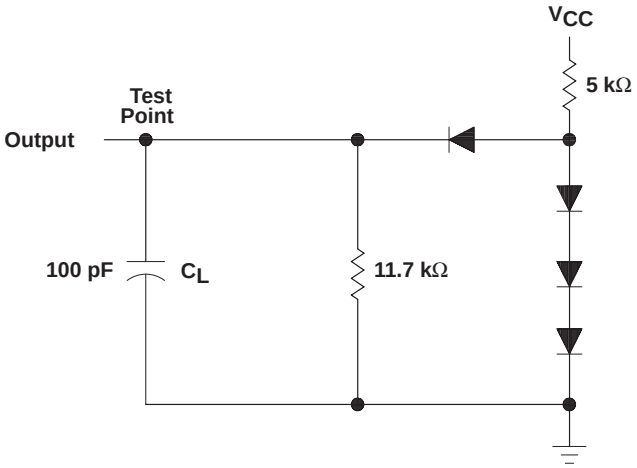


Figure 1. Test Circuit

PRINCIPLES OF OPERATION

The ADC0808M consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 2). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors.The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

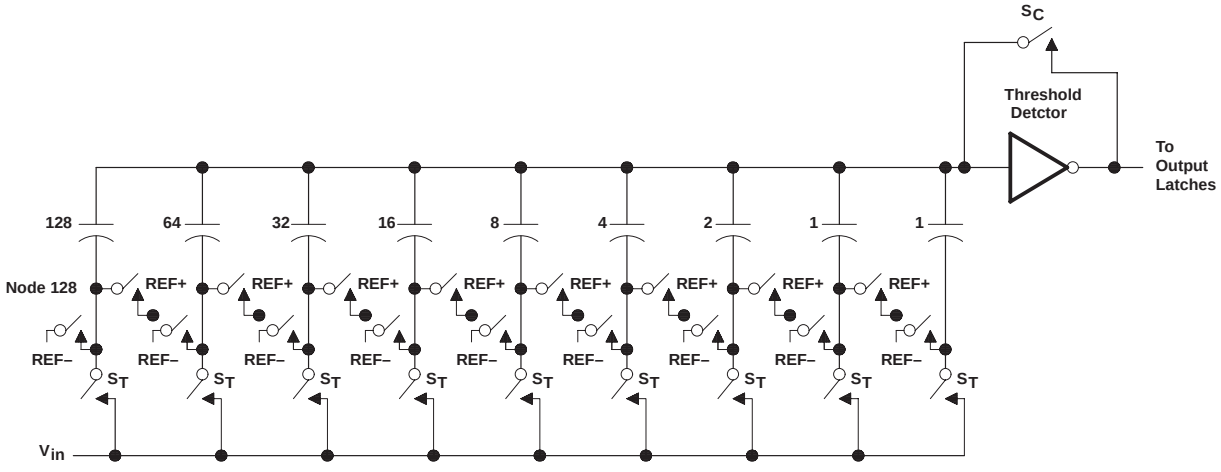


Figure 2. Simplified Model of the Successive-Approximation System

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