# **SIMULINK Laboratory Exercises In Communication Technology**

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#### Abstract

In this paper, we present simulation exercises with emphasis on learning to build blocks and subsystems and integrating them into a communication system. Through these exercises, the students learn to build communication subsystems from the basic building blocks that are available in the SIMULINK library. The subsystems are built as close approximation of instruments and hardware modules that are available in a laboratory. Data sources have included programmable jitter. Students make their own library of these subsystems and use them to build large and complex communication systems such as the BFSK, BPSK, QPSK and QAM systems. Exercises include finding frequency spectrum of analog signals and digital data streams, analog-to-digital conversion, digital modulation systems, phase lock loop operation and frequency synthesizer, coding and decoding processes.

### I. Introduction

Simulation exercises help greatly in learning of complicated systems which otherwise will be difficult to build in a two or three-hour lab class period. Equivalent hardware exercises would require extensive set-up time and frustrating trouble-shooting experience. Moreover, the hardware components and equipments are expensive and have long acquisition times in an educational setup.

The communication circuits and subsystems are now available as merchant integrated circuits. Engineers and technologists in the modern telecommunication industry configure systems and build them from subsystems and ICs. The subsystems, even though procured from multiple vendors, use standard interfaces to enable trouble-free interfacing. The uppermost design issues before the engineers now are interfacing of subsystems. MATLAB SIMULINK [1] is popular software for developing educational exercises. However, several of these exercises use blocks that perform mathematical operations [2]. These blocks have little resemblances to the equipments and hardware units, which are used in practice. In this paper, we present the simulation exercises that enable the students to build equipment-like blocks and construct complete communication systems and simulate, observe and understand parametric variations. A

number of probing questions are asked after simulation of each block and subsystem to test the student's comprehension and satisfaction.

The laboratory comprises of exercises of complex systems such as ASK, PSK, QAM, TDMA and CDMA systems. These systems are well explained in several textbooks in both engineering and technology textbooks in communication <sup>[3]</sup>. The appendix of the paper gives the list of the simulation exercises developed using the idea of this paper.

### II. The Digital Communication System

A typical digital communication system is shown in Fig. 1. The left and right vertical blocks are housed in the transmitter and receiver stations respectively. Data stream from a source is clocked. The data stream is shaped by the transmission filters to reduce the inter-symbol-interference errors. A typical transmission filter is the Root Raised Cosine filter. The pulse-shaped data stream is modulated by a high frequency sine wave carrier to enable transmission on the physical link between the source and destination. The transmitter block amplifies the modulated signal includes the antenna or a device to transmit maximum power on the medium of the link.

On the destination end the Receiver unit includes antenna or a device to collect the maximum signal power. This unit may include selective tuning filters and preamplifiers. The Demodulation unit is based on coherent or non-coherent demodulation comprising of multipliers, mixers and filters. The carrier signal is recovered in coherent demodulation. The receiver filter typically undo pulse-shaping using Root Raised Cosine filter. The last block is where the logic state of the data is determined.

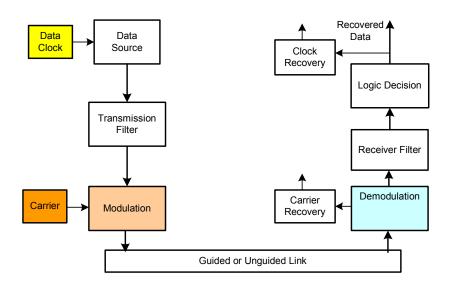


Fig. 1 A simple digital communication system

The data communication designer negotiates several imperfections and interferences such as

Internal noise
Interfering signals and noises
Timing jitters in clock
Inter Symbol Interference errors

We will restrict this paper to the exercises on digital communication from a single data source to a single destination on a wired channel such as a telephone channel. The SIMULINK exercises are aimed for the first course in communication systems, therefore, we will avoid FEC coding and decoding and multiple access topics. Figure 2 shows the SIMULINK model of a system consisting of the Binary phase shift keying modulator /demodulator and band-limited noisy telephone channel. The constituent subsystems are described in the next section.

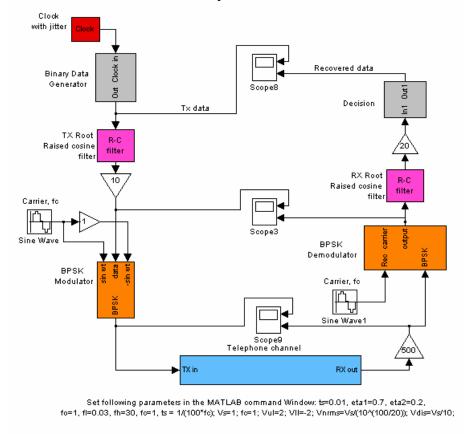


Fig. 2 BPSK System model

### 2.1 Sources

A practical source has non-idealities such as distortion, amplitude saturation and internal noise etc. A digital data source also has timing jitter. As the first exercise, the students build the

models of practical sine wave, triangle and saw tooth sources, pulse source and binary data generator for future use in designing complex communication systems.

### 2.1.1 Data Source

A practical clock-triggered binary data generator contains clock jitter. For illustration, we present the design of a clock triggered binary data generator as shown in Fig. 5.

Pseudo random generator specifications:

Signal: Pseudo random noise, 1Hz, 1/0 V amplitude with seed: 23341

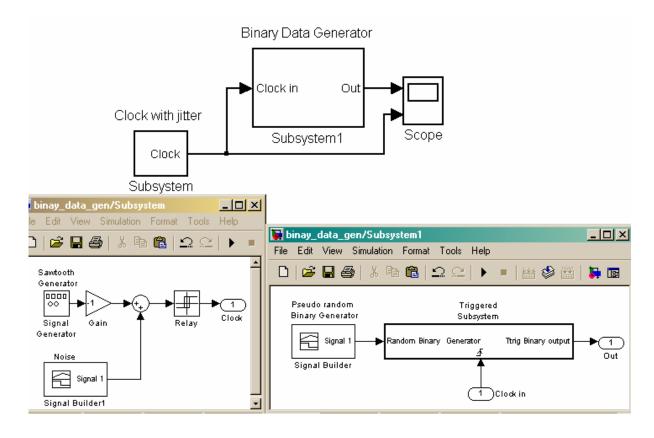
# 1Hz Clock with following specifications:

Saw tooth wave: +/-1V, 1Hz,

Sampled Gaussian noise as the noise source: 10Hz, mean=0.0V, variance=0.2V,

1/0 V amplitude with seed: 23341

Comparator hystersis (Relay block): +/- 0.1 V and 1/0 V amplitude



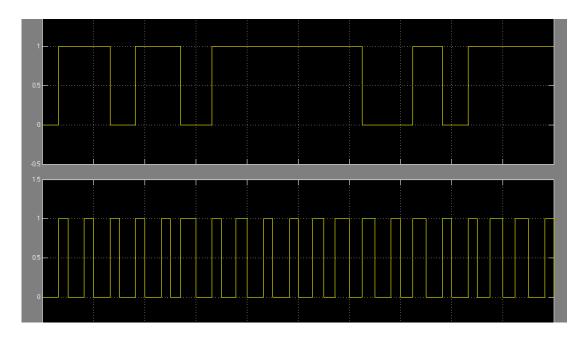


Fig. 3 Clock-Triggered binary generator with programmable jitter

# 2.1.2 Transmission and Receiver Filters

A rectangular pulse when passed through a filter such a telephone channel becomes an exponentially decreasing since wave<sup>[4]</sup>. Adjacent pulses when passed through such a channel,

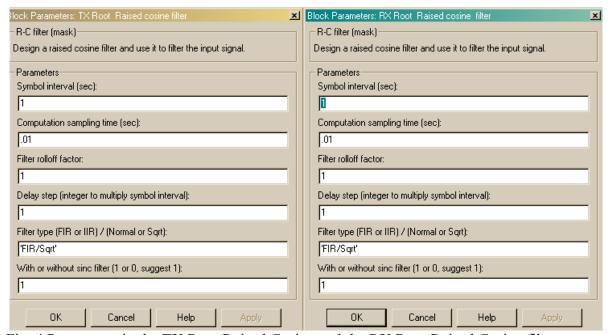


Fig. 4 Parameters in the TX Root Raised Cosine and the RX Root Raised Cosine filters

generate inter symbol interference, each pulse representing a symbol. Special filter can be used to minimize this inter symbol interference. In one of the methods, two special purpose filters, called the Root Raised Cosine filters, are inserted in the transmitter and the receiver systems before and after respectively, the modulation/demodulation with the high frequency carrier. Set the following parameters in the two filters as shown below in Fig. 6.

A delay of one symbol period is inserted in both filters to stabilize the filter performance.

#### 2.1.3 BPSK Modulator

The BPSK modulator is basically a two-position switch, controlled by the data stream. The high-level in data allows the positive carrier signal (0° phase) and the low-level data allows the negative carrier signal (180° phase) on the output terminal.

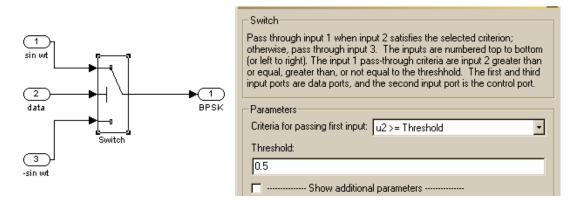


Fig. 5 BPSK Modulator

### 2.1.4 Telephone Channel

The telephone channel is a limited bandwidth 30Hz-3000 kHz channel with attenuation and additive Gaussian noise. We have modeled the telephone channel such that the carrier frequency of 1Hz lies in the middle of the pass band. The transfer function of the band pass filter is set as,

$$T(s) = \frac{2\pi fh s}{s^2 + 2\xi 2\pi (fl + fh)s + (2\pi)^2 fl fh}$$

where fl: lower cutoff frequency

fh: upper cutoff frequency  $\xi$ =0.7 the damping factor.

Set the following parameters:

Attenuation:  $1/(2\pi 30)$ 

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Bandwidth: 0.03Hz-30Hz

Limited bandwidth noise power: 2 mW Sample time for the noise: 1 second

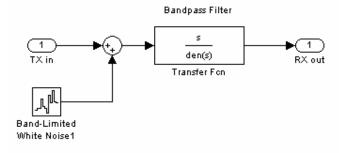


Fig. 6 Telephone channel block

### 2.1.5 BPSK Demodulator

The BPSK demodulator is modeled by a preamplifier, multiplier, an input that takes in the recovered carrier signal oscillator that generates the carrier frequency of 1Hz, a low pass filter with a frequency of a cutoff frequency of 1Hz.

Preamplifier: 10 Low pass cut-off frequency: 1Hz

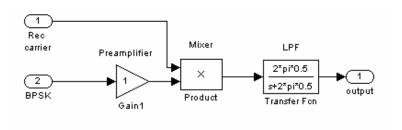


Fig. 7 BPSK Demodulator block

# 2.1.6 Logic Determination in Receiver

The logic Decision circuit in the receiver is comparator with hysteresis:

Switch On point: +0.1 V Switch Off point: -0.1 V

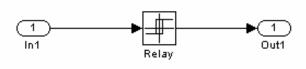
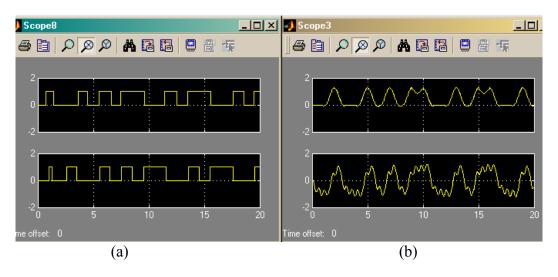
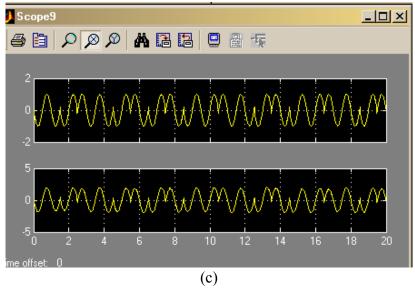


Fig. 8 Logic determination block

#### 2.1.7 Simulation Waveforms

The simulation waveforms are shown in Fig. 9. Note that the recovered data in Fig. 9 (a) is delayed in time. This delay is intentional to achieve stabilization in the recovered data. Figure 9 (b) shows the ISI-minimized shaped transmitted data stream. Figure 9 (c) and (d) show the recovered and transmitted and recovered carrier and clock data waveforms. The intentional delay introduced is also necessary to avoid the initial transition period over the recovered carrier and the recovered clocks waveforms stabilize. Figure 9 (e) shows the received and the transmitted BPSK waveforms. The simulation uses data clock rate equal to the carrier frequency for easy understanding of the BPSK waveforms. Students are asked to simulate this system for different noise powers in the telephone channel, different logic decision thresholds, different filter bandwidths and different jitter amounts.





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- Fig. 9 a) The transmitted and recovered data streams
  - b) The data stream after shaping by transmission filter
  - c) The transmitted and received BPSK data stream

# III. Testing Comprehension

Students are required to explain in their final lab report the function of each basic building block and subsystem in their own words. Doing so makes the students to revisit the blocks they have built and used in the simulation exercise. If the students do labs in teams, then each student is required to give individual explanations. Some more probing questions may be added to test their comprehension. We list the sample of questions that are related to above exercise:

- 1. What do you understand by jitter in data stream?
- 2. Describe the operation of the block, clock with controllable jitter.
- 3. Describe the operation of the random data generator in your words.
- 4. Describe the operation of BPSK demodulator in your words.
- 5. Why is the recovered data delayed in time?
- 6. How do the Root Raised Cosine filters help in data transmission?

### IV. Conclusion

The SIMULINK exercises are designed to enhance the learning of communication systems through building simpler blocks and subsystems. The subsystems are designed to be close replicas of the instruments used in the laboratory. These exercises are being used in the first course in communication technology. Verbal responses from the students show that they can better comprehend the functioning of basic communication blocks and subsystems.

# **Reference:** (superscript in body)

- [1] "MATLAB SIMULINK", Mathworks Inc.
- [2] "Contemporary Communication Systems Using Matlab and SIMULINK", John G. Proakis, M. Salehi and G. Bauch, Second Edition, Thompson-Brooks/Cole.
- [3] "Electronic Communication systems", 6th Ed. -Wayne Tomasi, Prentice-Hall, 2001
- [4] "Digital communications", 2<sup>nd</sup> Ed. Andy Bateman (Addison-Wesley)

#### **Appendix**

List of SIMULINK laboratory exercises:

- 1. Frequency spectrum of periodic signals
- 2. Frequency spectrum of data stream
- 3. Filters
- 4. Phase Locked Loop
- 5. ASK Communication System

- 6. FSK and BPSK Communication System
- 7. 16-QAM Communication System

# **Biography**

JAI AGRAWAL is a Professor with joint assignment in Electrical and Computer Engineering Technology and Electrical & Computer Engineering. He received his PH.D. in Electrical Engineering from University of Illinois, Chicago, in 1991, M.S. and B.S. also in Electrical Engineering from I.I.T. Kanpur, India in 1970 and 1968 respectively. Professor Agrawal has worked recently for two years in optical networking industry in the Silicon Valley in California. Professor Agrawal is the Founder Advisor to Agni Networks Inc., San Jose, California. His expertise includes optical networking at Physical and Data link layers, optical and WDM interface, SONET and Gigabit Ethernet and analog electronic systems. He is the author of a Textbook in Power Electronics, published by Prentice-Hall. His professional career is equally divided in academia and industry. He has authored several research papers in IEEE journals and conferences.

OMER FAROOK is a member of the faculty of the Electrical and Computer Engineering Technology Department at Purdue University Calumet. Professor Farook received the Diploma of Licentiate in Mechanical Engineering and BSME in 1970and 1972 respectively. He further received BSEE and MSEE in 1978 and 1983 respectively from Illinois Institute of Technology. Professor Farook's current interests are in the areas of Embedded System Design, Hardware – Software Interfacing, Digital Communication, Networking, C<sup>++</sup> and Java Languages.

CHANDRA R. SEKHAR is a member of the faculty of the Electrical and Computer Engineering Technology at Purdue University Calumet. Professor Sekhar earned a Bachelor's Degree in Chemistry from the University of Madras (India), a Diploma in Instrumentation from Madras Institute of Technology and Master's Degree in Electrical Engineering from University of Pennsylvania. Professor Sekhar's primary teaching and research focus is in the areas of Biomedical and Process Control Instrumentation and Clinical Engineering.