

ADVANCED GLOBAL NAVIGATION SATELLITE SYSTEM RECEIVER DESIGN

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Abstract

The research described by this thesis was undertaken at a very timely moment in the development of global navigation satellite systems (GNSS). During the course of this work the signal structure of an entirely new generation of GNSS signals was been defined. The first satellites producing a new range of different coding and modulation schemes have been launched, initiating the modernisation of the American GPS and the introduction of the European Galileo system.

An important aspect of the new signal structure for both GPS modernisation and Galileo is an entirely new kind of modulation called BOC (Binary Offset Carrier). Despite certain advantages this modulation comes with the notorious characteristic of a multi-peaked correlation function. In our view all known receivers, or receiver principles, have problems with this: either because the receiver is not fail safe and is potentially unreliable (the so-called *bump-jumping* receiver); or the multi-peaks are eliminated at the very substantial cost in much degraded accuracy. During my research under Dr Hodgart what seems to be an entirely new and original method has been developed which entirely solves the problem of tracking BOC. The problem of multi-peaks goes away and there is no loss of potential accuracy. This thesis describes in detail this invention and the first experimental results.

This research was carried out at the University of Surrey under the joint supervision of Surrey Space Centre and Surrey Satellite Technology Ltd. Shortly before this work began SSTL achieved a contract to design and build the first ever test satellite (Giove-A) of the Galileo signals and technology. This research contributed to the design and manufacture of a Galileo signal generator which was flown on-board the satellite (launched December 2005). Expanding upon SSTL's existing designs this work enabled the design and creation appropriate receivers to monitor the transmissions both in ground based emulations and real live tests after launch. These designs are intended to be the core of future SSTL space receivers. This thesis describes in detail the creation of both transmitter and receiver architectures for the testing and evaluation of GNSS signals.

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ABBREVIATIONS

ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
AltBOC	Alternate Binary Offset Carrier
AMBA	Advanced Microprocessor Bus Architecture
ASIC	Application Specific Integrated Circuit
BOC	Binary Offset Carrier
BPSK	Binary Phase Shift Keyed
C/A	Coarse Acquisition
CASM	Coherent Adaptive Subcarrier Modulation
CBOC	Composite Binary Offset Carrier
CFI	Customer Furnished Item
COTS	Commercial Off The Self
CW	Continuous Wave
DAC	Digital to Analogue Converter
DCM	Digital Clock Module
DCO	Digitally Controlled Oscillator
DE	Double Estimator
DLL	Delay Locked Loop
E	Early
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FLL	Frequency Locked Loop
FPGA	Field Programmable Gate Array
GCLK	Global Clock
GEO	Geostationary Earth Orbit
GETR	Galileo Experimental Test Receiver
GJU	Galileo Joint Undertaking
GNSS	Global Navigational Satellite System
GPS	Global Positioning System
HDL	Hardware Description Language
I	In-phase
IF	Intermediate Frequency
IMP	Inter-Modulated Product
IOB	Input Output Block
L	Late
LC	Inductor Capacitor
LEO	Low Earth Orbit
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LUT	Look Up Table
MAG	Magnitude
MBOC	Multiplexed Binary Offset Carrier
MEO	Medium Earth Orbit
MFUU	Modulator Frequency Up-converter Unit

MGD	Multiple Gate Discriminator
MSB	Most Significant Bit
NMGU	Navigational Message Generation Unit
P	Prompt
PC	Personal Computer
PIF	Prototype Intermediate Frequency
PLL	Phase Locked Loop
PRN	Pseudo Random Noise
PSD	Power Spectral Density
PSK	Phase Shift Keying
PVT	Position Velocity Time
Q	Quadrature
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right-Hand Circularly Polarised
RT	Radiation Tolerant
SAW	
SCC	Sub-Carrier Cancellation
SGR	Space GNSS Receiver
SLL	Sub-carrier Locked Loop
SNR	Signal to Noise Ratio
SSB	Single Side-Band
SSC	Surrey Space Centre
SSTL	Surrey Satellite Technology Limited
SV	Space Vehicle
TCXO	Temperature Controlled Crystal Oscillator
TMBOC	Time Multiplexed Binary Offset Carrier
TTFF	Time To First Fix
TWT	Travelling Wave Tube
UART	Universal Asynchronous Receiver-Transmitter
VE	Very Early
VL	Very Late

SYMBOL LIST

Λ	Idealised PRN code correlation function
\square	Pulse equivalent to a PRN code chip
∇^Λ	PSK equivalent early minus late discriminator function
$\hat{\phi}$	Receiver estimated carrier phase
$\hat{\tau}$	Receiver DLL estimated PRN code delay
$\tilde{a}(t)$	Orthogonal PRN code sequence
w'	Time adjacent correlation result
$\Delta\hat{\phi}$	Receiver estimated carrier phase difference between epochs
$\tilde{b}(t)$	Orthogonal BOC modulated code sequence
\mathcal{W}	Idealised BOC correlation function
\mathcal{W}^I	Idealised BOC discriminator function

$\tilde{s}(t)$	Orthogonal sub-carrier waveform
$\hat{\tau}^*$	Receiver SLL estimated code delay
\hat{d}	Navigational data estimate
$\hat{\tau}^+$	Corrected SLL delay estimate
ω	Carrier frequency
λ	Carrier wavelength
κ	Spectral separation coefficient
Σ	Mean square timing timing jitter
σ	Normalised standard deviation of timing jitter
ε	Timing error
η	One sided white noise density
Δ	Normalised discriminator spacing
α	Coefficient of reflection
ϕ	General phase shift term
τ	Time delay of PRN code sequence
ρ	Pseudorange
$\Delta\tau$	PRN code delay error
$\Delta\phi$	Carrier phase difference between epochs
$\theta(t)$	Composite phase modulation introduced for interplex modulation
τ_{DCO}^*	Sub-carrier DCO phase (ms)
ω_b	Centre frequency of IF signal
τ_{DCO}	Code DCO phase (ms)
ϕ_{DCO}	Carrier DCO phase
Δf	Frequency error
ω_n	Natural loop frequency
σ_N	Standard deviation of the synthesised noise
β_R	Two sided receiver front-end bandwidth
λ_{SC}	Sub-carrier wavelength
A	Signal Amplitude
$a(t)$	PRN code sequence
b	Normalised receiver front-end bandwidth
$b(t)$	BOC modulated waveform
B_d	Data bandwidth (two-sided)
B_L	Loop bandwidth
B_S	Signal bandwidth (two-sided)
c	Speed of light
C	Carrier power
$C(t)$	Composite modulation of BOC sub-carrier and/or PRN code sequence
C_{dLi}	Code lock indicator
C_{rLi}	Carrier lock indicator
$d(t)$	Navigational data message
e_ϕ	PLL estimated carrier phase error
e_ω	FLL estimated carrier frequency error
e_τ	DLL estimated PRN code delay error
e_{τ^*}	SLL estimated PRN code delay error
f_ϕ	Integrated carrier phase error
f_ω	Integrated carrier frequency error

f_C	PRN code chipping rate
f_{DAC}	Sampling frequency of DAC
f_N	Update frequency of noise samples
f_S	BOC sub-carrier frequency
f_s	Sampling frequency
G	LFSR polynomial
G_τ	Correlation gain with PRN code delay error
G_F	Correlation gain with frequency error
$i(t)$	Interfering signals
ICP	Integrated carrier phase
$ISCP$	Integrated sub-carrier phase
k	Loop gain
K	Total number of early late gates
k_ϕ	Carrier to code Doppler scaling factor for a coherent receiver
k_ω	Carrier to code Doppler scaling factor for a incoherent receiver
k_{ϕ^*}	Carrier to sub-carrier Doppler scaling factor for a coherent receiver
k_{ω^*}	Carrier to sub-carrier Doppler scaling factor for a incoherent receiver
K_{FD}	Frequency discriminator gain
K_{PD}	Phase discriminator gain
K_{CD}	Code discriminator gain
K_{DCO}	DCO gain
K_N	Ratio between the DAC sampling rate and noise update rate
K_{SC}	Ratio between the DAC sampling rate and PRN code rate
L_D	Length of data bit (ms)
m	Modulation index
n	LFSR length
N	Number of chips in PRN code sequence
$n(t)$	Additive noise
N_0	Noise density
NF	Theoretical receiver noise floor value
N_{HC}	Number of half chip per code epoch
P	Signal power
p	Integer count of early late gates
R	Autocorrelation function
$S(\omega)$	Signal power spectral density
$s(t)$	Square sub-carrier waveform
$S(t)$	PSK signal representation
$ScLi$	Sub-carrier lock indicator
$sqc(t)$	Square cosine waveform
T	Integration time
T_τ	Transmit time from DLL
T_{τ^*}	Transmit time from SLL
$t(m)$	Cross correlation values
T_C	PRN code chip period
T_D	Early to late discriminator spacing
T_{DC}	Code loop discriminator spacing
T_R	Receiver estimated time
$trc(t)$	Triangular cosine function
Trs	Trapezoidal sine function
$trs(t)$	Triangular sine function

T_S	Sub-chip period
T_T	Transmission time
$u(t)$	Received signal representation
$v(t)$	Received signal multiplied by receiver generated replicas
w	Correlation result
$w(t)$	Noise sample
w_s	Search correlation
$X(s)$	Input to filter (s domain)
$x(t)$	Input to filter (time domain)
X_{CC}	Carrier cycle counter
X_D	Data bit counter value
X_E	Epoch counter value
X_{HC}	Half chip counter value
X_{SC}	Sub-carrier cycle counter
$Y(s)$	Output of filter (s domain)
$y(t)$	Output of filter (time domain)
$Z[k]$	Random number at sample k

Acknowledgements

First and foremost I would like to express my gratitude for the significant theoretical support offered by my academic supervisor Dr Stephen Hodgart. Much of this was in unpublished technical memoranda which duly appear here in the various appendices. I would also like to acknowledge the contribution of my industrial supervisor Dr Martin Unwin for his invaluable guidance, practical knowledge and instruction

This research has been supported by the Location and Timing Knowledge Transfer Network, EPSRC, Surrey Satellite Technology Limited and the Surrey Space Centre. Many individuals from SSTL and SSC have helped and encouraged me during my studies and my thanks to them all. I am particularly indebted to Michael Meier for his expert practical knowledge and teaching. Also, I would like to thank the members of the GNSS team at SSTL for their help and friendship.

I thank my family and my extended Finnish family for their love and support over the past years. Finally my greatest thanks go to Hanna-Leena for inspiring and encouraging me throughout and keeping me somewhat sane.

1 Introduction

This chapter introduces the various partnerships that have invested in and contributed to this research project. A brief history of the contributing parties is given to provide a context for the project. Following this, a short description of the content in the subsequent chapters of this report is given.

1.1 The CASE PhD studentship

The CASE PhD studentship was created by the Electrical and Physical Sciences Research Council (EPSRC) to promote collaboration between industry and academia through research with common goals. EPSRC set up a number of groups, each devoted to a specific area of electrical and physical sciences and called these Faraday partnerships. Each partnership is given funding to develop the interaction between industry and academia through research in its specific area. The Pinpoint Faraday partnership is devoted to research into the applications of Global Navigation Satellite Systems (GNSS) and enabled the core funding for this research.

The goals of the CASE research are expected to satisfy both industrial and academic partners. For this reason the CASE projects tend to contain more practical work than the traditional theoretical PhD.

The industrial partner of this CASE studentship was Surrey Satellite Technology Limited (SSTL). SSTL was formed as a spin-off company from the University of Surrey in 1985. Since then, SSTL has been involved in 26 satellite missions and become a world-leader in supplying small satellites platforms. SSTL manufactures its own range of GNSS receivers, which are operated on-board its own satellites and supplied externally as sub-systems. The academic partner was Surrey Space Centre (SSC), who specialise in all areas of space research including GNSS at the University of Surrey. Common office locations and the close working relationship between SSTL and SSC provide the ideal environment for the CASE student.

1.2 The future of GNSS

The generic term GNSS is currently used to encompass two operational systems : the US Global Positioning System (GPS) and the Russian (GLONASS). Although originally conceived for military use, in recent years civilian use of GNSS has increased rapidly. Recent market research [Research and Markets 2006] has projected the worldwide market value of GPS as reaching \$22 billion by 2008. A huge ever-expanding range of applications for GNSS receivers has resulted in their adoption into many aspects of daily modern life. In turn, the number of GNSS applications for space-borne users has also increased. GPS is predominantly used for most applications mainly due to smaller numbers of operational GLONASS satellites. The US has already started its campaign of GPS modernisation, with two block IIR-M satellites currently operational and potentially five more to be launched in 2007.

GPS modernisation aims to improve upon the existing system by broadcasting additional military and civil signals. This is intended to satisfy the increasing civil demand for high-precision dual frequency systems. However, competition for the already large GNSS market is set to increase with the introduction of the European GNSS, Galileo.

This new generation of GNSS will provide more satellites transmitting a range of high-bandwidth, high precision signals with precise ephemeris and integrity monitoring. The new signals can potentially provide a number of performance advantages over the existing systems. However, the new complex signal specifications require new receiver architectures and new techniques to achieve signal acquisition and tracking.

This research project was formed to study the impact and implications of new generation GNSS on receiver design with emphasis on space applications. The expected outcomes of this project were as follows.

- To further develop SSTL's space GNSS receiver designs – Providing a platform capable of receiving the new generation of GNSS signals in order to derive benefit for space applications.
- To analyse the impact of the new GNSS on receiver design – Providing a comprehensive comparative study of the receiver techniques required for receiving future GNSS signals, while developing novel, beneficial approaches where possible.

This thesis describes the work carried out to achieve these goals, with particular emphasis given to a novel technique for tracking Binary Offset Carrier (BOC) modulated signals.

The work described in this thesis was carried out at a very timely moment in the development of global navigation satellite systems. The world as a whole, with its billions of potential customers, is now perceived as a customer of such systems, not just the military and specialist users. During the period of my work (starting from September 2003) there have been important international agreements and developments, which have confirmed or at least recommended the structure of entirely new signals. A new range of different coding and modulation schemes has been conceived to serve an expanding multi-faceted market. The Americans are implementing significant changes and hopefully improvement in the development of the next generation of GPS. There may well be implemented soon the independent European Galileo system, which will also adopt new codes and modulations, as well as the latest technology in atomic clocks. As a student of Surrey University I was well placed to make a contribution to these challenging developments at both theoretical and practical level under the joint auspices of Surrey Space Centre and Surrey Satellite Technology Ltd. Shortly before this research began SSTL achieved a contract to design and build the first ever test satellite Giove-A of the Galileo signals and technology. The satellite was launched on the 28th of December 2005. The opportunity existed then to design and build a test transmitter (see [Blunt 2005]) for installation on the satellite before launch; and also to design and build appropriate receivers to monitor the transmissions both in ground based simulations or emulations and real live tests after launch. I am grateful to the technical and financial support

from the GNSS team of the company headed by one of my supervisors Dr Martin Unwin, which made this possible.

Before describing in detail the point, purpose and potential novelty of these practical developments, the beginning chapters of this thesis lead up to a description of a theoretical novelty, initiated jointly by myself and my other supervisor Dr Stephen Hodgart of Surrey Space Centre. An important feature of the new signals for both GPS modernisation and Galileo is an entirely new kind of modulation called BOC (Binary Offset Carrier). A family of modulations based on BOC are characterised by a sub-carrier modulation imposed on the code-modulation. The effect is well known to create a split spectrum (see Figure 3-9). It is perhaps surprising that a family of signals using this modulation and their precise specification was agreed internationally (see Table 3-2 and Table 3-3) for both new GPS and Galileo, despite the reservations published in many papers on the practical difficulties in realising a good working BOC receiver. The notorious perceived difficulty is due to the characteristic multi-peaked correlation function. In our view all known receivers, or receiver principles, have problems with this: either because the receiver is not fail safe and is potentially unreliable (the so-called *bump-jumping* receiver [Fine and Wilson 1999]); or the multi-peaks are eliminated at the very substantial cost in much degraded accuracy [Bello and Fante 2005].

With my work under Dr Hodgart what seems to be an entirely new and original method has been developed which entirely solves the problem of tracking BOC. The problem of multi-peaks goes away and there is no loss of potential accuracy. The invention has been assigned to the University of Surrey, and a professionally drafted patent application filed with the Patent Office from August 2006 with ourselves named as joint inventors. All simulations, emulations and further practical work seem to show that the invention does indeed work and has no problems. There is no indication in any published work that others have perceived our way to the solution. This thesis describes in detail this invention and the first experimental results. When in due course it is published our work hopefully will re-assure conservative technical and political interests internationally, if such exist, that it is now safe to go ahead with BOC (and also AltBOC for the Europeans).

1.3 Outline of thesis

This thesis consists of 11 chapters with the following content.

Chapter 2 describes the driving forces behind this project and the motivation for research in this area. The specific goals of the research are described, which satisfy both the industrial and academic requirements of the research. To emphasise the need for the research examples of space applications to which this work may benefit are given.

Chapter 3 gives an overview of the current and future GNSS signal characteristics. This is essential to provide background for the thesis, which is fundamentally about the new techniques and approaches required to transmit and receive these signals. Details of the modulation, multiplexing and coding schemes are given along with mathematical representations of current and future GNSS signals.

Chapter 4 provides an analysis of the advantages and disadvantages of BOC modulation with comparison to the existing modulation techniques. The effects of BOC on the transmitted frequency spectrum are described and detailed comparative analysis of the tracking and multipath performance of BOC modulation is given. Chapter 5 gives a detailed theoretical description and performance analysis of current and future GNSS receiver search, acquisition and tracking techniques. Firstly, current GPS receiver techniques are described in depth covering both coherent and incoherent systems. Following this, a comparison is given of the techniques currently proposed by the literature in order to successfully search for and track BOC signals. Each scheme is compared with consideration of the receiver acquisition speed, tracking sensitivity and the hardware impact of the technique.

Chapter 6 provides a detailed theoretical description and performance analysis of the novel Double Estimating (DE) BOC receiver, which was developed during this research. A comprehensive description of DE technique is given, showing how it can be applied to coherent and incoherent BOC systems and to the Alternate BOC (AltBOC) modulation. The technique is compared against the BOC tracking schemes

identified in Chapter 5 and a number of advantages are found for both performance and hardware considerations. The practical issue of distortions or asymmetry in transmitted BOC spectrums and its effect on receiver tracking techniques are also analysed. Further advantages are identified for the DE BOC tracking technique while operating with distorted signals.

Chapter 7 describes hardware implementations of GNSS signal generators. Emphasis is given to the SSTL approach to implementing a Galileo signal generator on the Giove-A satellite, which this research has contributed to. This efficient and elegant approach to generating GNSS signals is capable of producing all variations of signals that have been proposed for the future GNSS. Examples of signals from an Intermediate Frequency (IF) bench prototype signal generator and the flight module flown on Giove-A are given. The hardware implementation of a digital noise generator in the signal generator is also described. This noise generator can be used to emulate various levels of additive Gaussian noise for receiver bench testing.

Chapter 8 provides a in-depth look at the SSTL Space GNSS Receiver (SGR) design and follows on to describe the development of a Prototype IF (PIF) receiver, designed to receiver future GNSS signals. Firstly, an overview of the SSTL SGR architecture is given to provide a background receiver design and identify specific areas that can be improved by this research. Subsequently, the design of the PIF receiver architecture is then described, which is intended to replace and enhance many of the core SGR components. The PIF receiver platform also has been used to provide a bench demonstration and evaluation of the DE BOC tracking technique detailed in Chapter 6. The adaptations required to the correlator hardware elements, processor software to implement the DE technique are presented.

Chapter 9 described the testing of the PIF receiver using current and future GNSS signals. Methods for deriving measurement data from the receiver while operating the DE BOC tracking technique and evaluating the performance of the low-level receiver functions are given.

Chapter 10 shows the development and testing of a prototype receiver based on a single FPGA. The receiver was tested with live signals from both the GPS constellation and the Galileo E1 signal from Giove-A satellite.

Chapter 11 describes the contributions made to the field of GNSS by this research. Each contribution is detailed with a description of its potential benefit to the GNSS community. Following this suggestions are made for future research into the areas covered by this research. These include the exploitation of a patent filled for the novel BOC tracking scheme developed during this research.

2 Background, motivation and goals

In order to judge the merit of this research it is important to understand how the project came into being and its potential impact to GNSS academia and industry. In this chapter the driving forces behind this research and the history of its conception are discussed. To provide a context for the research, examples of GNSS receiver applications in space are given, with emphasis on the research activities at SSC and SSTL. Following this, the aims of the research are described, which, given the nature of the CASE studentship, contain a strong industrial emphasis to reflect the research investment by SSTL.

2.1 SSC, SSTL, satellites and GPS

In 1993 SSTL and SSC pioneered the use of GNSS in space through the first operation of a GPS receiver on a micro-satellite in low-earth orbit (LEO). The receiver was used to provide the satellite with position, velocity and time (PVT) information [Unwin 1995], which enabled determination of the satellite's orbit. The first receiver flown by SSTL in orbit was manufactured and adapted for operation in space by the GNSS receiver manufacturer Trimble. Since then SSTL have produced their own space GPS receivers (SGR). The SGR receivers are operated on SSTL's own missions and have also been supplied to ESA, NASA and the US Air-Force.

As the SGR designs have progressed they have enabled a variety of applications. In 1999 the 24-channel SGR-20 was flown on the Uosat-12 satellite. This receiver can process signals on four separate antennas with six channels devoted to each antenna. This enabled a demonstration of attitude determination using GPS by comparing the signals across the antennas [Purivigraipong *et al* 2000]. Further research has taken place to provide a GPS attitude system which is more robust to multipath errors, again making use of real data and demonstrations using the SSTL hardware [Duncan *et al* 2006].

On-board the UK-DMC micro-satellite SSTL have an adapted version of the SGR-10, which is pioneering research into the use of sea-state monitoring with GNSS signals

[Gleason *et al* 2005]. The experimental receiver is specially designed to receive GPS signals reflected back to the satellite from the ocean surface. Again this is supported by research from SSC into modelling and simulating the scatter of the signal with the ultimate aim of determining quantities such as ocean roughness, wave height and wave direction. The acquisition of real data from the satellite has successfully demonstrated the credibility and validity of this technology and fuelled research into this area.

Another experimental SSTL receiver has been flown on the Giove-A satellite, specially designed to operate in a high-earth orbit (HEO) with the potential of providing a low-cost receiver for geostationary earth-orbits (GEO) in the future [Steenwijk *et al* 2006]. This receiver is adapted to acquire and track extremely weak GPS signals in order to obtain PVT information while in an orbit outside the transmitting GPS constellation. Again complementing SSTL's advances in receiver designs this application provides a number of research challenges currently under investigation at SSC, including weak signal acquisition, weak signal tracking and orbit estimation.

Each of the above applications can potentially benefit through advances in GNSS receiver technology provided by this research. Specific aims to benefit GNSS attitude, GNSS remote sensing and GEO GNSS receivers are given in the following section of this chapter.

In 2003 SSTL was awarded the contract to design and manufacture the first Galileo test satellite, Giove-A. This satellite's mission was to claim the frequency bands allocated to the European Community by transmitting representative signals in those bands. Also, the satellite provides a demonstration of a number of key technologies required by the Galileo programme. In December 2005, Giove-A was launched and has successfully claimed the Galileo frequency bands.

The contract to manufacture Giove-A has provided SSTL and SSC with a unique opportunity to study, analyse and evaluate the impact of the next generation of GNSS (GPS modernisation and Galileo) signals on receiver design. Under the Giove-A contract SSTL has developed a Galileo transmitter capable of producing

representative Galileo signals, which this research has contributed to (see Chapter 7). This access to the early Galileo specification, representative signal generators and real signals from space has been an enabler and a driver of this research.

The working relationship between SSC and SSTL has already provided many valuable contributions to the world of GNSS. The partnership strikes a rare balance which many organisations aspire to; between the industrial ‘market pull’ of a commercial company and the ‘technology push’ driven by academia. This partnership is entirely in tune with the spirit of the EPSRC CASE studentship bringing industry and academia together through research with mutual goals.

2.2 Research objectives and goals

The aim of this research was to analyse the impact of the next generation in GNSS (GPS modernisation and Galileo) and determine the advances required by receiver architectures to take advantage of these new systems, providing novel approaches where possible. Emphasis was given to developing receiver architectures for small satellite applications, although the work also provides significant technical value to the terrestrial applications of GNSS.

SSTL have developed a range of space GPS receivers [SSTL 2007] and have pioneered a number of novel space applications. However, the current design is based on an aging chipset that has no flexibility to adapt to the signal specifications proposed for GPS modernisation and Galileo. In order to continue the evolution of SSTL’s SGR family of receivers and benefit from the potential of the future signals, a new high-performance flexible receiver architecture is required. Therefore, a primary industrial and commercial aim of this project was to remove the dependency of the SGR range on an aging and potentially obsolete chipset.

Many scientific space missions require accuracy greater than the typical 10 metre accuracy obtained through single frequency GNSS. The next generation of GNSS will make dual frequency signals available to civil users enabling virtual elimination of residual errors due to the ionosphere and increased navigation accuracy. GNSS

ambiguity resolution used in attitude determination and many terrestrial applications can benefit from multiple frequency receivers [Teunissen *et al* 2002]. Therefore, the second hardware goal was to develop a low-cost receiver architecture capable of processing multiple frequency bands.

The combination of future GPS and Galileo constellations will make over 50 GNSS signals available to the space user. Currently SGR receivers have a maximum capacity of 24 receiving channels. A receiver with greater channel capacity and capability to process a range of GNSS signals would significantly benefit a number of space applications. GNSS reflectometry requires reflected signals from more than one satellite to determine wind direction [Komjathy *et al* 2001] and therefore benefits from more satellites in the sky. Also, more receiver tracking channels enables greater ocean coverage and may allow receivers to perform real-time formations of the delay-Doppler map, a valuable tool in GNSS reflectometry. The reliability of GNSS attitude determination could also be greatly increased through greater receiver channel capacity, devoting extra channels to each antenna (currently limited to 6 channels per antenna). Hence, the third hardware goal of this research was to provide the ability for the receivers to increase the number of tracking channels available to the user. Preferably this should be a flexible choice depending on the application.

Both the modernised GPS and Galileo systems will provide pilot tones on some of their signals. The pilot tones permit long integration times enabling acquisition and tracking of very weak GNSS signals. This is particularly useful for GEO receivers where navigational positioning is only made possible by receiving the very weak signals from GNSS satellite antenna side-lobes [Ebinuma *et al* 2004]. Therefore, an advanced receiver architecture capable of receiving modernised GPS and Galileo signals may benefit GEO receivers greatly and provide robust PVT information for GEO users. Also, GEO GNSS receivers are currently very expensive and hence users would benefit from low-cost receiver architecture suitable for the high-radiation environments experienced in HEO and GEO.

The above examples illustrate the need for new advanced GNSS receiver architecture for both commercial and scientific space applications. To summarise, the areas of

space receiver architecture to which this research project was intended to contribute to were as follows.

- Removing the dependency of the SSTL SGR range on an aging and potentially obsolete chipset.
- Low-cost receiver architecture capable of processing multiple frequency bands.
- Receiver architecture with greater and more flexible channel capacity.
- Receiver architecture capable of receiving GPS modernised and Galileo signals.
- Low-cost receiver architecture suitable for severe radiation environments.

Although multi-faceted, these advances in receiver technology generally embody the goals SSTL desires from this research. However, the design of receiver architecture for the next generation of GNSS results in a significant number of challenges both theoretical and practical from which academic value can be derived.

The new signals include a host of new complex modulation, multiplexing and coding schemes designed to cover higher bandwidths and deliver higher precision than ever transmitted before see [ESA and GJU 2006] and [GPS SIS 2007]. New approaches to receiver design and operation are required in order to take full advantage of the proposed signal specifications. Research broad enough to encompass the entire impact of the new GNSS is beyond the scope of this research project. Hence, a number of key areas of investigation were identified, which were of specific interest to SSTL and SSC. From this the academic goals of this research were formed and can be summarised as follows.

- Search, acquisition and tracking of Binary Offset Carrier (BOC) modulated signals – providing a comparison of the proposed receiver techniques, identifying flaws and determining where improvements can be made.
- The effect of complex multiplexing schemes on transmitter and receiver architectures and operation – analysing how these multiplexing schemes can be implemented and what approaches can be adopted in the receiver.

- Modulation and high bandwidth signals – evaluating the potential benefits and problems associated with BOC modulated and high-bandwidth signals.

3 Signal characteristics

This chapter details the signal structure of existing and future signals to be transmitted in the L-band GNSS frequency allocations. It is important to fully understand all possible future GNSS signal structures in order to evaluate their impact on GNSS receivers and formulate receiver solutions. Firstly, a review of the current or heritage GPS signal structure is given with signal representations, modulation and coding techniques. Secondly, the proposed changes to the GPS signal structure by the modernisation programme are detailed. Finally, the current Galileo signal structure, its specifications and properties are described in detail.

3.1 Heritage GPS signal characteristics

GPS is a spread spectrum system, where the spread signal occupies a bandwidth, much greater than the rate of the data being transmitted [Sklar 1988]. This redundancy of bandwidth serves to suppress detrimental effects of interfering signals and reduces the peak transmitted signal power levels to effectively hide the signal in background noise. The spreading technique denoted, Direct Sequence-Spread Spectrum (DS-SS), refers to technique where a carrier wave is modulated by a data signal overlaid with a high frequency Pseudo-Random Noise (PRN) spreading signal.

A conceptual diagram of a spread spectrum system is shown in Figure 3-1, the modulation onto the carrier is omitted for simplicity. The narrow bandwidth, B_d of the data signal $d(t)$ is spread by a PRN code spreading signal, $a(t)$ of significantly higher bandwidth, B_S . The transmitted signal then passes through a channel, which applies additive noise, $n(t)$ and interfering signals, $i(t)$. A synchronised replica spreading code signal multiplied onto the received signal will then result in recovery of the desired signal with some error from thermal noise (spectral density N_0) and interference.

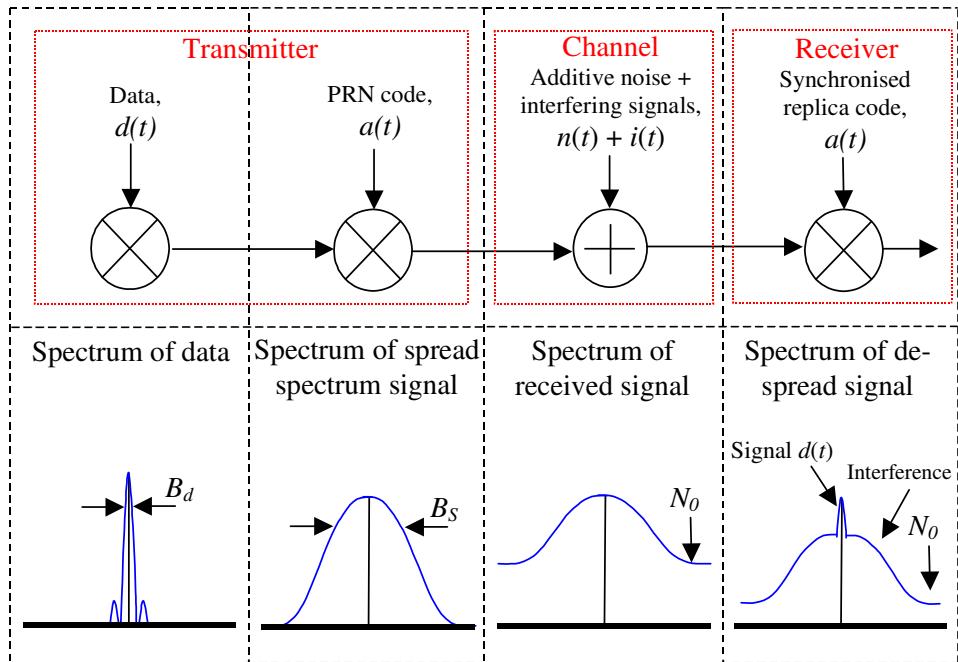


Figure 3-1, Simplified conceptual spread spectrum system

The innovation of the GPS is to use the PRN code sequence as a ranging signal. In combination with its associated data signal this allows the path difference from transmitter to receiver to be recovered. The GPS satellite signals share the same carrier frequency and are separable in a receiver only because each respective transmission employs a unique PRN spreading code. Each effective bit of the PRN code sequence is called a ‘chip’. Despite the fact that GPS is a code modulation of a continuous wave (CW) carrier, the navigational or ranging signal is effectively a sequence of periodic pulses, with a periodicity equal to the code length and pulse width of one chip. The range to each differently located GPS satellite is measured by the timing of these pulses and comparing the relative time delay of the pulses enables three-dimensional navigation.

Heritage GPS uses Binary Phase Shift Keyed (BPSK) modulation [GPS ICD 2007], where ideally the carrier phase changes instantaneously by 180° , depending on the data modulated spreading sequence. A PSK modulated signal can be written as

$$S_{PSK}(t) = \sqrt{2P} \times a(t) \times \cos(\omega t) \times d(t)$$

3-1

where $d(t), a(t) \in (-1, +1)$.

P is the signal power, $d(t)$ is the bi-phase data signal, $a(t)$ is the bi-phase PRN code spreading signal and ω is the carrier frequency. The designation BPSK-R(f_c) has been adopted to define this type of modulation, where f_c is the chipping rate and is an integer multiple of 1.023MHz.

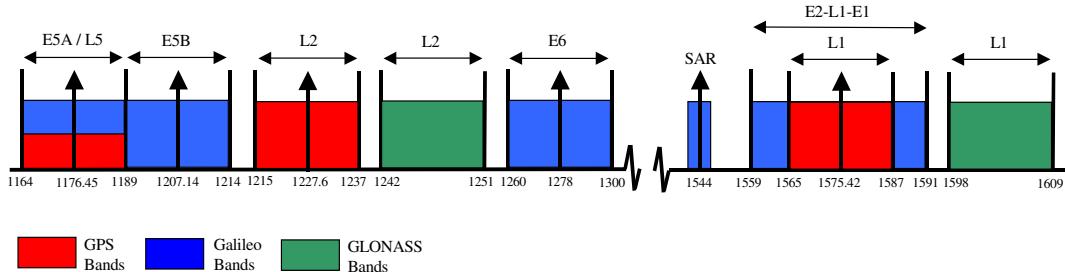


Figure 3-2, L-Band GNSS frequency allocations

Figure 3-2 shows the L-band frequency allocations for current and future GNSS systems. Currently, GPS consists of between 24 and 32 satellites broadcasting three navigational signals in the L-band; one signal available for civil use transmitted on the L1 carrier frequency and two military signals transmitted on the L1 and L2 carriers. The Heritage GPS signal structure is depicted in Figure 3-3. All the GPS signals are derived from the fundamental GPS frequency of 10.23MHz.

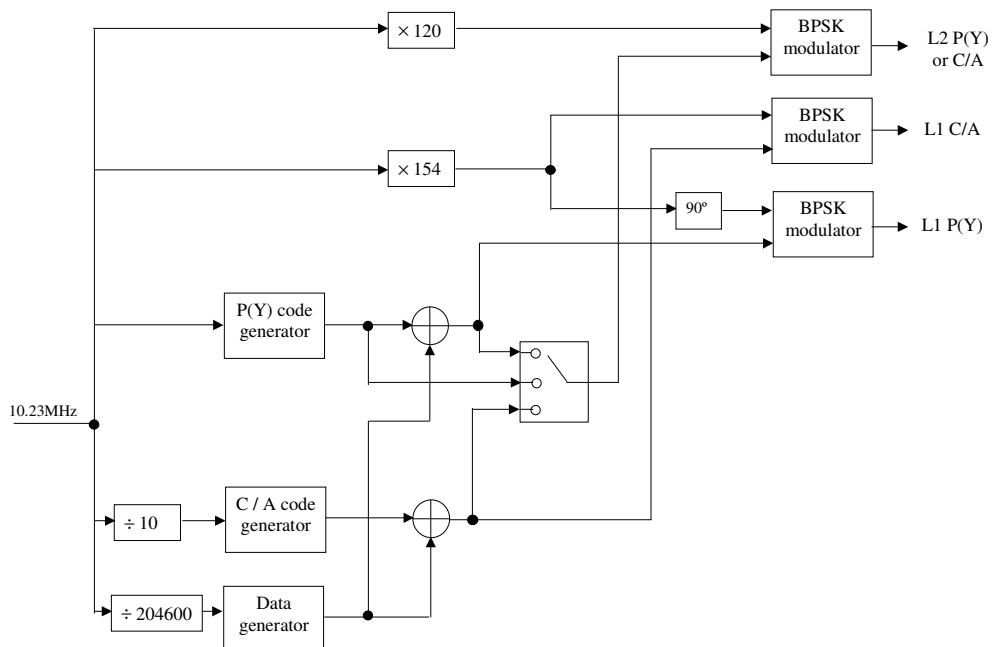


Figure 3-3, Heritage GPS signal generation structure [Kaplan and Hegarty 2006]

GPS signals on L1 retain orthogonality because they are broadcast in phase quadrature, which can be represented as follows.

$$S_{L1}(t) = \sqrt{2P_C}d_{CA}(t)a_{CAi}(t)\cos(\omega_{L1}t) + \sqrt{2P_P}d_P(t)a_{Pi}(t)\sin(\omega_{L1}t) \quad 3-2$$

$a_{CAi}(t)$ is denoted the Coarse Acquisition (C/A) code, which is a 1023 chip long PRN sequence, unique to the transmitting satellite i (1 to 32), from the Gold code family [Gold 1967]. Each bit or ‘chip’ of the C/A code, T_C is $(1/1,023)$ μ s long and therefore is said to have a ‘chipping rate’ of 1.023 Mcps (Mega chips per second). The entire C/A code sequence repeats every 1 ms. $a_{Pi}(t)$ is named the precision code, which is a PRN sequence, unique to the satellite i , with a chipping rate of 10.23 Mcps and repeats once a week. This code is known as the P(Y) code because if desired, the satellites have the ability to switch transmission to modulate the carrier with the encrypted Y code, which is only available to U.S. government users.

$d_{CA}(t)$, is the bi-phase navigational data signal associated with the civil C/A code and is transmitted at a rate of 50Hz. $d_P(t)$ is the navigational data associated with the military P code signal. The navigational data contains information necessary for the receiver to compute position, velocity and time solutions for each satellite. ω_{L1} is the L1 carrier frequency, P_C and P_P are the C/A and P(Y) signal powers, respectively.

The relative power of the currently transmitted C/A code is 3dB greater than that of the P(Y) code and hence, $P_P = \frac{P_C}{2}$.

One chip of the GPS C/A code propagating at the speed of light, c has a length of 293 m ($T_C \times c$), although actual discrimination generally achieves accuracies that are a very small fraction of this. The repeat interval of 1 ms implies a range ambiguity of around 300 km. However, transitions of navigational data potentially occur every 20 ms, which expands the ambiguity to around 6000 km. This range ambiguity is resolvable by examination of the data stream $d(t)$. The P(Y) code chipping rate of 10.23 Mcps results in an equivalent resolution of 29 m. Again, actual discrimination

is some small fraction of the resolution. Currently, the majority of GPS satellites transmit only the P(Y) code signal in the GPS L2 band, which can be represented as follows.

$$S_{L2}(t) = \sqrt{2P_p} d_p(t) a_{Pi}(t) \cos(\omega_{L2} t) \quad 3-3$$

ω_{L2} is the L2 carrier frequency.

The GPS C/A code is generated using two 10 bit linear feedback shift registers (LFSR), G1 and G2, as shown in Figure 3-4. Both registers are initialised with all bits set to a logical ‘one’ state. The feedback taps of the registers are commonly described in polynomial form as follows [Sklar 1988].

$$G1 = 1 + X^3 + X^{10} \quad 3-4$$

$$G2 = 1 + X^2 + X^3 + X^8 + X^9 + X^{10}$$

X^i represents the i th bit of the LFSR. 37 PRN codes are generated by combining the output of the G1 register with a unique selection of two bits from the G2 register.

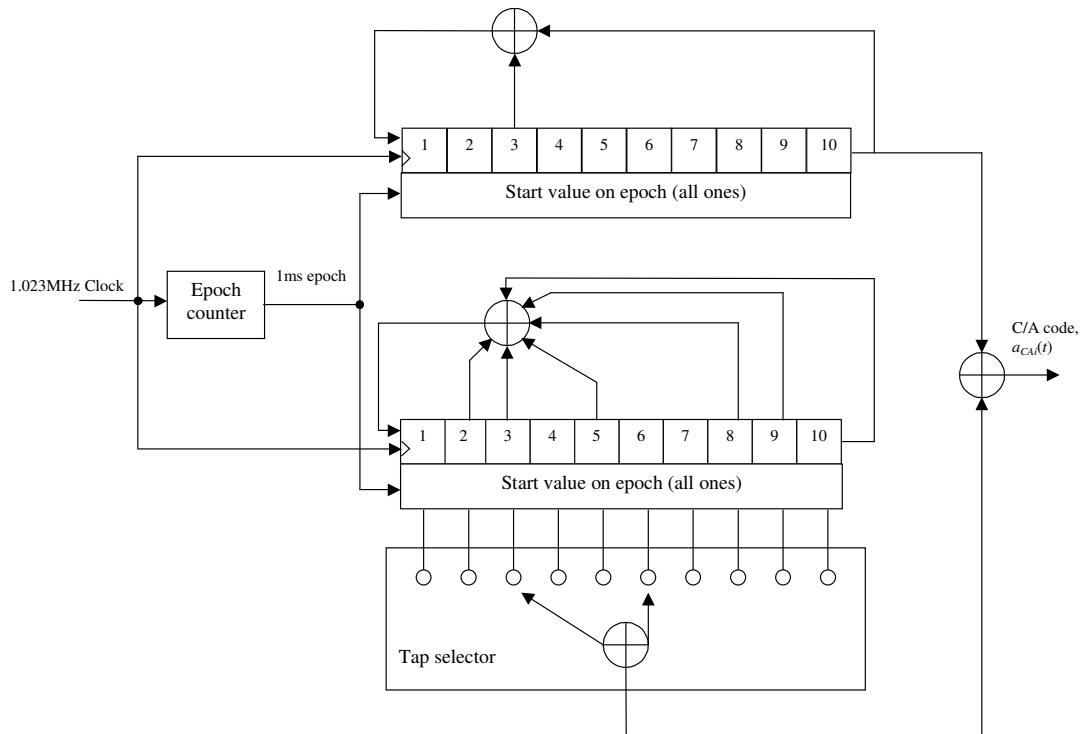


Figure 3-4, C/A code generator

The resulting PRN codes are maximal length sequences with $N = 2^n - 1$ chips, where n is the length of the LFSR. The periodic autocorrelation function for a PRN sequence $a(t)$ of length n chips, with a chip period T_C can be written as follows.

$$\Lambda(\tau) = \frac{1}{NT_C} \int_0^{NT_C} a(t)a(t+\tau)dt \quad 3-5$$

The autocorrelation envelope (Figure 3-5) can be approximated by a triangle function, the peak of which (amplitude A) corresponds to the perfect alignment (correlation) between the received code and the locally generated replica. Outside the correlation interval the ideal cross-correlation function is $-A/N$ due to the avoidance of the all-zero (stable) state in the generation of Gold codes.

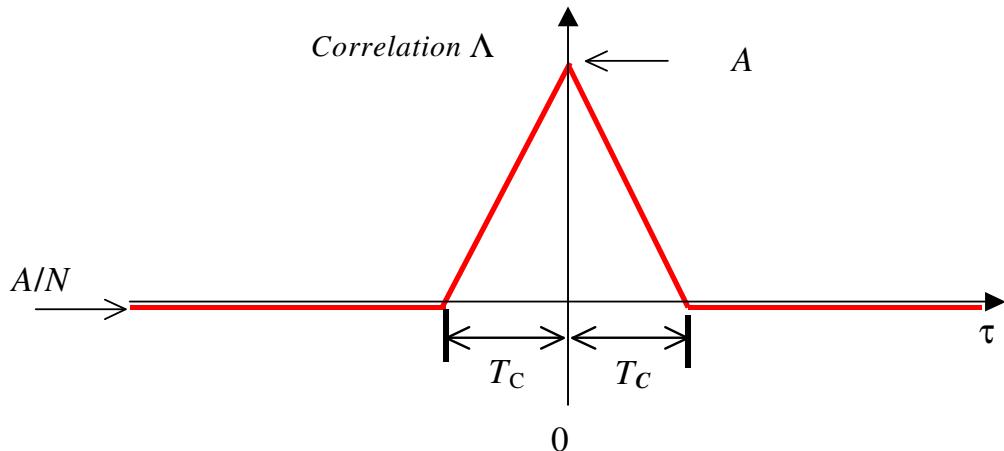


Figure 3-5, Ideal autocorrelation of a PRN sequence

In practice the sequences identified by Gold exhibit a three-valued cross-correlation function with values $\left\{ \frac{-1}{2^{n-1}}, \frac{-t(n)}{2^{n-1}}, \frac{t(n)-2}{2^{n-1}} \right\}$, where

$$t(n) = \begin{cases} 2^{(n+1)/2} + 1 & (\text{odd } n) \\ 2^{(n+2)/2} + 1 & (\text{even } n) \end{cases} \quad 3-6$$

Therefore, Gold sequences employed for GPS C/A code have cross correlation values of $\left\{ \frac{-1}{1023}, \frac{-65}{1023}, \frac{63}{1023} \right\}$. The autocorrelation of the GPS C/A code (PRN1) is shown in Figure 3-6.

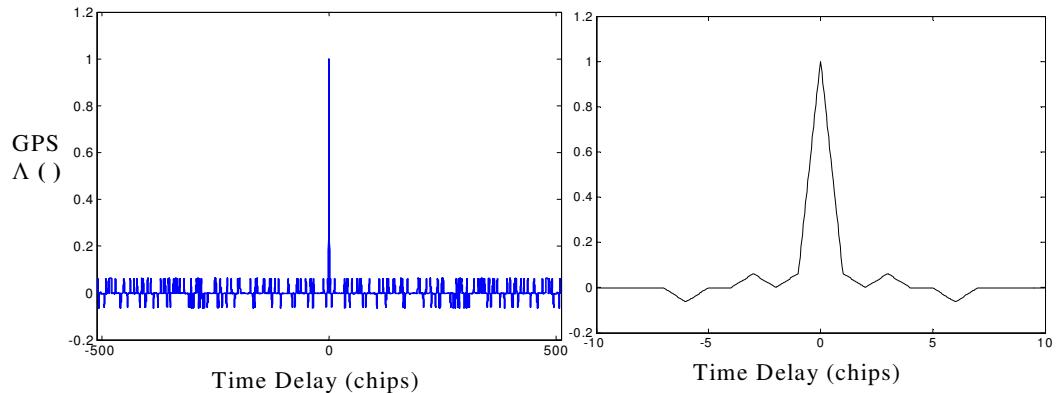


Figure 3-6, Normalised autocorrelation of GPS C/A code

A PRN code sequence can be viewed as a periodic sequence of pseudo-randomly repeated rectangular pulses. Therefore, the two-sided power spectral density of a sequence with chip period T_C and pulse amplitude A , can be written as

$$S_{PRN}(\omega) = A^2 T_C \text{sinc}^2\left(\frac{\omega T_C}{2}\right) \quad 3-7$$

$$\text{where, } \text{sinc}(x) = \frac{\sin(x)}{x}$$

The power spectral densities (PSD) of the current GPS signals are shown in Figure 3-7, assuming no filtering to the signals and 1W signal power. The main lobe of the C/A code signal is seen to spread ± 1.023 MHz around the L1 carrier. The higher chipping rate of the P(Y) code, ten times the C/A code rate, causes the spectral energy of the main lobe to be spread over ± 10.23 MHz around the carrier.

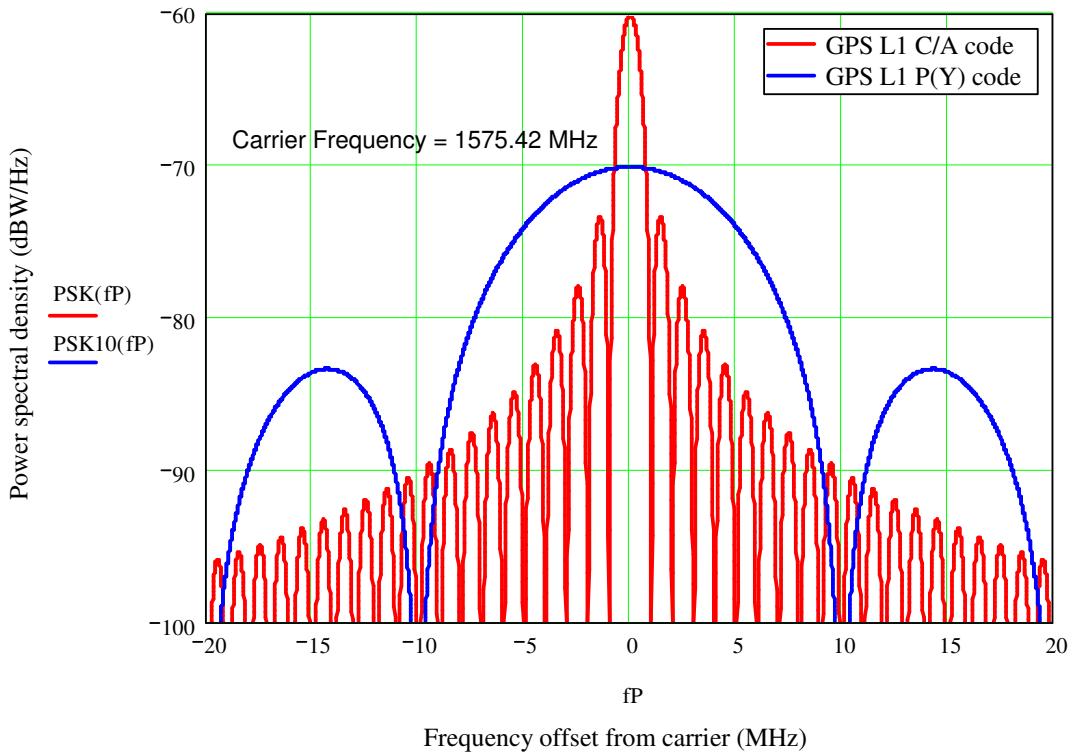


Figure 3-7, Power spectral density of current GPS L1 signals: (unfiltered, 1W signal power)

The Radio Frequency (RF) link budget for GPS signals is shown in Table 3-1. The free space propagation loss, L_{PR} is calculated as follows.

$$L_{PR} = \left(\frac{\lambda}{4\pi r} \right)^2 \quad 3-8$$

λ is the transmitted carrier wavelength and r is the distance to the satellite ($r = 25236$ km at 5° elevation).

Table 3-1, Link budget for GPS satellites

	L1 C/A code	L1 P(Y) code	L2 P(Y) code
Satellite TX power, [P_T] ¹	13.4 dBW	10.4 dBW	8.2 dBW
TX Antenna gain, [G_{TX}] (max pointing error 14.3°)	13.4 dB	13.4 dB	11.5 dB
Required SV EIRP =[P_T] + [G_{TX}]	26.8 dBW	23.8 dBW	19.7 dBW
Atmospheric losses, [L_A]	0.5 dB	0.5 dB	0.5 dB
Propagation loss, [L_{PR}] (R = 25236km)	184.4 dB	184.4 dB	182.3 dB
Receiving antenna gain, [G_{RX}]	0 dB	0 dB	0 dB
Minimum received power =[P_T] + [G_{TX}] - [L_A] - [L_{PO}] - [L_{PR}] + [G_{RX}]	-158.1 dBW	-161.1 dBW	-163.1 dBW

Generally the received power levels of the GPS satellites are up to 5dB greater than the specified minimum power levels [Kaplan and Hegarty 2006].

3.2 GPS modernised signal characteristics

The completion of GPS modernisation under the current plans [GPS ICD 2007] will result in four additional navigational signals transmitted in the L-band; one military signal broadcast on the L1 carrier frequency, L1 M, one military and one civil signal on the L2 frequency, L2 M and L2 C respectively, and an additional civil signal on the L5 carrier (see Figure 3-2). The GPS block IIR satellites will transmit the new L1 and L2 signals while the subsequent block IIF satellites will transmit the new L5 signal. Discussions between the US and ESA are still on-going as to whether to accept a proposal to implement a common civil signal in the L –band (L1 C). Table 3-2 shows the centre frequencies, currently agreed modulation schemes, data rates and types of data of current and future GPS signals.

¹ The use of square brackets [] denotes a dB quantity

Table 3-2, Future GPS signals [GPS ICD 2007]

Signal	Centre frequency (MHz)	Modulation scheme	Main lobe bandwidth (MHz) ²	Types of data	Data rate (sps)
L1 C/A	1575.42	BPSK-R(1)	2.046	Civil	50
L1 C	1575.42	BOC(1,1) or MBOC(6,1,1/11)	4.092 and 14.332	Civil	Unknown
L1 P(Y)	1575.42	BPSK-R(10)	20.46	Military	50
L1 M	1575.42	BOC (10, 5)	30.69	Military	Unknown
L2 C	1227.6	BPSK-R(1)	2.046	Civil	50
L2 P(Y)	1227.6	BPSK-R(10)	20.46	Military	50
L2 M	1227.6	BOC (10, 5)	30.69	Military	Unknown
L5 I	1176.45	BPSK-R(10)	20.46	Civil	100
L5 Q	1176.45	BPSK-R(10)	20.46	Civil	Data-less

A 12 month study by the GPS Joint Program Office (JPO) [Betz 1999] resulted in the decision to use Binary Offset Carrier (BOC) modulation for the new military signals on L1 and L2. This modulation type will also be implemented for Galileo signals in various forms. BOC modulation is a rectangular sub-carrier modulation (sine or cosine) of the PRN spreading code and is denoted $\text{BOC}(f_s, f_c)$, where, f_s is the sub-carrier frequency, f_c is the PRN code chipping rate and both are multiples of 1.023×10^6 . The subcarrier frequency is chosen such that it has an integer number of half periods, T_s (sub-chips) within a chip of the spreading sequence. A number of different BOC modulations are depicted in Figure 3-8. The normalised PSD of a sine phased BOC signal can be written as [Betz 2001]

$$S_{\text{BOC}_s}(f) = f_c \begin{cases} \frac{\sin\left(\frac{\pi f}{2f_s}\right) \sin\left(\frac{\pi f}{f_c}\right)}{\pi f \cos\left(\frac{\pi f}{2f_s}\right)}^2 & \text{for } 2f_s/f_c \text{ even} \\ \frac{\sin\left(\frac{\pi f}{2f_s}\right) \cos\left(\frac{\pi f}{f_c}\right)}{\pi f \cos\left(\frac{\pi f}{2f_s}\right)}^2 & \text{for } 2f_s/f_c \text{ odd} \end{cases} \quad 3-9$$

² For BOC modulations the main lobe bandwidth is defined as the bandwidth encapsulating the largest two spectral lobes.

If the BOC subcarrier is cosine phased with respect to the code sequence the normalised PSD can be written as

$$S_{BOC_c}(f) = f_c \begin{cases} \frac{2 \sin^2\left(\frac{\pi f}{4f_s}\right) \sin\left(\frac{\pi f}{f_c}\right)}{\pi f \cos\left(\frac{\pi f}{2f_s}\right)} & \text{for } 2f_s/f_c \text{ even} \\ \frac{2 \sin^2\left(\frac{\pi f}{4f_s}\right) \cos\left(\frac{\pi f}{f_c}\right)}{\pi f \cos\left(\frac{\pi f}{2f_s}\right)} & \text{for } 2f_s/f_c \text{ odd} \end{cases} \quad 3-10$$

The most desirable effect of BOC modulation is that it produces replicas of the spread signal pushed away from the centre frequency at $\pm f_s$. Hence, the spectral energy is shifted away from the carrier frequency, potentially allowing localised jamming of the civil signal without significantly affecting the integrity of the military signal.

Frequency reuse is the primary justification for using BOC modulation for GNSS systems, reducing or eliminating the spectral overlap of the signals within a given bandwidth. However, BOC modulation also claims potential advantages in multipath mitigation and code tracking accuracy. These issues are addressed in detail in Chapter 4.

The GPS M code signals are to be transmitted using a BOC(10, 5) modulation. Therefore, the main lobes of the signal will be spread over 10.23MHz and the lobes will be shifted $\pm 10.23\text{MHz}$ away from the carrier. The modernised signals for L1 are shown in Figure 3-9 with the M code signal.

Recently a joint GPS-Galileo working group [Hein *et al* 2006] have proposed a common multiplexed BOC (MBOC) structure for future L1 civil signals. Studies on this signal were beyond the scope of this project due to its late introduction. Therefore, MBOC is considered in the Chapter 11 of this report, describing extensions of this work.

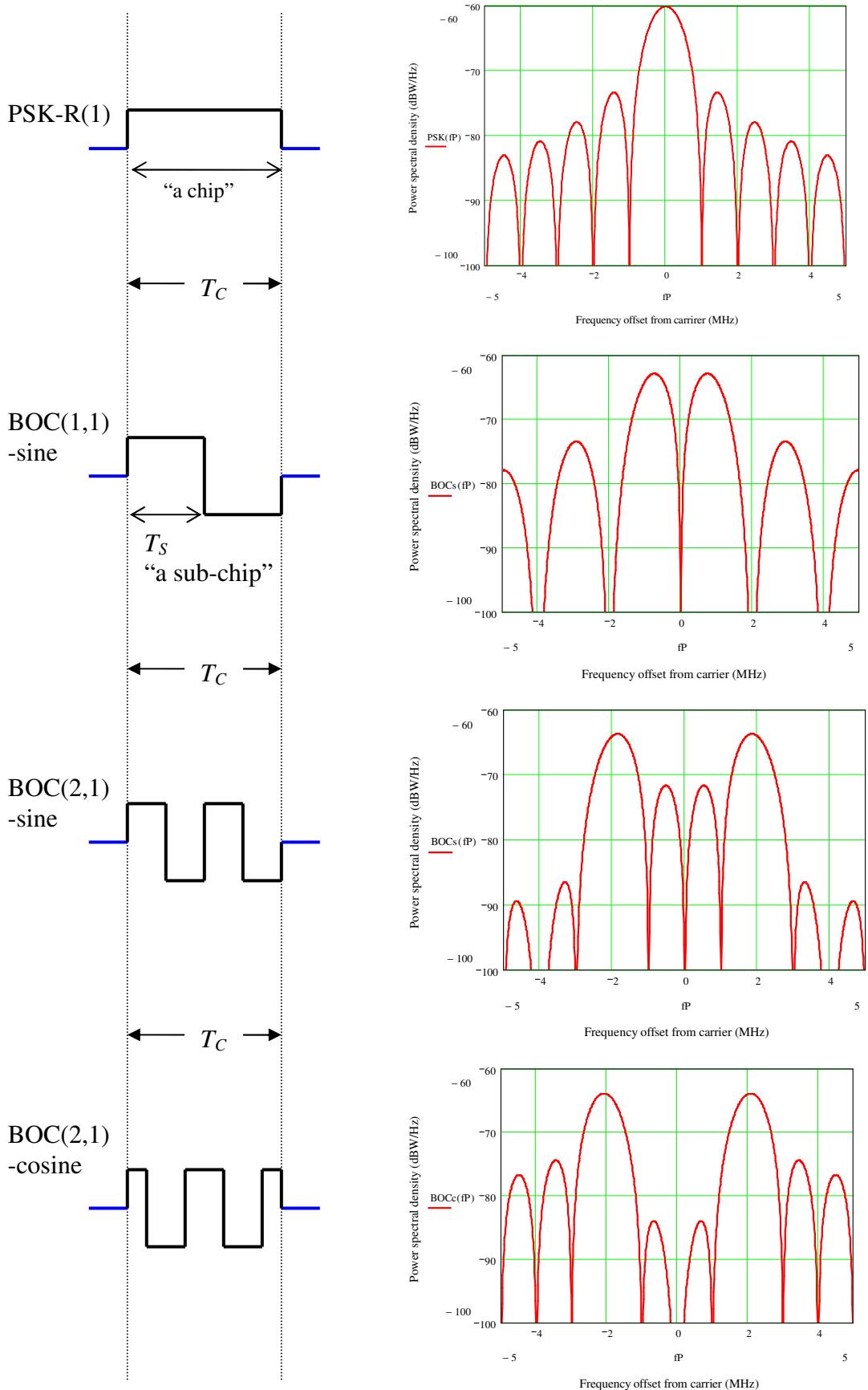


Figure 3-8, Spreading waveforms and PSD of BPSK(1), BOC(1,1)-sine, BOC(2,1)-sine and BOC(2,1)-cosine modulations

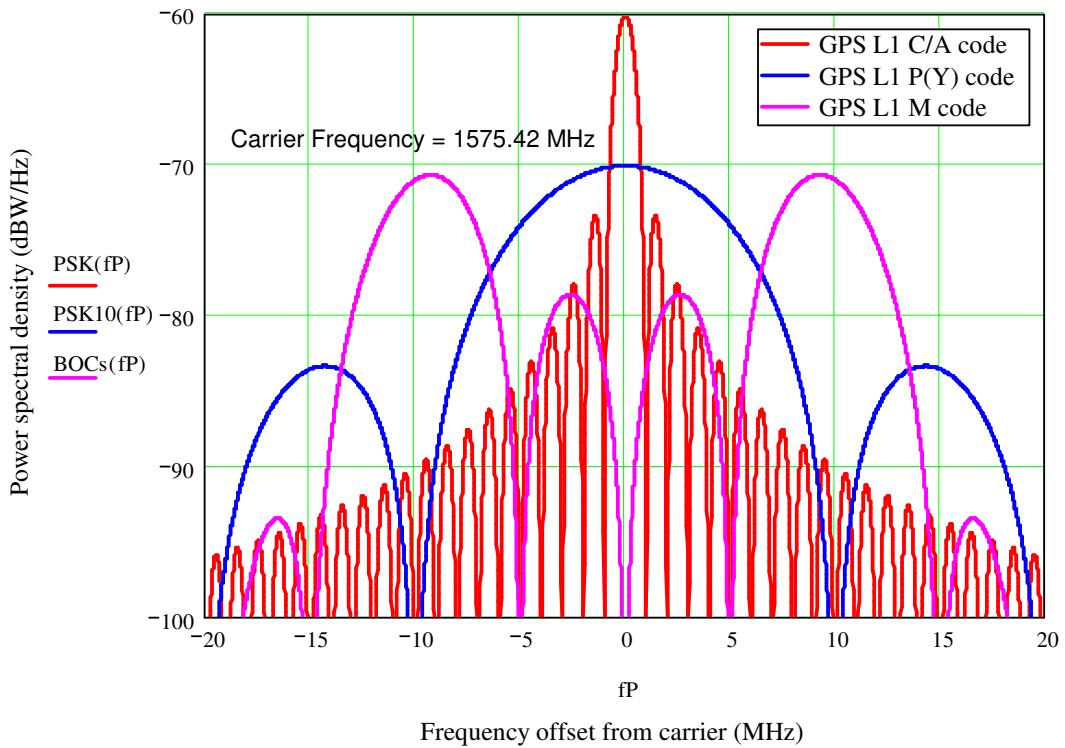


Figure 3-9, Power spectral density of future L1 GPS signals (unfiltered, 1W signal power)

The spectral shape of the current baseline for the modernised GPS L2 band is equivalent to that shown in Figure 3-9, with a centre frequency of 1227.6 MHz. The new civil signal on the L2 carrier, akin to the C/A code signal, uses BPSK-R(1) modulation. However, there are subtleties in the generation of the PRN codes for which the L2C signal yields unique distinction.

The L2C signal combines two PRN codes of different lengths, the moderate length (20msec) CM code and the long (1.5sec) CL code. The L2(C) signal generation scheme is shown in Figure 3-10. Each code is generated at a rate of 511.5kchip/s. The CM is modulated by data at 50 sps (symbols per second), which is half-rate Forward Error Correction (FEC) coded. The CL code has no data modulation. The CM and CL code are then multiplexed together on a chip by chip basis to provide a combined chip rate of 1.023 Mcps.

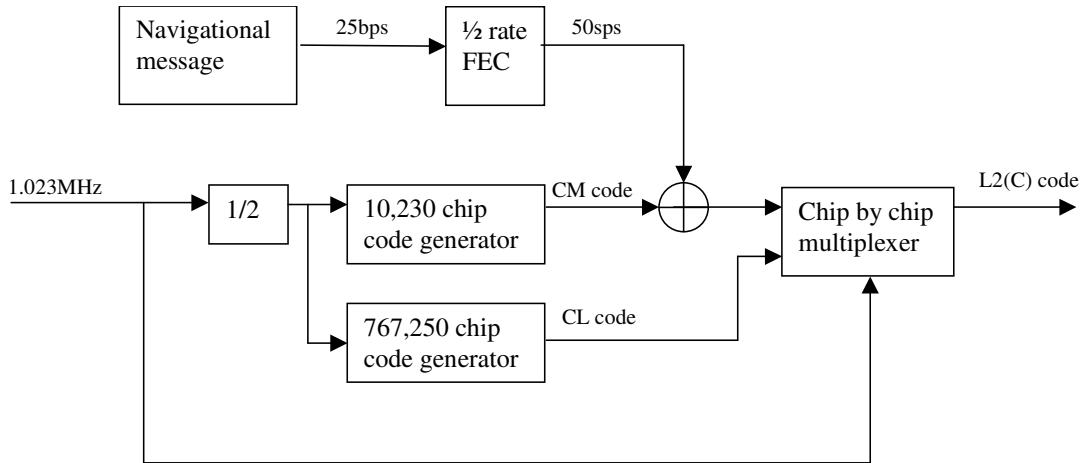


Figure 3-10, L2(C) code signal generation

A code or channel with no data modulation is known as a ‘pilot’, this is an important design feature and is incorporated many times into the modernised GPS and Galileo signal structures. A pilot code or channel allows GNSS receivers to use true Phase Locked Loop (PLL) discriminators, providing more accurate tracking than the Costas loop discriminators, which are commonly used in existing GNSS receivers. The pilot tones also allow longer integration periods to be easily implemented in the receiver for weak-signal acquisition and tracking.

Combining three signals onto a single carrier frequency requires an additional multiplexing or modulation scheme and can impact on signal attributes such as power and constant envelope properties. The phase II Replacement Modernised (IIR-M) GPS satellites will use a modulation named ‘interplex’ or ‘modified hexaphase’ to combine the three signals onto both the L1 and L2 carrier waves [GPS ICD 2007]. In Section 7.1, we describe how this modulation can be produced in hardware and demonstrate an elegant modulation architecture. The impact of interplex modulation on receiver design is discussed in detail in Section 10.3. However, for completeness the current baseline for the future GPS L1 and L2 signals after interplexing can be written as follows [Dafesh *et al* 2000].

3-11

$$S_{FL1}(t) = \left[\sqrt{2P_I} d_p(t) a_{Pi}(t) \cos(m) - \sqrt{2P_Q} d_M(t) s(t) a_{Mi}(t) \sin(m) \right] \cos(\omega_{L1} t) + \left[\sqrt{2P_Q} d_{CA}(t) a_{CAi}(t) \cos(m) + \sqrt{2P_I} s(t) a_{CAi}(t) a_{Pi}(t) a_{Mi}(t) \sin(m) \right] \sin(\omega_{L1} t)$$

3-12

$$S_{FL2}(t) = \left[\sqrt{2P_I} d_P(t) a_{Pi}(t) \cos(m) - \sqrt{2P_Q} d_M(t) s(t) a_{Mi}(t) \sin(m) \right] \cos(\omega_{L2} t) \\ + \left[\sqrt{2P_Q} d_C(t) a_{Ci}(t) \cos(m) + \sqrt{2P_I} s(t) a_{Ci}(t) a_{Pi}(t) a_{Mi}(t) \sin(m) \right] \sin(\omega_{L2} t)$$

P_I and P_Q are the total powers in the in-phase and quadrature channels before interplex modulation, which are set by the choice of modulation index m , $s(t)$ is the square wave sub-carrier for BOC modulation with a frequency of 10.23MHz, $a_{Ci}(t)$ is the combination of the L2 CM and CL codes, and $a_{Mi}(t)$ is the classified PRN sequence for M code signal. $d_M(t)$, is the bi-phase navigational data signal associated with the military M code signal.

The new GPS L5 signal potentially offers the most significant benefit to civil GPS users, primarily through the delivery of a dual frequency civil system with high precision measurements.

The GPS L5 signal is a complex signal consisting of an in-phase carrier modulated by a tiered code spreading sequence (see Appendix A) with navigational data and a data-less pilot channel in phase quadrature modulated only by a tiered code spreading sequence. The GPS L5 signal can be represented as follows

$$S_{L5}(t) = \sqrt{2P_{L5}} d_{L5}(t) a_{I5i}(t) \cos(\omega_{L5} t) + \sqrt{2P_{L5}} a_{Q5i}(t) \sin(\omega_{L5} t) \quad 3-13$$

Where, ω_{L5} is the L5 carrier frequency, P_{L5} is the L5 signal power, a_{I5i} and a_{Q5i} are the tiered PRN code sequences for the in-phase and quadrature channels respectively. $d_{L5}(t)$, is the bi-phase navigational data signal associated with the civil L5 signal.

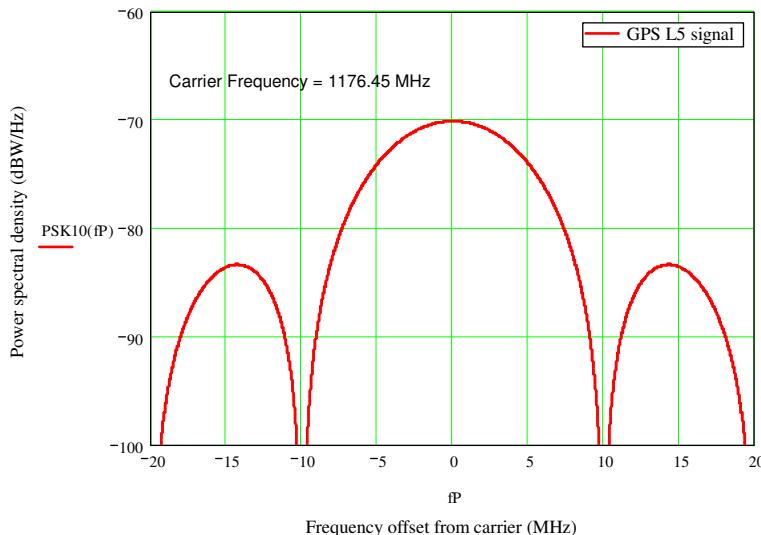


Figure 3-11, Power spectral density of future L5 GPS signal (unfiltered, 1W signal power)

3.3 Galileo signal characteristics

Under the current plans [ESA and GJU 2006] the new European Galileo GNSS will provide a wide range of radionavigation signals to both civil and regulated users. The current baseline of Galileo signals is believed to be as shown in Table 3-3. Galileo will introduce six data-modulated signals and four data-less signals into the L-band spectrum, which are to provide the core Galileo services as follows [Dutton *et al* 2002].

- Open Service (OS) – This service which provides position, velocity and time (PVT) information, will be available on two frequencies, unencrypted and free of charge.
- Commercial Service (CS) – This service will be a controlled access service for professional applications with service guarantees. CS provides two signals with encrypted data messages at different frequencies to OS broadcasting.
- Safety of Life (SoL) – This service is targeted at users where navigation safety is critical (maritime, aviation, trains) and high level global performance is required. SoL signals will be broadcast on three carrier frequencies, one of which is separated in frequency from all other services.
- Public Regulated Service (PRS) – This service is designed to provide a high level of data protection in so-called ‘times of extreme tension’. PRS is to be

broadcast on two frequencies and will be heavily encrypted. Access to the PRS will be controlled through EU member states.

Table 3-3, Galileo signals [ESA and GJU 2006]

Signal	Centre frequency (MHz)	Modulation scheme	Main lobe bandwidth (MHz)	Types of service	Data rate (sps)
E1 A	1575.42	BOC(15, 2.5)	35.805	PRS	
E1 B	1575.42	BOC(1,1) or MBOC(6,1,1/11)	4.092	OS, SoL, CS	250
E1 C	1575.42	BOC(1,1) or MBOC(6,1,1/11)	4.092	Data-less	
E5a I	1191.795	AltBOC(15, 10)	51.15	OS	50
E5a Q	1191.795	AltBOC(15, 10)	51.15	Data-less	
E5b I	1191.795	AltBOC(15, 10)	51.15	OS, SoL, CS	250
E5b Q	1191.795	AltBOC(15, 10)	51.15	Data-less	
E6 A	1278.75	BOC(10, 5)	30.69	PRS	
E6 B	1278.75	BPSK-R(5)	10.23	CS	1000
E6 C	1278.75	BPSK-R(5)	10.23	Data-less	

The Galileo codes are based on the tiered code concept, the primary and secondary codes length are shown in Table 3-4. The table also indicates whether or not the codes are based on LFSR polynomials or memory stored binary sequences.

Table 3-4, Galileo codes [ESA and GJU 2006]

Signal	Primary code length (chips)	Secondary code length (chips)	Code epoch (ms)	Generator Polynomial (octal)	
				1	2
E1 A	Unknown	Unknown	Unknown	Unknown	Unknown
E1 B	4092	1	4	Memory stored	Memory stored
E1 C	4092	25	100	Memory stored	Memory stored
E5a I	10230	20	20	40503	50661
E5a Q	10230	100	100	40503	50661
E5b I	10230	4	4	64021	51445
E5b Q	10230	100	100	64021	43143
E6 A	Unknown	Unknown	Unknown	Unknown	Unknown
E6 B	5115	1	1	Unknown	Unknown
E6 C	10230	50	100	Unknown	Unknown

Figure 3-12 and Figure 3-13 show the power spectral densities for the Galileo E1 and E6 bands respectively. Both bands have two data modulated signals and one data-less channel, which are to be combined through interplex modulation and can be represented as follows.

$$S_{E1}(t) = \left[\sqrt{2P_I} d_{E1B}(t) s_{E1B}(t) a_{E1Bi}(t) \cos(m) - \sqrt{2P_Q} s_{E1C}(t) a_{E1Ci}(t) \sin(m) \right] \cos(\omega_{L1} t) \quad 3-14$$

$$+ \left[\begin{aligned} & \sqrt{2P_Q} d_{E1A}(t) s_{E1A}(t) a_{E1Ai}(t) \cos(m) \\ & + \sqrt{2P_I} s_{E1A}(t) s_{E1B}(t) s_{E1C}(t) a_{E1Ai}(t) a_{E1Bi}(t) a_{E1Ci}(t) \sin(m) \end{aligned} \right] \sin(\omega_{L1} t)$$

$$S_{E6}(t) = \left[\sqrt{2P_I} d_{E6B}(t) a_{E6Bi}(t) \cos(m) - \sqrt{2P_Q} a_{E6Ci}(t) \sin(m) \right] \cos(\omega_{E6} t) \quad 3-15$$

$$+ \left[\begin{aligned} & \sqrt{2P_Q} d_{E6A}(t) s_{E6A}(t) a_{E6Ai}(t) \cos(m) \\ & + \sqrt{2P_I} s_{E6A}(t) a_{E6Ai}(t) a_{E6Bi}(t) a_{E6Ci}(t) \sin(m) \end{aligned} \right] \sin(\omega_{E6} t)$$

ω_{E6} is the E6 carrier frequency, $s_{IA}(t)$, $s_{IB}(t)$ and $s_{6A}(t)$ are square wave sub-carriers, $a_{E1Ai}(t)$, $a_{E1Bi}(t)$, $a_{E1Ci}(t)$, $a_{E6Ai}(t)$, $a_{E6Bi}(t)$ and $a_{E6Ci}(t)$ are the PRN sequences, including secondary codes for the E1 A, B and C signals and the E6 A, B and C

signals, respectively. $d_{E1B}(t)$, $d_{E1A}(t)$, $d_{E6B}(t)$ and $d_{E6A}(t)$ are bi-phase navigational data signals for the respective signals.

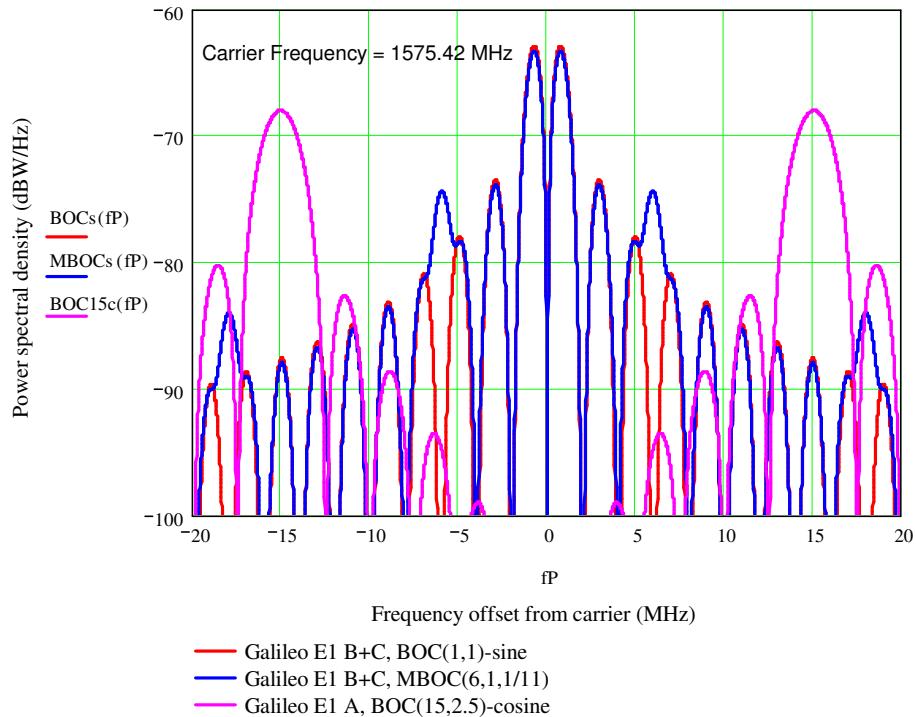


Figure 3-12, Power spectral density of the Galileo E1 signals (1W signal power)

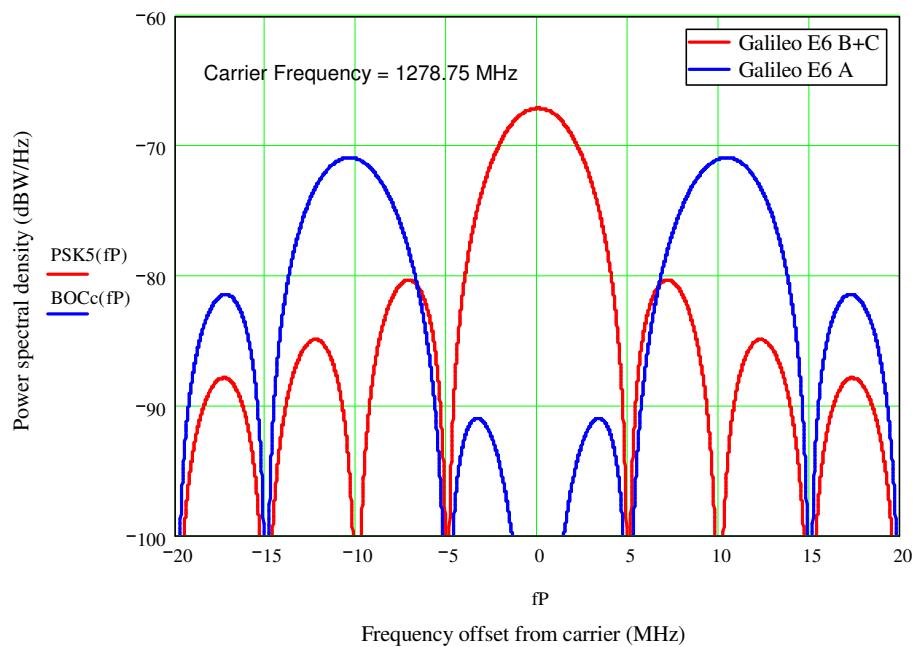


Figure 3-13, Power spectral density of the Galileo E6 signals (1W signal power)

The Galileo E5a and E5b bands will each transmit a data-modulated and a data-less channel. These four signals are combined onto a single centre frequency, this is accomplished through the use of Alternate BOC (AltBOC) modulation. This high-bandwidth complex signal offers unprecedented code tracking accuracy and multipath mitigation properties. This generation of this signal is detailed in Section 7.1, receiver design for AltBOC signal is covered in Section 6.3. The Galileo E5a and E5b bands can be represented as follows.

$$\begin{aligned}
 s_{E5}(t) = & \sqrt{2P_{E5}} \times [a_{E5al}(t) \times d_{E5a}(t) + a_{E5bl}(t) \times d_{E5b}(t)] \times s(t) \times \cos(\omega_{E5}t) \\
 & + \sqrt{2P_{E5}} \times [a_{E5al}(t) \times d_{E5a}(t) - a_{E5bl}(t) \times d_{E5b}(t)] \times \tilde{s}(t) \times \sin(\omega_{E5}t) \\
 & + \sqrt{2P_{E5}} \times [a_{E5aQ}(t) + a_{E5bQ}(t)] \times \tilde{s}(t) \times \cos(\omega_{E5}t) \\
 & - \sqrt{2P_{E5}} \times [a_{E5aQ}(t) - a_{E5bQ}(t)] \times s(t) \times \sin(\omega_{E5}t)
 \end{aligned} \quad 3-16$$

ω_{E5} is the E5 carrier frequency, $s(t)$, is a 15.345MHz sine square wave sub-carrier, $\tilde{s}(t)$ is a 15.345MHz cosine square wave sub-carrier, $a_{E5al}(t)$, $a_{E5aQ}(t)$, $a_{E5bl}(t)$, $a_{E5bQ}(t)$, are the tiered code spreading sequences for the E5 band. $d_{E5a}(t)$ and $d_{E5b}(t)$ are bi-phase navigational data signals for the respective signals. The power spectral density of the Galileo E5 band is shown in Figure 3-14 [Rebeyrol *et al* 2005].

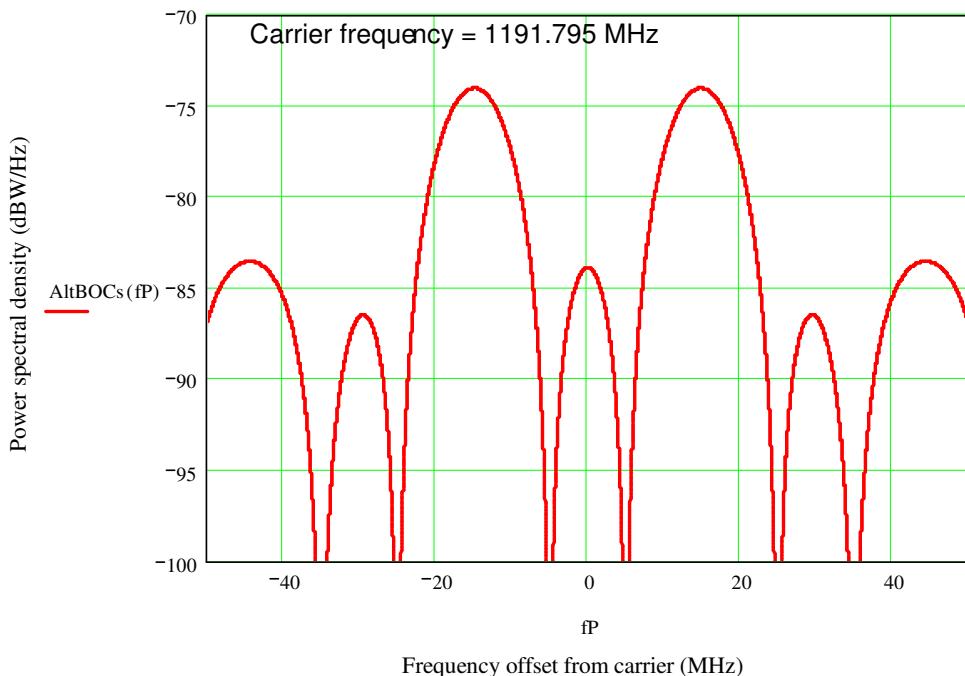


Figure 3-14, Power spectral density of the Galileo E5 band (1W signal power)

The predicted received power levels of the Galileo signals are shown in Table 3-5.

Table 3-5, Received power levels of Galileo signals [ESA and GJU 2006]

	E1B	E1C	E6B	E6C	E5a (I)	E5a (Q)	E5b (I)	E5b (Q)
Satellite TX power, [P_T]	15.66 dB		15.85 dB		15.24 dB			
TX Antenna gain, [G_{TX}] (max pointing error 14.3°)	13.4 dB		13.4 dB		13.4 dB			
Required SV EIRP =[P_T] + [G_{TX}]	29.06 dBW		29.25 dBW		28.64 dBW			
Atmospheric losses, [L_A]	0.5 dB		0.5 dB		0.5 dB			
Propagation loss, [L_{PR}] (R = 25236km)	185.56 dB		183.75 dB		183.14			
Receiving antenna gain, [G_{RX}]	0 dB		0 dB		0 dB			
Minimum received power =[P_T] + [G_{TX}] - [L_A] -[L_{PO}] - [L_{PR}] + [G_{RX}]	-157 dBW		-155 dBW		-155 dBW			

4 PSK and BOC signals

In this chapter, the advantages and disadvantages of BOC signals are discussed and comparison is made with PSK systems. Also, theoretical equations for timing jitter are given for both PSK and BOC systems, and are used in subsequent chapters to evaluate receiver performances. The effect of BOC modulation on the signal spectrum, receiver timing jitter and multipath performance are considered and compared to equivalent PSK modulations.

Binary Offset Carrier (BOC) modulation is ideally a square wave sub-carrier modulation of a PRN sequence. Its effect is that the signal is amplitude modulated, with its power spectrum shifted away from the carrier frequency in upper and lower sidebands with a null at the centre frequency. The null is the primary benefit of BOC modulation, allowing frequency re-use along with current PSK signals. In addition, BOC modulation claims greater resistance to short-range multipath and a small advantage in code tracking accuracy. However, these advantages come at a price, namely the difficulties in acquiring and tracking signals with a sub-carrier modulation.

4.1 Signal spectra and bandwidth

In order to perform a fair comparison between BOC and PSK systems it is necessary to identify a number of different definitions of bandwidth. The *Nyquist bandwidth* embodies the minimum spectral bandwidth into which a PSK transmission can be compressed. For PSK transmissions this bandwidth is identical to the chipping rate and so we define a *processing rate*, which for PSK transmissions is also equal to the chipping rate.

The effect of BOC modulation is the creation of upper and lower sidebands of the signal, which effectively doubles the Nyquist bandwidth to twice the chip rate. We define the processing rate for a BOC signal as the sub-chip rate which is the same as twice the sub-carrier frequency. Both the Nyquist bandwidth and processing rate are inherent to a given signal and are independent of the signal's spectral shape. The

front-end bandwidth of a GNSS receiver must be equal to or greater than both the Nyquist bandwidth and the processing rate. The different definitions of bandwidth are depicted in Figure 4-1. These notions of bandwidth are used in Section 4.4 and Section 4.5 of this chapter to provide a fair basis of comparison between PSK and BOC signals.

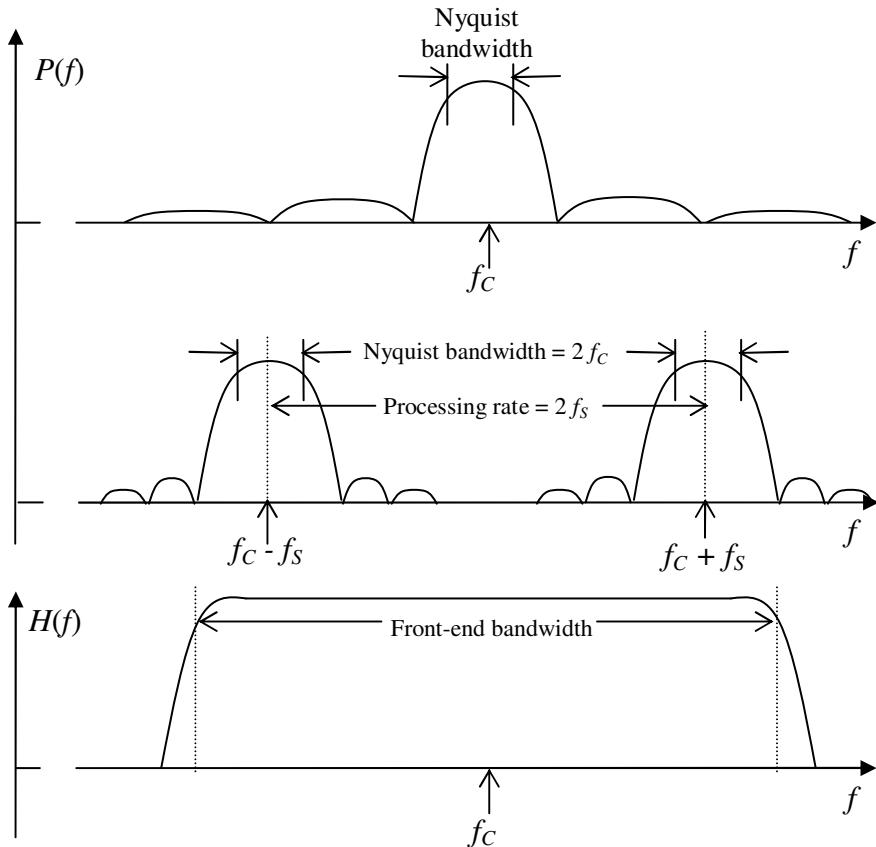


Figure 4-1, PSK and BOC bandwidth definitions

The phasing of the BOC sub-carrier to the code has an effect on the spectral shape of the signal. The most noticeable effect is on the secondary lobes of the BOC transmission. Cosine sub-carrier phasing has the effect of pushing more spectral energy into the secondary lobes further away from the centre frequency compared to sine sub-carrier phasing. The choice of sub-carrier phasing is dependent on number and location of the signals within a given bandwidth. BOC signals with high-rate sub-carriers are generally selected to have cosine phasing to reduce spectral overlap and hence interference with signals transmitted within the BOC null. For example, in the L1 band the Galileo BOC(15, 2.5) signal has cosine phasing to reduce the

interference with the GPS BOC(10, 5) M code signal. The effect of sub-carrier phasing on the signals spectral shape is shown in Figure 4-2 with a BOC(10, 5) modulation.

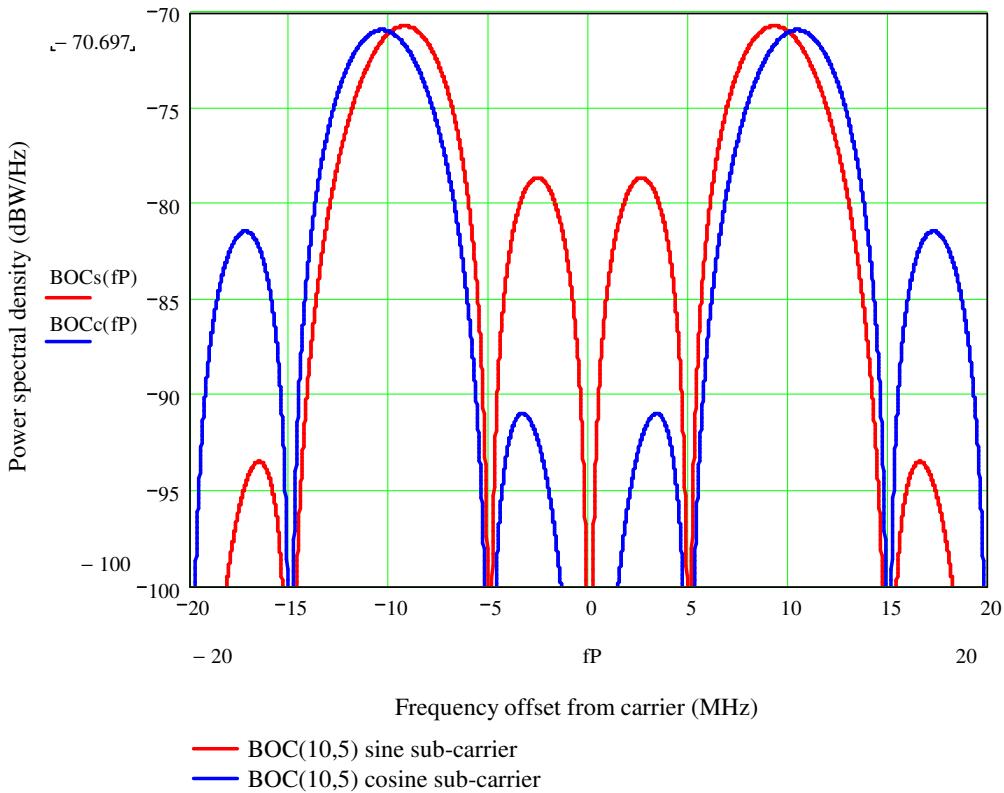


Figure 4-2, Power spectral density of a BOC(10, 5) signal with sine and cosine sub-carriers

A common measure of the amount of signal degradation incurred from interference between two signals in a receiver channel is given by their spectral separation coefficient. Envisioning the receiver as a matched filter process (see Figure 4-3), the spectral separation coefficient defines the signal degradation due to the interference on the desired ‘matched’ signal.

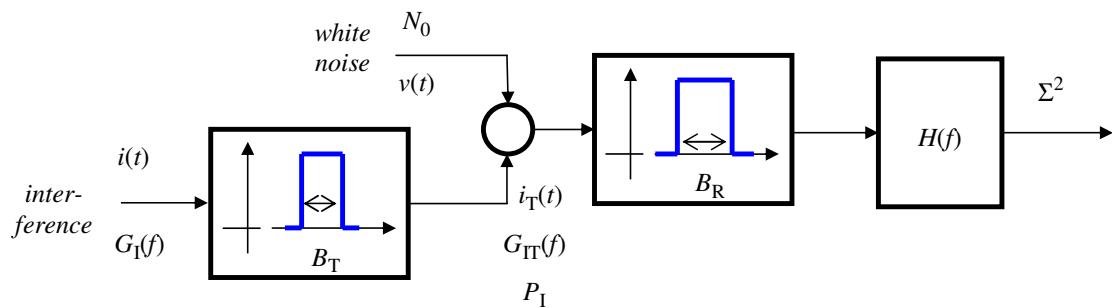


Figure 4-3, Matched filter equivalent to GNSS receiver

A spectral separation coefficient between two signals in the notation of [Pratt and Owen 2003] and generalising to include effect of bandwidth limiting B_R in the receiver and bandwidth limiting B_T in an interference transmitter is as follows.

$$\kappa_{IS} = \int_{-\infty}^{+\infty} \Phi_I(f) \times \Phi_S(f) df \quad 4-1$$

$\Phi_I(f)$ is a normalised power spectral density of the interfering signal and $\Phi_S(f)$ is the normalised power spectral density of the wanted signal where

$$\begin{aligned} \Phi_S(f) &= \frac{G_S(f)}{\int_{-B_R/2}^{+B_R/2} G_S(f) df} & |f| < B_R / 2 \\ &= 0 & |f| \geq B_R / 2 \end{aligned} \quad 4-2$$

and

$$\begin{aligned} \Phi_I(f) &= \frac{G_I(f)}{\int_{-B_T/2}^{+B_T/2} G_I(f) df} & |f| < B_T / 2 \\ &= 0 & |f| \geq B_T / 2 \end{aligned} \quad 4-3$$

One can also define a ‘separation coefficient’ of a signal with itself

$$\kappa_{SS} = \int_{-\infty}^{+\infty} \Phi_S(f)^2 df \quad 4-4$$

In [Pratt and Owen 2003] it is shown that the separation coefficient can be partitioned into partial spectral separation coefficients as follows.

$$\kappa_{IS} = \int_{f \in f_2} \Phi_I(f) \times \Phi_S(f) df + \int_{f \notin f_2} \Phi_I(f) \times \Phi_S(f) df \quad 4-5$$

f_2 is a partitioning frequency. Partial coefficients allow the contribution to the signal degradation to be quantified for different parts of the interference source. Therefore, the contribution to signal degradation of the main lobes of the interfering signal can be separated from the contribution by the side-lobes. The partial coefficient frequency range is adjusted by setting f_2 . Thus, spectral separation coefficients provide a method for selecting the optimum combination of GNSS signals in a given bandwidth and enable evaluation of sub-carrier phasing choices.

BOC modulation therefore can provide a more efficient use of an allotted bandwidth and the BOC Subcarrier phasing can be used to minimise interference between signals and systems.

4.2 Correlation functions

A BOC signal is created through modulation of a PRN sequence, $a(t)$ by a square wave sub-carrier, $s(t)$ represented as follows.

$$b(t) = a(t) \times s(t)$$

4-6

The periodic autocorrelation of a BOC modulated signal can be written as

$$\mathcal{A}(\tau) = \frac{1}{NT_c} \int_0^{NT_c} b(t)b(t+\tau)dt \quad 4-7$$

where N is the PRN code length in chips and T_c is the chip period.

The autocorrelation envelopes of BOC signals produce sets of triangle functions with positive and negative peaks. The autocorrelations of a BOC(10, 5) signal with no filtering and a front-end bandwidth of 24MHz respectively are shown in Figure 4-4 (derived from a Matlab Simulink simulation).

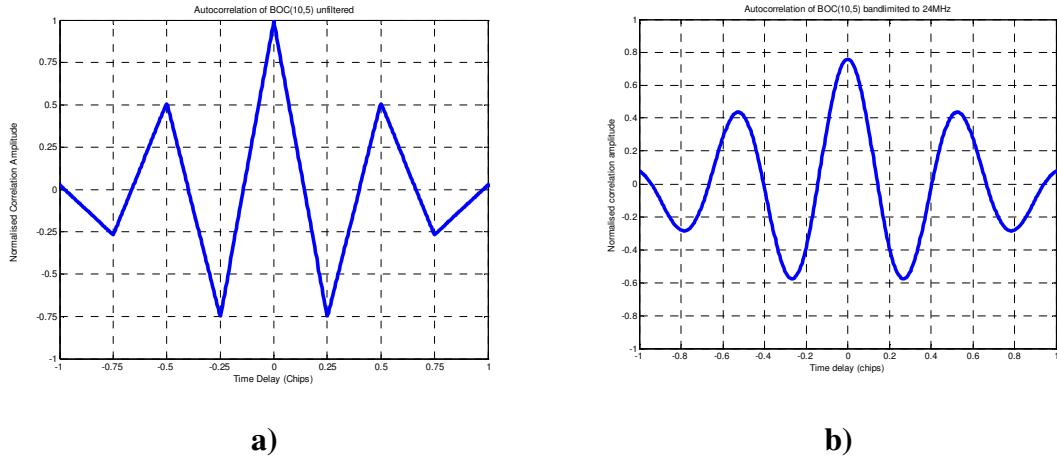


Figure 4-4, Autocorrelations of BOC(10, 5) signals: a) unfiltered b) 24MHz bandwidth

Conventional GNSS receivers subtract the difference of correlations by replica signals advanced ('early') and retarded ('late') in time to form a code discriminator curve (Figure 4-5). This discriminator gives the receiver code loop an error signal, required to steer the loop toward the correct correlation between the incoming signal and locally generated ('prompt') replica. The PSK discriminator has only one stable code loop state, one 'zero crossing'.

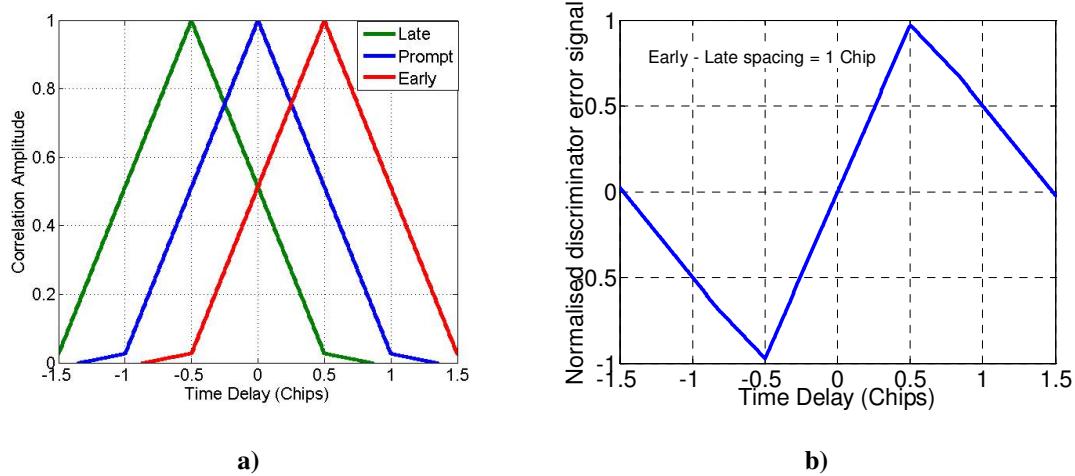


Figure 4-5, a) Autocorrelations of time delayed early, prompt and late PSK signals b) PSK discriminator curve

The multiple correlation peaks of BOC modulated signals result in several stable code loop states where only the central peak represents the correct correlation between the incoming signal and locally generated replica (Figure 4-6). This introduces an ambiguity in the receiver's code tracking loop, which can potentially lock to an

incorrect peak causing a large ranging error. This effect has been referred to as ‘BOC tracking ambiguity’ or ‘false-lock points’ [Bello and Fante 2005]. The ambiguity is exacerbated by band-limiting the signal, which increases the ratio of the largest incorrect peak to the correct peak, resulting in a greater probability of false tracking.

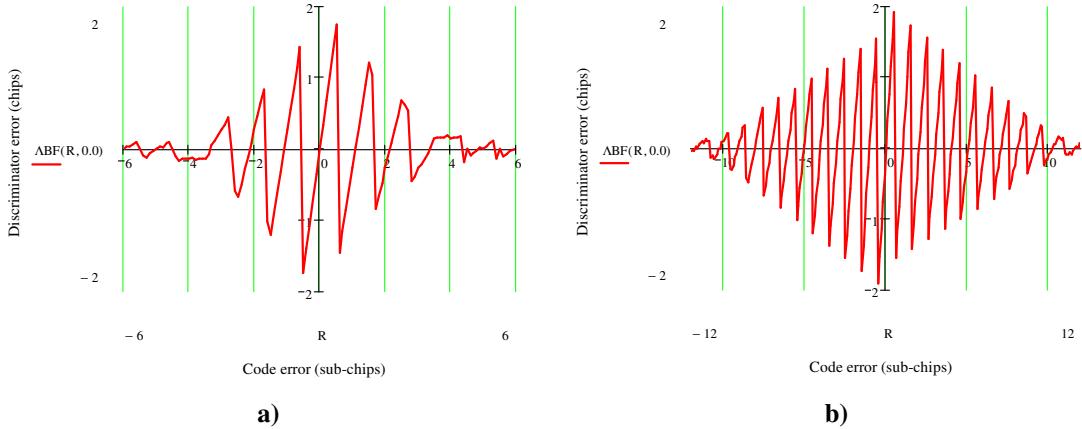


Figure 4-6, BOC discriminator curves a) BOC($2 \times f_c, f_c$) b) BOC($6 \times f_c, f_c$)

There are numerous techniques proposed in the literature for unambiguous tracking of BOC signals, each with varying degrees of ambiguity resolution and each with unique implications on receiver performance and complexity. The techniques proposed in the literature are detailed in Section 5.4. A novel BOC tracking technique developed during this research provides the best current solution to this problem and is described in detail in Chapter 6.

The phasing of the BOC sub-carrier also has an effect on correlation function and therefore, the code tracking accuracy of the receiver. Providing the receiver front-end bandwidth is large enough to support it, the correlation function of a BOC signal with cosine sub-carrier becomes markedly sharper than the equivalent sine sub-carrier correlation. Figure 4-7 shows BOC correlation functions with sine and cosine sub-carrier phasing.

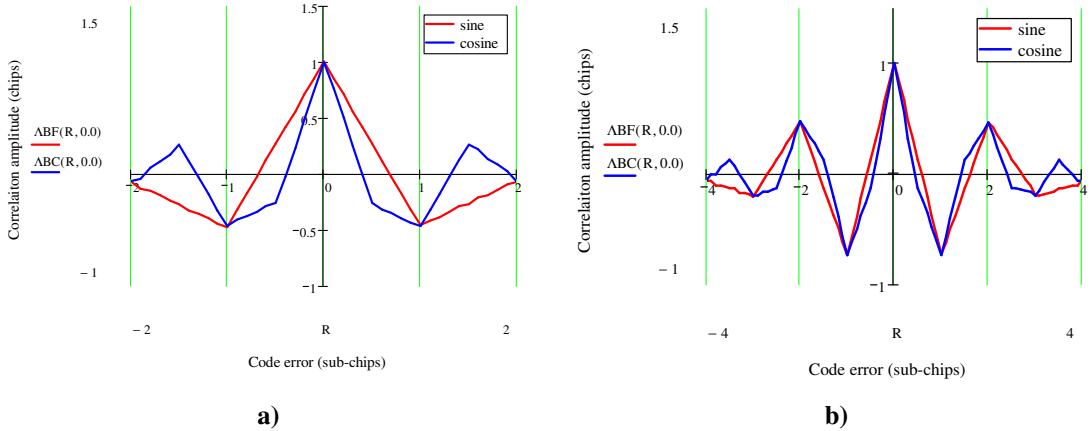


Figure 4-7, BOC correlation functions with different sub-carrier phasing

a) BOC(f_c, f_c) b) BOC($2 \times f_c, f_c$)

The sharpening of the correlation has a follow-on effect on the discriminator curve as shown in Figure 4-8 with no filtering. For a given correlation signal to noise the r.m.s. timing jitter is inversely proportional to the slope of the discriminator curve at the zero crossing. Therefore, cosine BOC modulation can provide better noise performance than sine BOC, but only for low ratios of sub-carrier to code ratio. This is bought at the expense of widening the effective bandwidth of the signal (see Figure 4-2), which is shown in [Ries *et al* 2003] to increase correlation losses for narrowband receivers, effectively cancelling any benefit. For wideband receivers the benefit of cosine BOC tends to zero with increasing sub-carrier to code ratios. Expressions for sine and cosine BOC timing accuracy are given and the relative benefits of each quantified in Section 4.4 of this chapter.

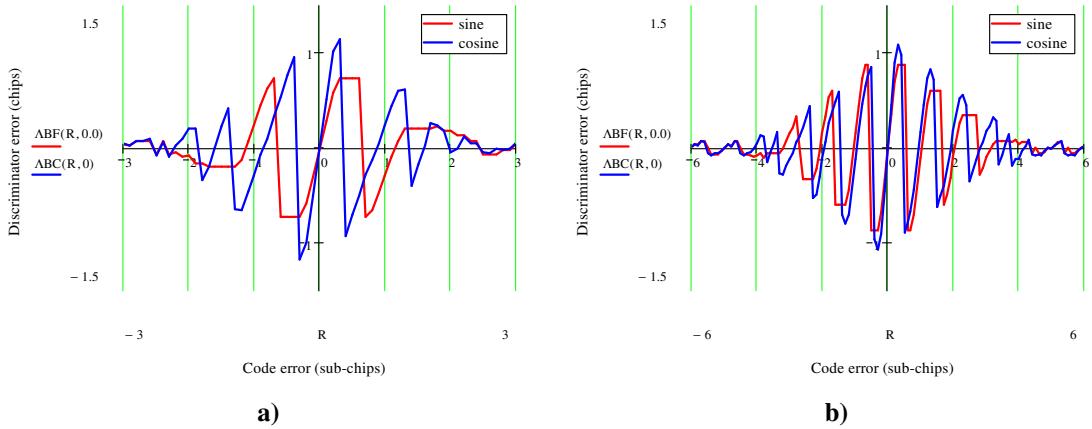


Figure 4-8, BOC discriminator curves with different sub-carrier phasing

a) BOC(f_c, f_c) b) BOC($2 \times f_c, f_c$)

4.3 Theoretical timing measurement of PSK modulated signals

A number of different approaches can be adopted to estimate the precision with which a GNSS receiver can calculate the time of arrival of the GNSS signals. The Cramér-Rao lower bound is commonly used to describe the theoretical performance limit of a time of arrival estimator. Defining a code loop bandwidth, B_L , carrier power C and noise density N_o , the Cramér-Rao lower bound states the variance of the code tracking error can be written as follows [Betz and Kolodziej斯基 2000].

$$\Sigma_{CR}^2 = \frac{B_L}{(2\pi)^2 \frac{C}{N_o} \int_{-\beta_R/2}^{\beta_R/2} f^2 S(f) df} \quad 4-8$$

β_R is the receiver front-end bandwidth, $S(f)$ is the normalised power spectral density of the GNSS signal and the square root of the integral is known as the r.m.s. or Gabor bandwidth.

Therefore, substituting from Equation 3–7 the code tracking jitter of a PSK signal normalised to its chip width T_C , can be written as

$$\begin{aligned} \sigma_{CR}^2 &= \left(\frac{\Sigma_{CR}}{T_C} \right)^2 = \frac{B_L}{(2\pi)^2 \frac{C}{N_o} T_C^3 \int_{-\beta_R/2}^{\beta_R/2} f^2 \sin c^2(\pi f T_C) df} \\ &= \frac{B_L}{2\beta_R T_C \frac{C}{N_o} [1 - \sin c(\pi \beta_R T_C)]} \\ &\approx \frac{B_L}{2b \frac{C}{N_o}} \quad \text{for } b > 1 \end{aligned} \quad 4-9$$

where $b = \beta_R \times T_C$ is the normalised receiver front-end bandwidth.

The theory given by Cramér-Rao is only a lower bound and strictly applies only in the limit of an infinite signal to noise. Therefore, a more robust analysis is required for

true approximation of timing jitter across various noise levels [Betz and Kolodziejksi 2000].

Precise understanding of the potential timing accuracy of GNSS systems can be achieved using a simple equivalent filter model of the GNSS receiver. Timing recovery in a GNSS navigation system can be reduced down to the problem of locating a pulse in the presence of additive noise. Here we show how this approach can be used to produce models of timing accuracy equivalent to those derived using complex loop analysis.

Dr MS Hodgart suggested simplifying the problem by assuming carrier demodulation and considering a single channel base-band model. The simplified base-band PSK received signal can be written as follows.

$$x_{PSK}(t) = A \times \square(t - \tau) + n(t) \quad 4-10$$

The ‘ \square ’ symbol represents a pulse equivalent to one chip of the PRN code sequence with unknown time delay of τ . $n(t)$ is additive noise assumed to be white and Gaussian.

We model the receiver timing recovery by an ideally rectangular matched filter and a delay line subtractor as shown in Figure 4-9. The output of the delay line subtractor can be written as follows.

$$z(t) = A \times v^\Lambda(t - \tau) + w(t) \quad 4-11$$

The ‘ v^Λ ’ symbol is equivalent to the coherent (assuming perfect carrier demodulation) discriminator created by the subtraction of early and late signals in a GNSS receiver (see Figure 4-5). The time delay T_D is equivalent to the spacing in time between the early and late signals, limited to $0 < T_D \leq T_C$.

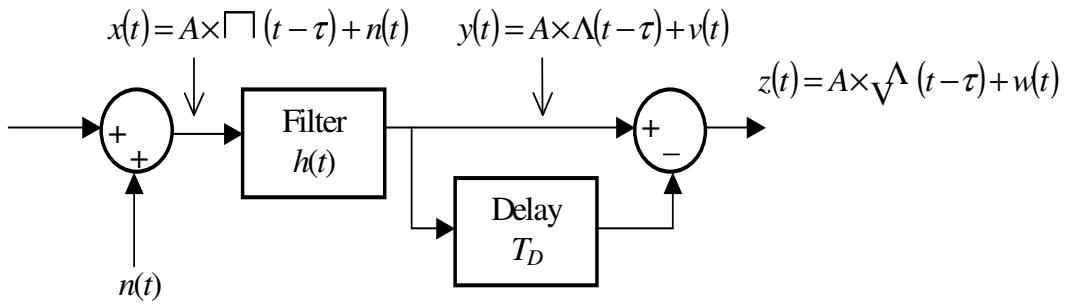


Figure 4-9, Timing recovery model of PSK GNSS receiver

The linear zero crossing of the discriminator characteristic represents the correct timing of the received pulse. Additive noise bounded within the tracking range of the discriminator ($\pm T_D/2$) converts directly to a timing error.

Figure 4-10 shows representations of the function realised by the timing recovery model.

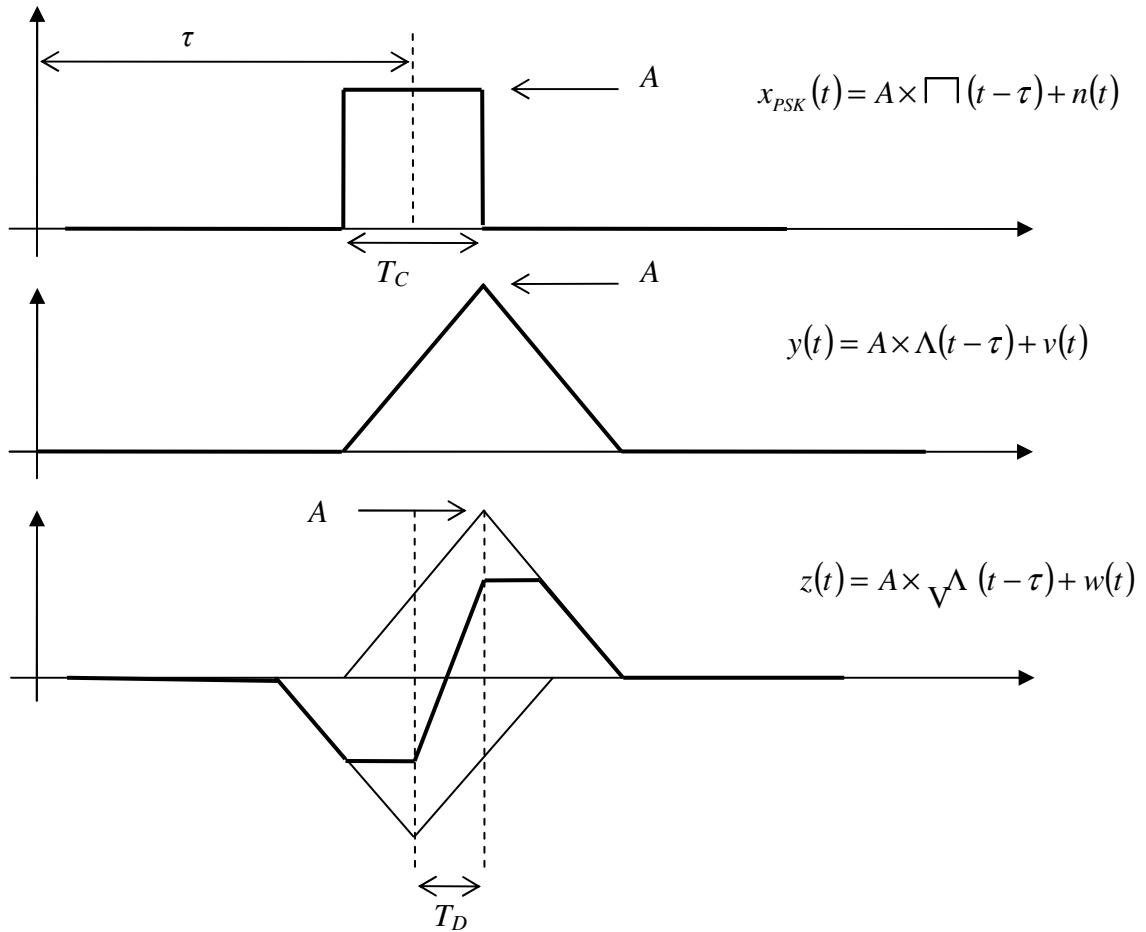


Figure 4-10, Representations of the PSK timing model functions

A noise sample w , can be converted to a timing error as

$$\epsilon = \frac{w}{dz/dt} \quad 4-12$$

where $\frac{dz}{dt} = \frac{2 \times A}{T_c}$ is the slope of the discriminator characteristic at the zero crossing. The mean square timing jitter is then

$$\Sigma^2 = \langle \epsilon^2 \rangle = \frac{\langle w^2 \rangle}{\left(\frac{dz}{dt} \right)^2} \quad 4-13$$

The mean square noise output from the filter is

$$\begin{aligned} \langle w^2 \rangle &= \frac{\eta}{2} \int [h(t) - h(t - T_D)]^2 dt \\ &= \eta \times \frac{T_D}{T_c^2} \end{aligned} \quad 4-14$$

where η is the one sided white noise density. Now substituting into Equation 4-13 we have the mean square jitter on a single pulse

$$\Sigma^2 = \frac{1}{4} \times \frac{T_D}{A^2 \eta} \quad 4-15$$

In practical systems the noise is reduced by averaging a great number of pulses over integration time T . We define an averaging loop with loop bandwidth $B_L = 1/(2 \times T)$, input carrier power C and input noise density N_0 . The mean square timing jitter for PSK normalised to the chip width can then be written as

$$\sigma_{PSK}^2 = \left(\frac{\Sigma_{PSK}}{T_c} \right)^2 = \frac{B_L \times \Delta_{PSK}}{2 \times C/N_0} \quad 4-16$$

where $\Delta_{PSK} = T_D/T_C$ is the normalised early-late discriminator spacing width. This equation corresponds to the standard equation for timing jitter for coherent early minus late discriminators given in [Parkinson and Spilker 1996] and [Ries *et al* 2002].

In [Betz and Kolodziejki 2000] extensive analysis of GPS code tracking accuracy, which has been widely accepted by the scientific community is given covering any degree of band-limiting of the signal. PSK receivers are categorised into three distinct groups, those who are limited by the receiver's early-late spacing (*spacing limited*), those who are limited by the receiver's front-end bandwidth, (*bandwidth limited*) and those who are in transition between (*transition*). Figure 4-11 shows the three groups as a function of normalised receiver front-end bandwidth and early-late spacing.

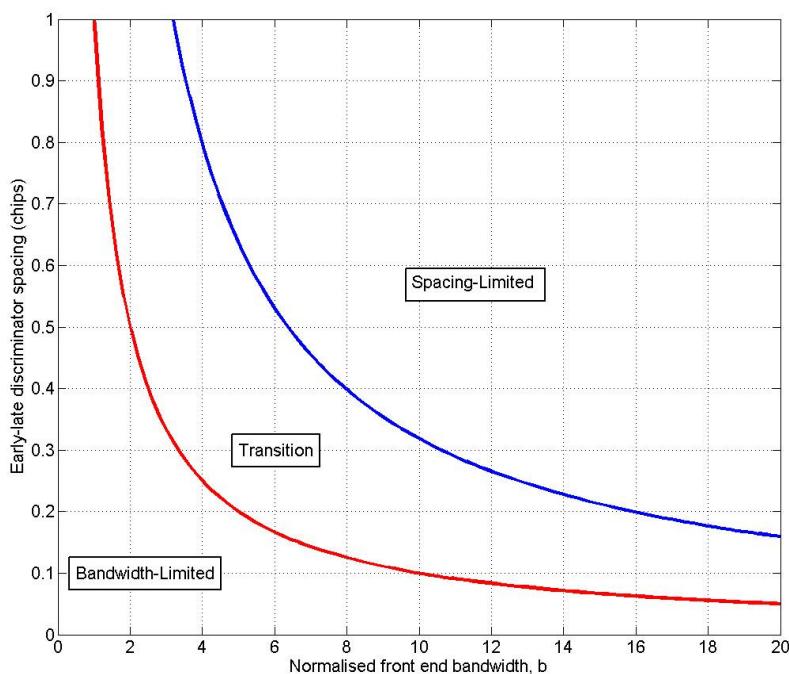


Figure 4-11, PSK receiver groups

The analysis of coherent early-late discriminator produced the following timing jitter equations for the three groups.

$$\sigma_{PSK} = \begin{cases} \frac{B_L \times \Delta}{2 \times C/N_0} & \text{for } \pi \leq \Delta \times b \\ & \text{(spacing limited)} \\ \frac{B_L}{2 \times C/N_0} \times \left[\frac{1}{b} + \frac{b}{\pi - 1} \left(\Delta - \frac{1}{b} \right)^2 \right] & \text{for } 1 < \Delta \times b < \pi \\ & \text{(transition)} \\ \frac{B_L}{2 \times C/N_0} \times \frac{1}{b} & \text{for } \Delta \times b \leq 1 \\ & \text{(bandwidth limited)} \end{cases} \quad 4-17$$

Equation 4–17 is equivalent to the timing analysis given here for the *spacing limited* group which is true for $\Delta \times b \geq \pi$. Note also that for *bandwidth limited* receivers Equation 4–17 corresponds to the timing jitter predicted by the Cramér-Rao lower bound in Equation 4–9. This indicates that there is no benefit to reducing the early-late spacing beyond the reciprocal of the front-end bandwidth.

4.4 Theoretical timing measurement of BOC modulated signals

The theoretical timing accuracy of a BOC GNSS system can be evaluated in precisely the same manner as shown for PSK system in the previous section. Again the problem is reduced to the optimal location of a pulse in the presence of additive noise. We assume that the receiver is maintaining lock on the central peak of the BOC correlation, which corresponds to the correct timing location. The mean square timing jitter can then be evaluated by comparison of the slope of the discriminator with the r.m.s. noise.

The slope of the sine sub-carrier BOC discriminator is $2 \times A \left(2 - \frac{T_s}{T_c} \right)$ and the slope of the cosine sub-carrier BOC discriminator is $2 \times A \left(2 + \frac{T_s}{T_c} \right)$ as shown in Figure 4-12.

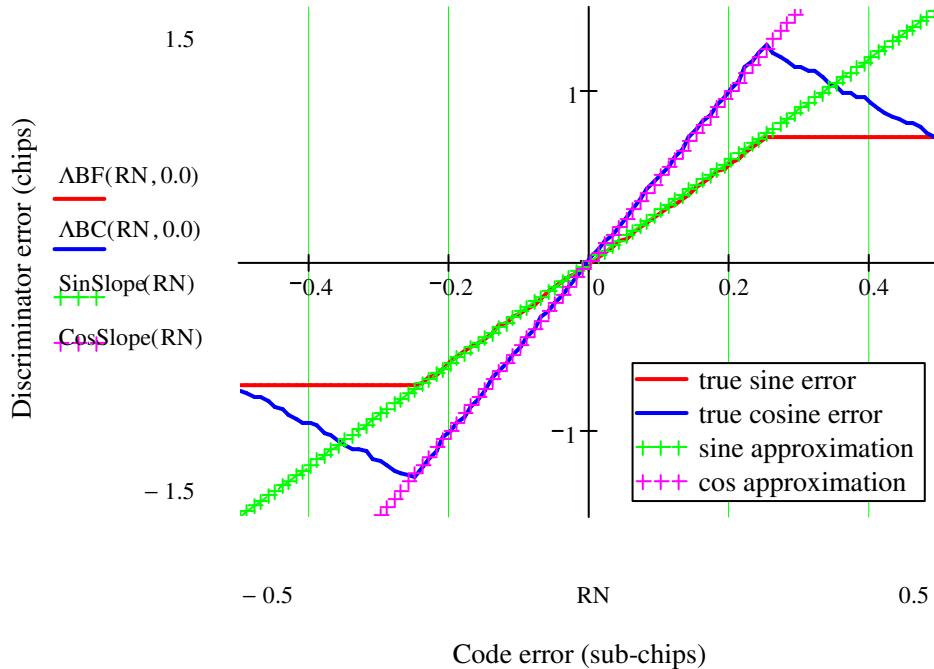


Figure 4-12, Sine and cosine BOC(f_c, f_c) discriminators with slope approximations

Appendix H shows the derivation of timing jitter for sine and cosine BOC modulated signals. Modelling the BOC timing recovery as a delay line subtractor we find the mean square timing jitter for sine BOC as follows.

$$\Sigma_{BOCs}^2 = \frac{2 \times B_L}{C/N_0} \times \frac{1}{4 \left(2 - \frac{T_s}{T_c} \right)} \times T_D \times T_s \quad 4-18$$

T_s is the sub-chip width and T_D is a delay equivalent to the early-late discriminator spacing limited to $0 < T_D \leq T_s$ for sine BOC or $0 < T_D \leq \frac{T_s}{2}$ for cosine BOC.

The equivalent expression for cosine BOC is

$$\Sigma_{BOCc}^2 = \frac{2 \times B_L}{C/N_0} \times \frac{1}{4 \left(2 + \frac{T_s}{T_c} \right)} \times T_D \times T_s \quad 4-19$$

Table 4-1 shows the resulting timing jitter formulations with various sub-carrier to code ratios for sine and cosine BOC.

Table 4-1, Timing jitter of BOC signals

Signal	Timing jitter		Relative timing benefit of cosine sub-carrier
	Sine	Cosine	
BOC(f_c, f_c)	$\frac{2 \times B_L}{C/N_0} \times \frac{1}{6} \times T_D \times T_S$	$\frac{2 \times B_L}{C/N_0} \times \frac{1}{10} \times T_D \times T_S$	1.66
BOC($1.5 \times f_c, f_c$)	$\frac{2 \times B_L}{C/N_0} \times \frac{3}{20} \times T_D \times T_S$	$\frac{2 \times B_L}{C/N_0} \times \frac{3}{28} \times T_D \times T_S$	1.40
BOC($2 \times f_c, f_c$)	$\frac{2 \times B_L}{C/N_0} \times \frac{1}{7} \times T_D \times T_S$	$\frac{2 \times B_L}{C/N_0} \times \frac{1}{9} \times T_D \times T_S$	1.29

As shown in Table 4-1 there is only a small benefit in terms of timing jitter (2.2dB maximum) to cosine BOC and only for low ratios of sub-carrier to code rate. For high ratios Equation 4-18 and Equation 4-19 are asymptotic to the following result.

$$\Sigma_{BOC}^2 = \frac{B_L}{4 \times C/N_0} \times T_D \times T_S \quad 4-20$$

It is common in the literature to normalise the mean square jitter to the chip width, normalising Equation 4-20 gives

$$\begin{aligned} \sigma_{BOC}^2 &= \left(\frac{\Sigma_{BOC}}{T_C} \right)^2 = \frac{B_L}{4 \times C/N_0} \times \frac{T_D \times T_S}{T_C^2} \\ &= \frac{B_L \Delta_{BOC}}{2 \times C/N_0 \times \frac{4f_s}{f_c}} \end{aligned} \quad 4-21$$

where $\Delta_{BOC} = T_D/T_C$ is the normalised early-late discriminator spacing, f_s is the sub-carrier frequency and f_c is the chipping rate. This equation corresponds to the equations derived for timing jitter for coherent early minus late BOC discriminators given in [Ries *et al* 2002]. However, we disagree with the authors about the implications of this result. Comparing Equation 4-21 to the standard PSK timing

jitter (Equation 4–16) the authors claim that BOC modulation reduces the mean square timing jitter by a factor of $4f_s/f_c$ when compared to PSK. This supposed advantage depends on a normalisation to the chip width, which does not provide a fair basis for comparison. For example, this implies comparing PSK-R(1) with BOC signals such as BOC(1,1), BOC(2,1) and BOC(6,1). Clearly these signals have vastly different bandwidth requirements and this is not a like-for-like comparison. The timing jitter must be evaluated in absolute terms to provide a fair comparison between BOC and PSK in an available bandwidth. The PSK and BOC timing jitter equations in absolute terms are as follows.

$$\begin{aligned}\Sigma_{PSK}^2 &= \frac{B_L}{2C/N_0} \times T_D \times T_C & 4-22 \\ \Sigma_{BOC}^2 &= \frac{B_L}{2C/N_0 \frac{4f_s}{f_c}} \times T_D \times T_C = \frac{B_L}{4C/N_0} \times T_D \times T_S\end{aligned}$$

The *processing rate* of a GNSS signal provides a fair basis of comparison. PSK and BOC systems have the same processing rate if the chip width T_C , of the PSK signal is set equal to BOC sub-chip width T_S . Then from Equation 4–22 we can see that the theoretical timing advantage of BOC modulation reduces to a factor of 2 for equal early-late separation. If we wish to compare normalised quantities, we must normalise BOC signals with respect to the sub-chip width as follows.

$$\begin{aligned}\sigma_{*BOC}^2 &= \left(\frac{\Sigma_{BOC}}{T_S} \right)^2 = \frac{B_L}{4 \times C/N_0} \times \frac{T_D}{T_S} \\ &= \frac{B_L \times \Delta_{BOC}}{4 \times C/N_0}\end{aligned} \quad 4-23$$

Comparing Equation 4–23 with the equivalent normalised PSK jitter given in Equation 4–16 results in a factor of improvement for BOC modulated signals. BOC modulation therefore provides a small timing advantage (3dB maximum) over equivalent PSK systems on this basis of comparison.

4.5 PSK and BOC multipath analysis

The simplest and most common way [Irsigler *et al* 2004] of evaluating the timing location error induced by the presence of multipath is to consider the effect of a single interfering multipath signal with various relative time delays. The multipath signal has the effect of shifting the code or carrier discriminator's zero crossing away from the correct timing location, this is depicted in Figure 4-13. The error induced by the presence of the multipath signal is then calculated from difference in the timing of the new zero-crossing from the correction timing location. This provides only a worse case analysis of error due to multipath but does provide an adequate performance measure with which we can compare PSK and BOC signals.

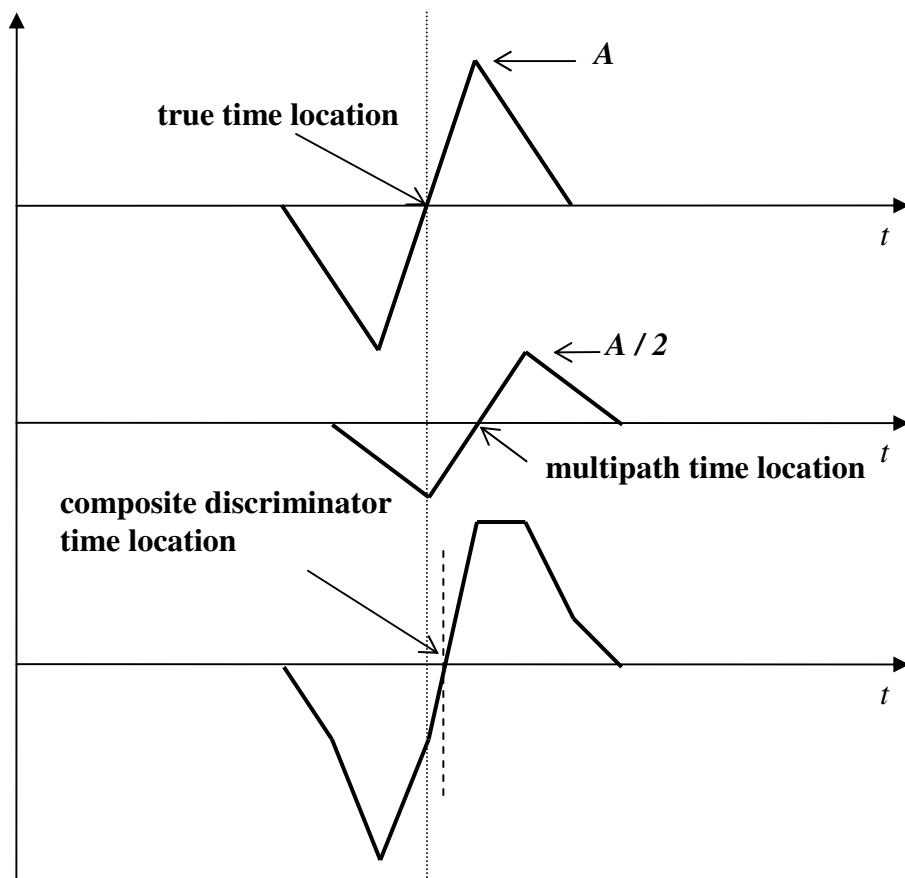


Figure 4-13, Depiction of discriminator error induced by the presence of multipath

The relative amplitude of the multipath interferer is defined by the coefficient of reflection, α . In all analysis presented here we assumed the maximum relative amplitude of multipath signal to be half amplitude ($\alpha = 0.5$). A multipath error

envelope can then be computed over various multipath time delays. The multipath error envelope for a PSK-R(1) modulation is shown in Figure 4-14 derived from Mathcad simulation (see Appendix B for details of the simulation). The carrier phase of the relative multipath is simulated at a worst-case of 0° and 180° . This results in the two sides of the multipath error envelope.

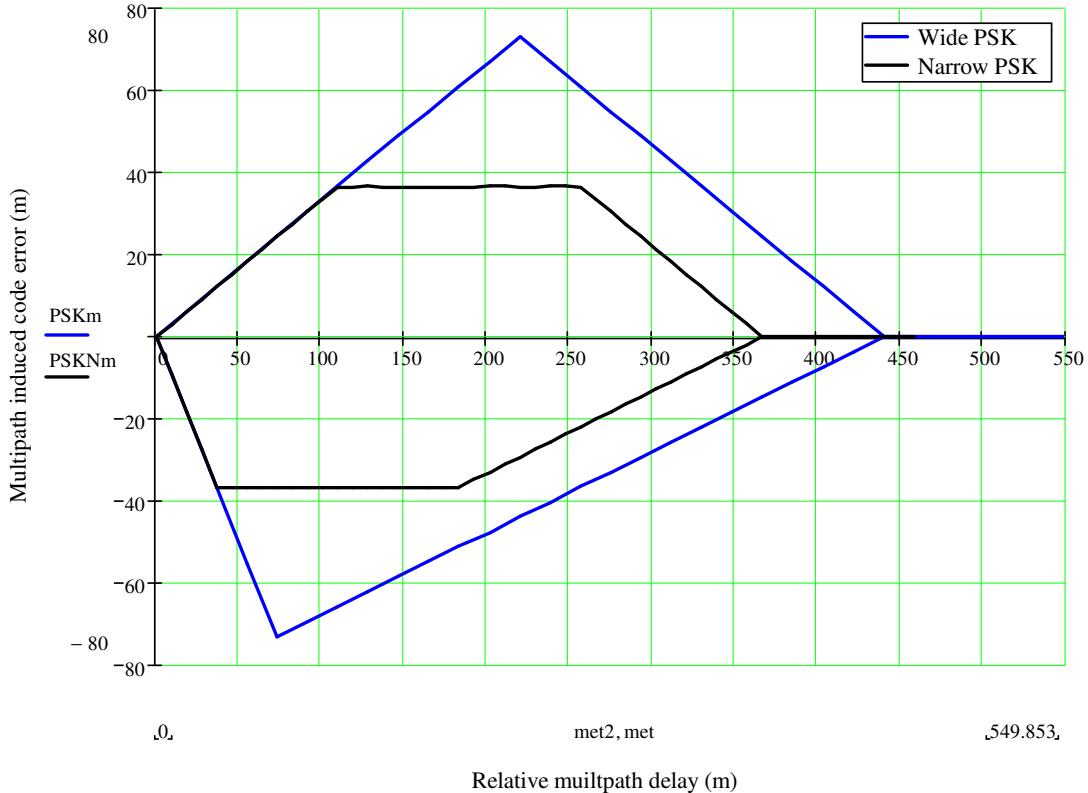


Figure 4-14, Multipath error envelopes for wide PSK ($T_D = T_C$) and narrow PSK ($T_D = T_C/2$)

The multipath induced error only occurs across the range of the PSK discriminator characteristic ($T_C + T_D/2$). Reducing the early-late discriminator spacing restricts the range over which the multipath signal can affect the discriminator. Also, the reduction in discriminator spacing flattens the discriminator, which limits the maximum error induced by the multipath. Therefore, narrow discriminator spacing can reduce timing jitter and multipath induced errors.

When considering PSK and BOC multipath performances it is common in the literature to make a comparison by setting equal chip widths [Irsigler *et al* 2004]. For example, comparing PSK-R(1) to BOC(1,1) as shown in Figure 4-15 for which we find agreement with the published results. However, this results in the suggestion that

BOC modulation provides better multipath error performance over PSK. This is again not a fair basis for comparison, for exactly the same reason as given for the timing jitter performance, clearly the processing rate of BOC(1,1) is twice that of PSK-R(1).

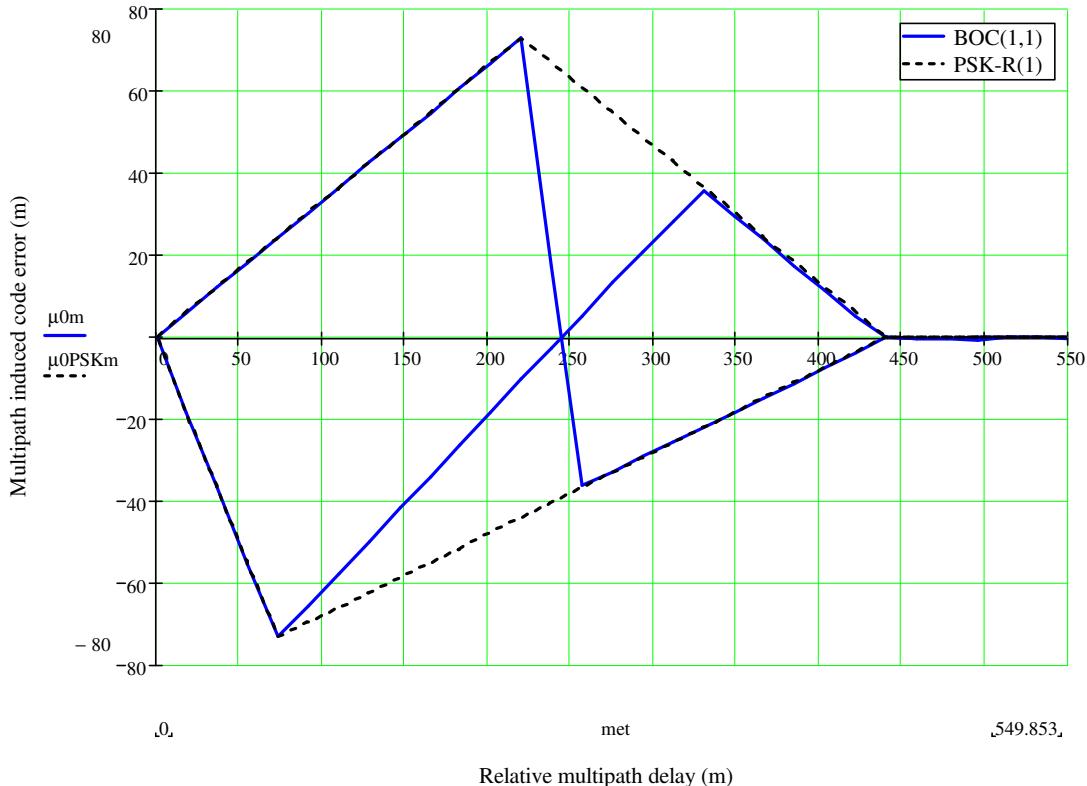


Figure 4-15, Multipath error envelopes of PSK-R(1) and BOC(1,1) signals
 $(T_D = 2 \times T_S^{(BOC)} = T_C^{(PSK)})$

In contrast, a fair comparison between PSK and BOC can be made by setting equal discriminator spacings and equal processing rates. A comparison between PSK-R(2) and BOC(1,1) provides a fair comparison with both discriminator spacings equal to the sub-chip width ($T_D = T_S^{(BOC)} = T_C^{(PSK)}$). The multipath error envelopes are shown in Figure 4-16. A clearer view of the relative performance of the two modulations can be seen by examining the running average error across the dataset, as shown in Figure 4-17. It can be seen that on a like-for-like basis BOC modulation outperforms PSK for short-range multipath delays. The lines intersect indicating equal

performance over the range of the PSK discriminator $\left(T_C^{(PSK)} + \frac{T_D^{(PSK)}}{2}\right)$. However,

across the entire range of delays PSK has a 14.7% lower average multipath error than

the equivalent BOC modulation. The degradation of BOC performance at long-range multipath delays is due to the secondary peaks in the BOC correlation.

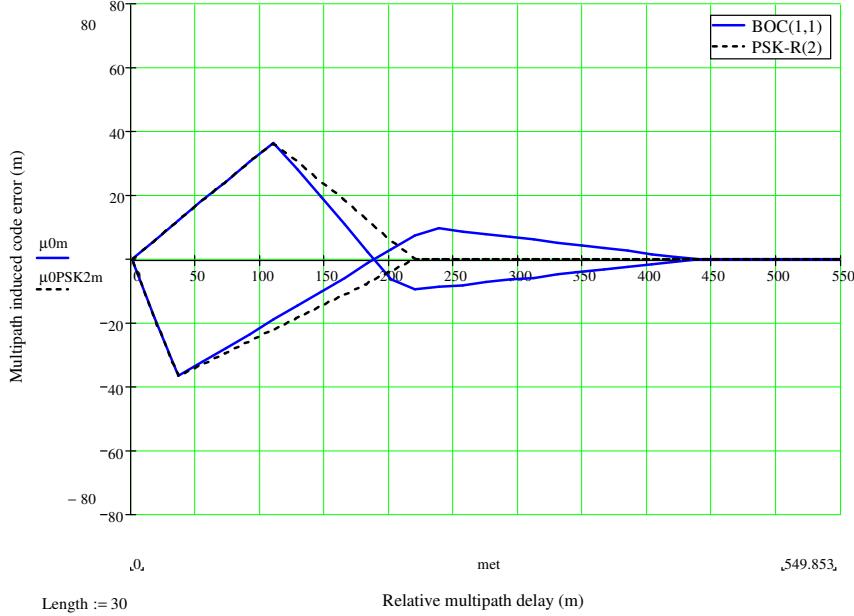


Figure 4-16, Multipath error envelopes for PSK-R(2) and BOC(1,1) signals
 $(T_D = T_S^{(BOC)} = T_C^{(PSK)})$

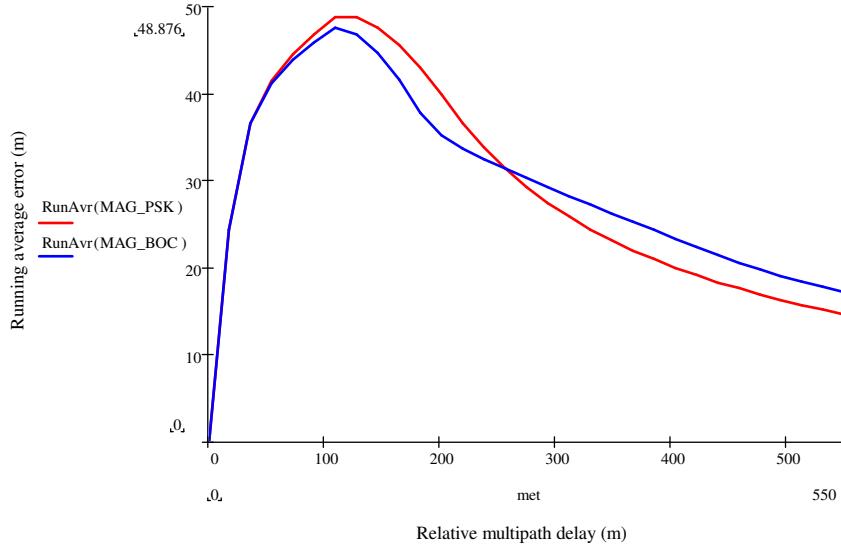


Figure 4-17, Running average multipath error of PSK-R(2) and BOC(1,1) signals
 $(T_D = T_S^{(BOC)} = T_C^{(PSK)})$

Doubling the processing rate we compare PSK-R(4) with BOC(2,1) modulation as shown in Figure 4-18 and Figure 4-19. Again BOC modulation outperforms PSK at short range multipath and the performances converge at the width of the PSK discriminator. However, the additional secondary peaks in the BOC correlation

degrade the overall performance such that the average PSK error is now 39.6% lower than the equivalent BOC error.

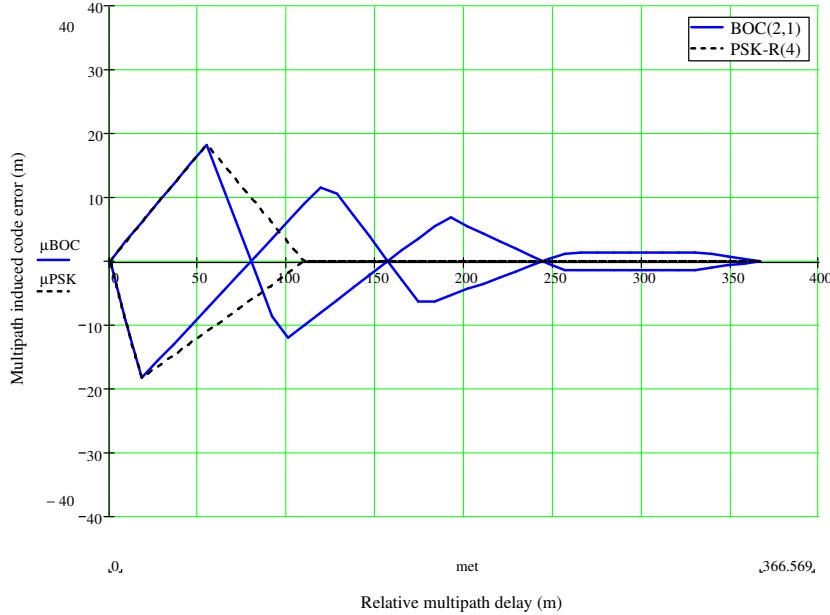


Figure 4-18, Multipath error envelopes for PSK-R(4) and BOC(2,1) signals ($T_D = T_S$)

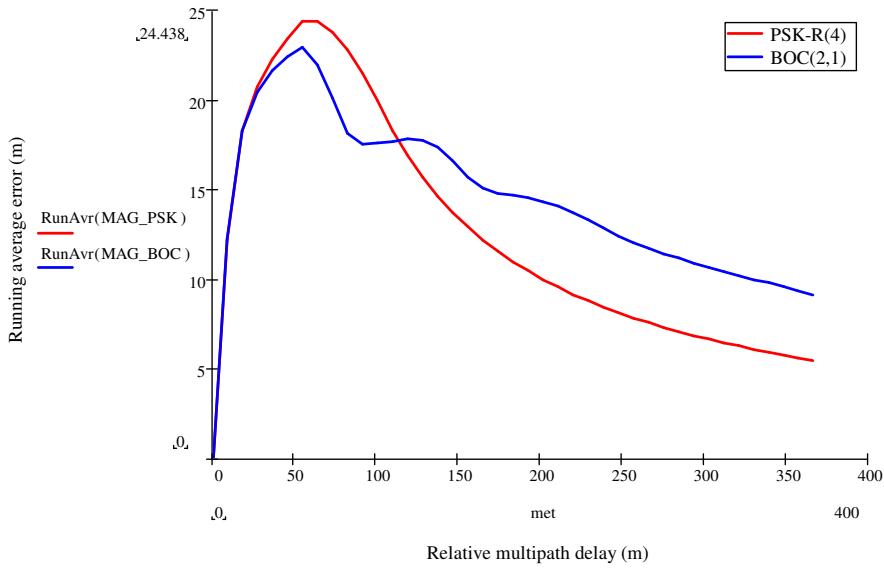


Figure 4-19, Running average multipath error of PSK-R(4) and BOC(2,1) signals ($T_D = T_S$)

The carrier phase error induced by multipath signals is closely related to the signal's fundamental correlation function (see Section 5.2 for a illustrative examples). Therefore, the multipath induced error envelope follows the envelope of correlation function, as shown in Figure 4-20 for PSK-R(4) and BOC(2,1). The running average carrier phase error is shown in Figure 4-21. BOC outperforms PSK at multipath

delays less than the PSK chip width where the multipath performance converges. Despite this, across all multipath delays the PSK signal significantly outperforms the equivalent BOC signal (63% improvement).

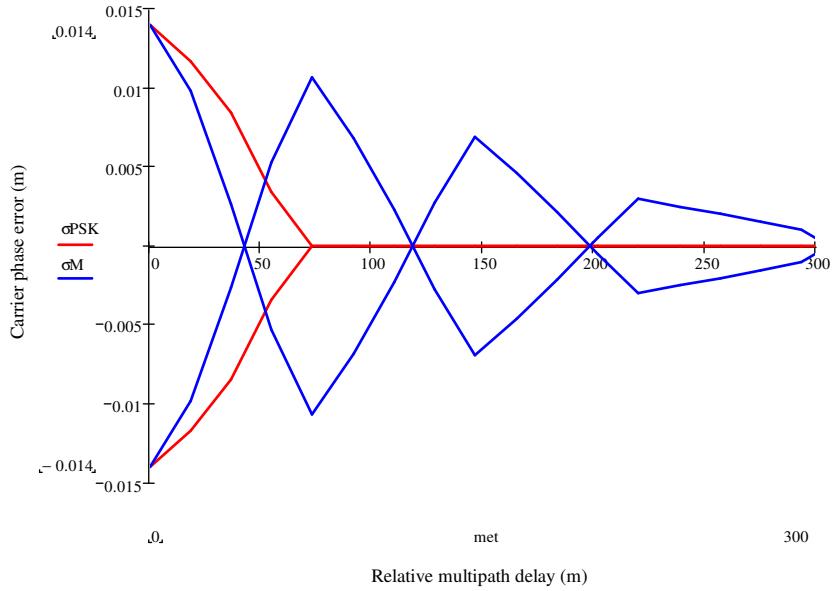


Figure 4-20, Multipath induced carrier phase error envelopes for PSK-R(4) and BOC(2,1) signals

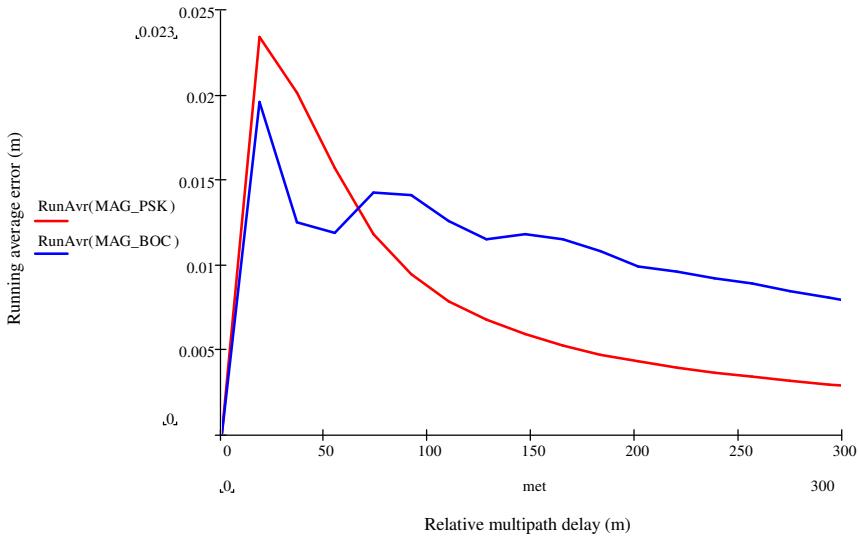


Figure 4-21, Running average carrier phase multipath error of PSK-R(4) and BOC(2,1) signals

Long range multipath is generally easier to distinguish and mitigate, therefore BOC modulation potentially offers better performance than PSK for complex multipath mitigating receivers. However, for receivers which either do not attempt to correct

for multipath errors or rely on correlator techniques such as narrow discriminator spacing, BOC can be considerably worse than the equivalent PSK system.

To summarise the discussion given in this chapter we consider the advantages and disadvantages of BOC modulation. The advantages of implementing a GNSS system with BOC modulation rather than the conventional PSK modulation are as follows.

- Spectral separation – BOC modulation provides a method of re-using frequency allocations in a bandwidth efficient way. This can provide spectral separation between signals within the same bandwidth allocation and therefore reduce the amount of interference between the signals. The spectral separation also enables filters to be employed to isolate individual signals.
- Interference regulation – BOC sub-carrier phasing can be adjusted to regulate the amount of interference with neighbouring signals.
- Reduced timing jitter – BOC modulation results in a small improvement (3dB maximum) to the code timing jitter in the presence Gaussian noise over the equivalent PSK system.
- Increased resilience to short-range multipath – The BOC correlation function results in a small reduction in multipath induced code and carrier phase errors in the presence of short-range multipath.

The disadvantages of implementing a GNSS system with BOC modulation rather than the conventional PSK modulation are as follows.

- False locking points – The secondary peaks in the BOC correlation envelope result in multiple zero crossings across the discriminator characteristic, only one of which corresponds to the correct timing location. It is then possible for the receiver to be in a stable lock at a false zero crossing causing a gross error in the receivers timing location. This research has developed a new solution which we believe to be superior to any currently proposed in the literature. This issue is analysed in depth in Section 5.4 and Chapter 6.
- Complicating the search process – The nulls in the BOC correlation envelope complicate search process requiring additional receiver technology to achieve equivalent PSK performance. This issue is analysed in depth in Section 5.3.

- Poor long-range code and carrier multipath performance – Compared on a like-for-like basis PSK would seem to significantly outperforms BOC in the presence of long-range relative multipath delays.

In this chapter we have focused purely on the technical considerations, which must be addressed when choosing a specific GNSS signal modulation. Clearly, the choice of future GNSS signals is also driven both politically and programmatically.

5 Receiver theory

This chapter describes in detail the process of acquiring and tracking various types of GNSS signals. Detailed comparisons are drawn between different techniques and algorithms for both PSK and BOC receivers considering both performance measures and the relative hardware impact. The theory described here is incorporated into the receiver designs given in Chapters 8 and 10. This chapter begins by describing the techniques currently employed to locate and acquire PSK signals, followed by a review of the established tracking techniques for PSK signals. A summary of the more recent theory required for acquiring and tracking BOC signals is given with comparisons of the various techniques. This chapter outlines the problems facing receiver designers using conventional techniques for tracking BOC signals and details the current progress in addressing these problems.

A generic block diagram for a GNSS receiver is shown in Figure 5-1. Although there are a number of changes required to receive new generation GNSS signals, the generic functions of the receiver are still valid.

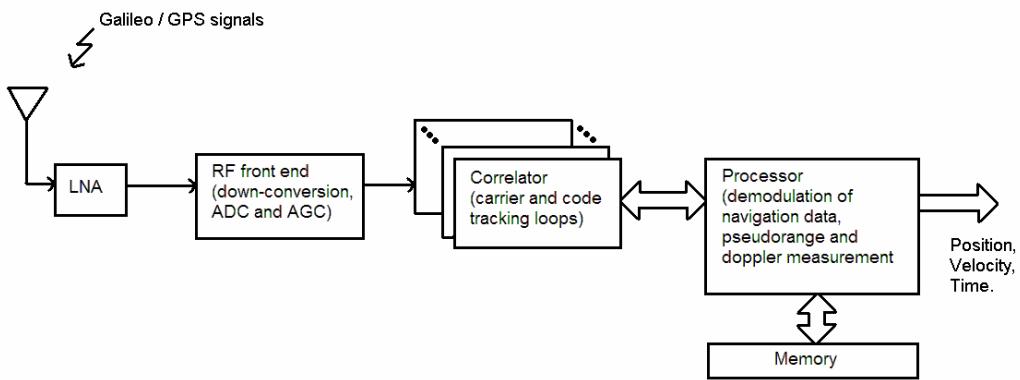


Figure 5-1, GNSS receiver block diagram.

GNSS signals are received through the use of a right-hand circularly polarised (RHCP) antenna and amplified using a low-noise amplifier (LNA), which essentially determines the receiver's noise figure. The radio frequency (RF) signals are down-

converted, typically in a number of stages, to an intermediate frequency (IF), sufficiently high in frequency to support the signal bandwidth.

The signal is then digitised by an analogue to digital converter (ADC), with automatic gain control (AGC) and the digital IF is then passed to the receiver's correlator channels. Here, the carrier signal and code sequence are removed from the signal by correlating the received signal with locally generated replicas. The processor then extracts the raw navigational data by monitoring the changes in phase angle. This data can be used in combination with phase information derived from the carrier and code tracking loops to form pseudorange and Doppler estimates, ultimately resulting in position, velocity and time information for the user.

5.1 Searching for PSK signals

Before GNSS signals can be used to solve for the receiver's position the signals must be found. The signals arriving at the receiver have an associated delay due to the distance between transmitter and receiver but have also been shifted in frequency. Therefore, the receiver must search in both frequency and delay (time) domains.

Assuming signal conditioning and down-conversion to a suitable IF we can model the received PSK signal as follows.

$$u_{PSK}(t) = A \times \cos(\omega_0 t + \phi) \times a(t - \tau) \times d \quad 5-1$$

A is the amplitude of the signal, ω_0 is the centre frequency of the IF signal, $a(t)$ is the PRN code sequence and d is the navigational data value having possible values of +1 and -1. τ is the time delay of the code and ϕ is a general phase shift implicitly allowing for time variation in phase as follows.

$$\phi = -\omega_0 \tau + \phi_0 \quad 5.2$$

ϕ_0 is an unrelated phase shift from the uncharacterised path from transmitter to receiver. Allowing a time varying delay, $d\tau/dt$ accounts for the Doppler shift $d\phi/dt$ on the incoming signal.

Additive noise and interfering signals are not present in this representation to simplify the following illustrations. The aim of a PSK receiver is to estimate the delay, τ and demodulate the incoming navigational data. This is accomplished using estimating correlators and feedback (a digital phase locked loop). The receiver produces replica in-phase and quadrature carrier signals with trial phase $\hat{\phi}$, which are mixed with the incoming signal. Subsequently, the signal is mixed with replica in-phase and orthogonal PRN codes with trial time delay $\hat{\tau}$. The orthogonal code sequence is defined as the difference between ‘*early*’ and ‘*late*’ time shifts of the code sequence, written as follows.

$$\tilde{a}(t - \hat{\tau}) = a\left(t - \hat{\tau} + \frac{T_{DC}}{2}\right) - a\left(t - \hat{\tau} - \frac{T_{DC}}{2}\right) \quad 5-3$$

T_{DC} is the total separation between the *early* and *late* replica waveforms, bounded by $T_{DC} \leq T_c$. Multiplication of the incoming signal by carrier and code replicas results in four correlation results denoted w_{II} , w_{QI} , w_{IQ} and w_{QQ} shown in Figure 5-2. The first subscript denotes mixing with an in-phase (I) or quadrature (Q) carrier replica, the second subscript denotes mixing with in-phase or quadrature (orthogonal) code replica.

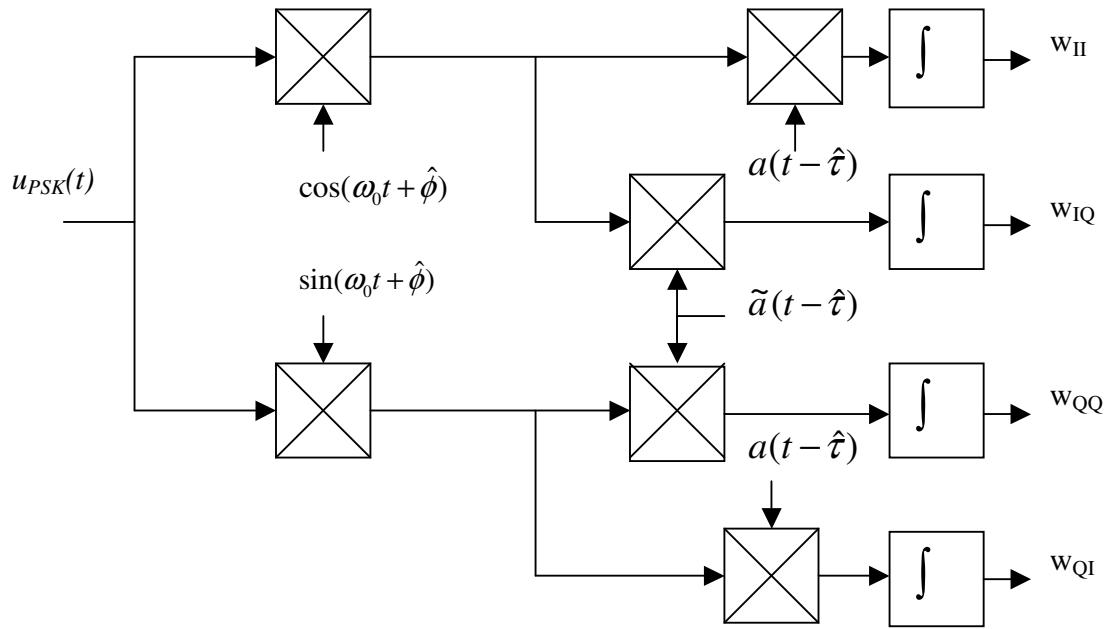


Figure 5-2, PSK correlator structure

As suggested by Dr Hodgart the resulting correlations can be written compactly using a four element matrix as follows.

$$\mathbf{W} = \begin{pmatrix} w_{II} & w_{IQ} \\ w_{QI} & w_{QQ} \end{pmatrix} = \frac{1}{T} \int_0^T u_{PSK}(t) \begin{pmatrix} \cos(\omega_0 t + \hat{\phi}) \\ \sin(\omega_0 t + \hat{\phi}) \end{pmatrix} \begin{pmatrix} a(t - \hat{\tau}) \\ \tilde{a}(t - \hat{\tau}) \end{pmatrix}^T dt \quad 5-4$$

Where T is the integration or averaging time. Combining the input signal $u_{PSK}(t)$ and the receiver trial estimates the result can be converted to

$$\mathbf{W} = \begin{pmatrix} w_{II} & w_{IQ} \\ w_{QI} & w_{QQ} \end{pmatrix} = \frac{1}{T} \int_0^T \begin{pmatrix} v_I(t) \\ v_Q(t) \end{pmatrix} \begin{pmatrix} a(t - \hat{\tau}) \\ \tilde{a}(t - \hat{\tau}) \end{pmatrix}^T dt \quad 5-5$$

where

$$\mathbf{v}(t) = \begin{pmatrix} v_I(t) \\ v_Q(t) \end{pmatrix} = \frac{\cos(\phi - \hat{\phi})}{\sin(\phi - \hat{\phi})} \times a(t - \tau) \times d \quad 5-6$$

The result of the integrals in Equation 5-5 can be written as follows.

$$\begin{aligned} w_{II} &\approx A \times \cos(\phi - \hat{\phi}) \times \Lambda(\hat{\tau} - \tau) \times d & 5-7 \\ w_{IQ} &\approx A \times \cos(\phi - \hat{\phi}) \times \sqrt{\Lambda}(\hat{\tau} - \tau) \times d \\ w_{QI} &\approx A \times \sin(\phi - \hat{\phi}) \times \Lambda(\hat{\tau} - \tau) \times d \\ w_{QQ} &\approx A \times \sin(\phi - \hat{\phi}) \times \sqrt{\Lambda}(\hat{\tau} - \tau) \times d \end{aligned}$$

The ' $\sqrt{\Lambda}$ ' represents the code tracking discriminator error signal, this is described fully in the Section 5.2 of this chapter. The symbol ' Λ ' represents the ideal PSK correlation function, which can be written

$$\begin{aligned} \Lambda(\hat{\tau} - \tau) &= \begin{cases} 1 - \frac{|\hat{\tau} - \tau|}{T_c} & \text{for } -T_c \leq (\hat{\tau} - \tau) \leq T_c \\ 0 & \text{otherwise} \end{cases} & 5-8 \\ &\approx \frac{1}{T} \int_0^T a(t - \tau) a(t - \hat{\tau}) dt \end{aligned}$$

The $\Lambda()$ function approximates the (almost) triangular correlation function of PSK PRN codes, ignoring cross correlation errors. This function peaks on $\hat{\tau} \rightarrow \tau$, with total width we define as $2 \times T_c$. This can be seen by inspecting the result w_{II} derived from Mathcad simulation and shown in Figure 5-3.

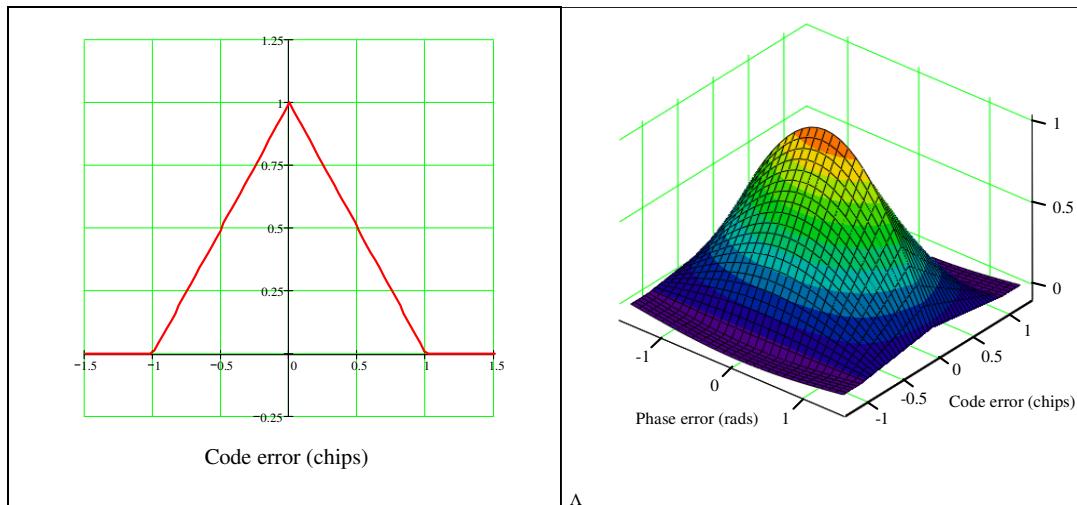


Figure 5-3, Correlation profile of w_{II} against code error (chips) and phase error (radians)

For PSK signals the result of w_{II} is a single correlation peak, however the correlation still has a phase dependency and may be inverted with the sign of the navigational data. At start-up the GNSS receiver must search for each signal with no knowledge of the phase of the received carrier. Phase independency for the PSK search correlation is achieved by adding the square of the w_{II} correlation combined with the square of the quadrature w_{QI} correlation. This forms an unambiguous peak for the search process, which is independent of phase error and the sign of the navigational data ($d^2 = 1$).

$$w_{SPSK} = w_{II}^2 + w_{QI}^2 = 2A^2\Lambda^2(\hat{\tau} - \tau) \quad 5.9$$

The correlation profile of w_{SPSK} is shown against code error and carrier phase error in Figure 5-4. It can be seen that the search correlation is independent of carrier phase error.

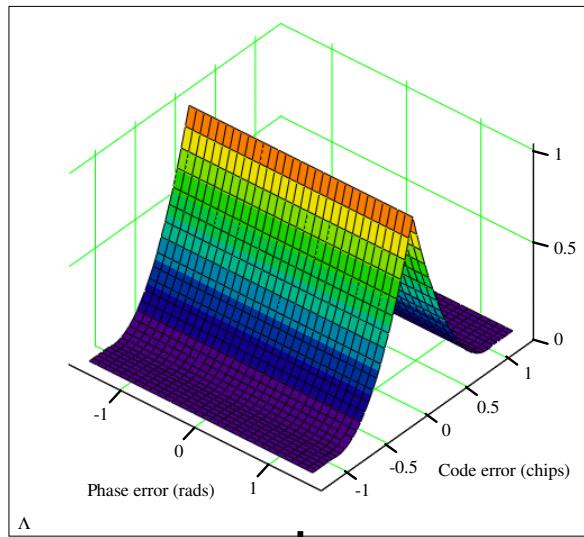


Figure 5-4, PSK search correlation w_{SPSK}

The search is a 2 dimensional process, locating the signal in time (code delay) and frequency. Traditionally, a serial search technique is used, holding a steady frequency while shifting through all possible code offsets, before moving to the next possible frequency (Figure 5-5). The frequency range the receiver is required to search across is strongly dependant on the dynamic environment the receiver is to operate in and the quality of the receiver clock. For a typical terrestrial receiver the frequency search

range can be up to ± 10 kHz, however for space receivers the range can expand up to ± 50 kHz [Unwin 1995].

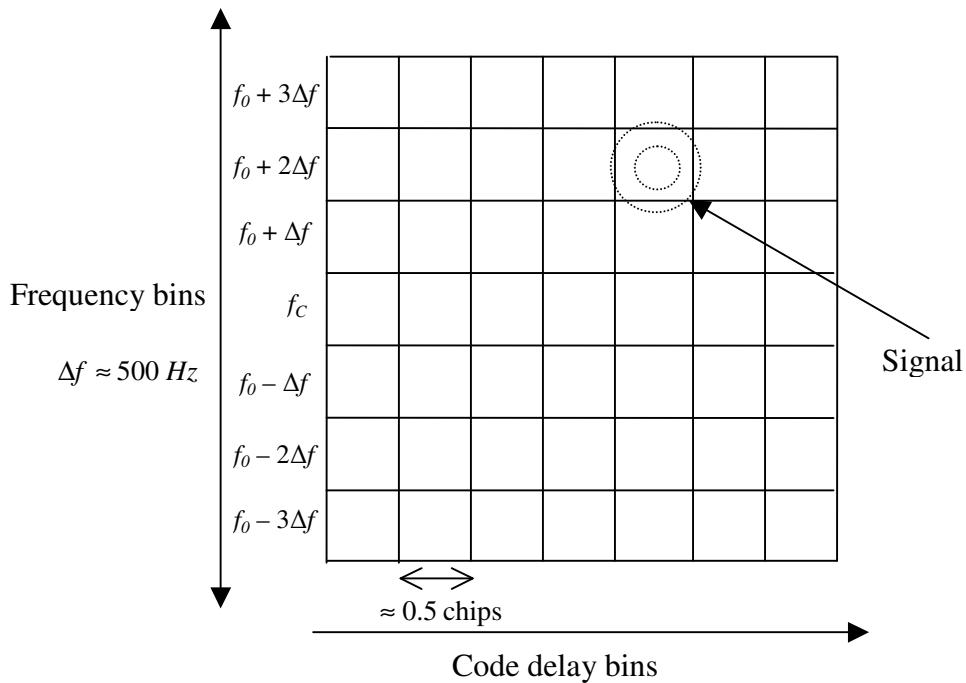


Figure 5-5, Serial GNSS signal search

Frequency is typically searched in bins of 500 Hz (for $T = 1\text{ms}$). The normalised correlation gain G_F , with frequency error Δf is given by [Mitel 1996]

$$G_F = \frac{\sin(\pi \times \Delta f \times T)}{(\pi \times \Delta f \times T)} \quad 5-10$$

where T is the integration period. The correlation gain is shown in Figure 5-6 for an integration time of 1msec. The minimum correlation gain for frequency bins of 500Hz is -4dB. Extending the integration period allows detection of weaker signals. However, the frequency bins are narrowed resulting in longer search times and potentially reductions in correlation gain due to changes in the Doppler during the correlation time.

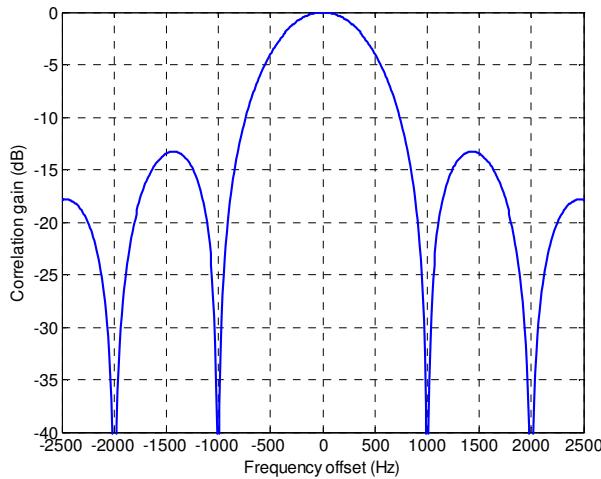


Figure 5-6, Correlation power loss with frequency offset

The code is typically searched in $\frac{1}{2}$ chip bins. Within the correlation interval $(\hat{\tau} - \tau \leq \pm T_c)$ the normalised correlation power G_τ , with code delay error, $\hat{\tau} - \tau$ is given by

$$G_\tau = \Lambda^2(\hat{\tau} - \tau) \quad \text{5-11}$$

For $\frac{1}{2}$ chip code bins the minimum correlation gain is -6dB. Narrower code and carrier bin width will result in more reliable signal detection. However, the search time will increase because there are now more bins to search through.

The serial search technique is inherently slow and may take a number of minutes to detect signal presence reliably. Modern receivers use search techniques based on Fast Fourier Transforms (FFT), which can detect the signal presence within a matter of milliseconds [Van Nee and Coenen 1991]. The basic principle of FFT signal detection is shown in Figure 5-7, first presented in [Kilvington 1986]. The received signal is mixed into real (in-phase) and imaginary (quadrature) components and its Fourier transform computed. The result is then conjugate multiplied by the Fourier transform of the code sequence. Multiplication of signals in the frequency domain is equivalent to correlating signals in the time domain. Therefore, the correlation across all code offsets can be computed by taking the inverse Fourier transform.

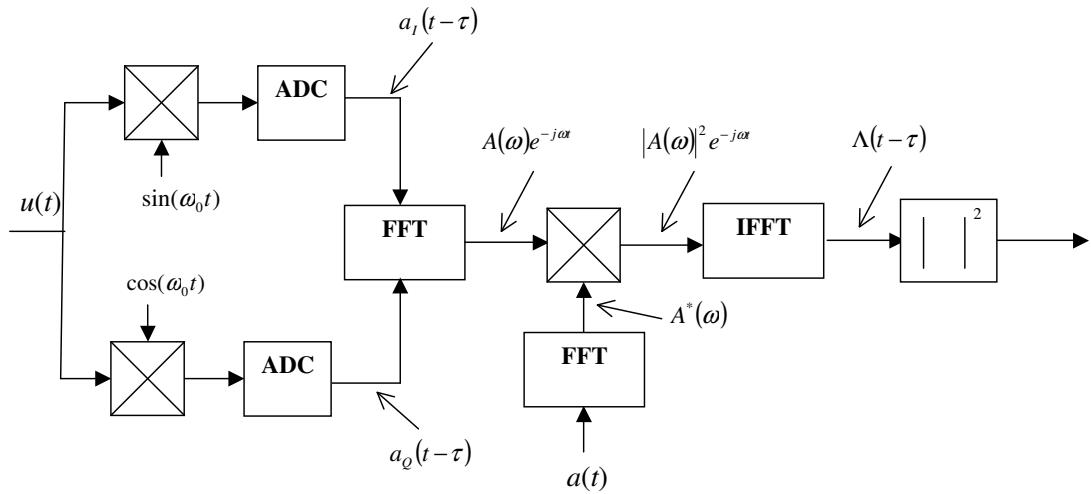


Figure 5-7, FFT signal detection principle

Figure 5-8 shows the FFT detection of a GPS C/A code signal. The result of a single FFT detection can deliver the equivalent to an entire serial search in a matter of milliseconds. It is shown in [Van Nee and Coenen 1991] that FFT detection can be up to 2000 times faster than the equivalent serial search technique. However, performing FFT detection in the receiver hardware imposes large processing overhead and often requires a dedicated FFT unit in the receiver design. More discussion of FFT detection for future GNSS signals is given in Chapter 10.

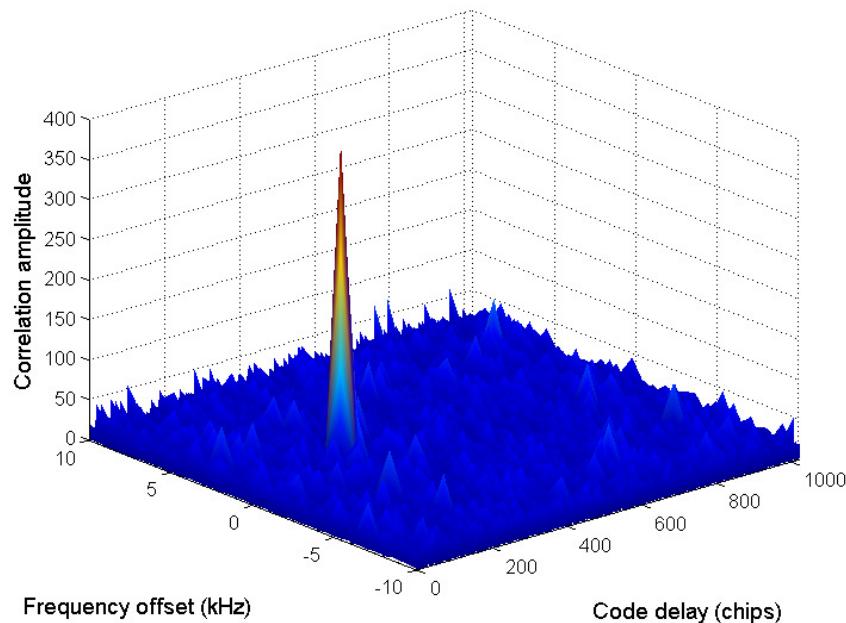


Figure 5-8, FFT of GPS C/A code signal

Whether using a serial search technique or FFT detection the correlation profile of the PSK signal is a single peak as given by Equation 5-9. A detection threshold must be set within the receiver software above which signal presence is declared. This may be based on a single search result, ‘*single dwell*’ or multiple search results, ‘*multiple dwells*’. Taking multiple dwells clearly increases the reliability of detection but also lengthens the signal search time. Raising the detection threshold reduces the risk of false alarm but also reduces the probability detecting the signal. The choice of detection threshold is strongly dependent on the receiver’s operating environment and application.

5.2 Tracking PSK signals

To achieve a reasonable estimate of the time delay of the received signal a PSK GNSS receiver must implement a carrier loop to maintain lock on the frequency and / or phase of the incoming carrier wave. Simultaneously, a code loop must also maintain lock on the PRN code sequence present in the received signal. This can only be achieved by adjusting the carrier phase estimate, $\hat{\phi}$ and the code phase estimate, $\hat{\tau}$ to track the incoming ϕ and τ respectively.

For the carrier loop a Frequency Locked Loop (FLL) or Phase Locked Loop (PLL) can be used from which we define an *incoherent* or *coherent* system respectively. A FLL delivers more robust tracking in highly dynamical environments and in very weak signal conditions [Kaplan and Hegarty 2006]. However, in order to enable precise delta pseudorange, integrated Doppler measurements and carrier phase positioning a GNSS receiver must track the phase of the incoming carrier. Hence, a coherent Phase Locked Loop (PLL) system is required.

The carrier phase error is commonly determined using a Costas decision-directed discriminator [Kaplan and Hegarty 2006] as follows.

$$e_{\phi} = w_{QI} \times \text{sgn}(w_{II}) \approx A \times \sin(\phi - \hat{\phi}) \times \text{sqc}(\phi - \hat{\phi}) \times \Lambda(\hat{\tau} - \tau) \quad 5-12$$

$\text{sqc}(\cdot)$ is a square wave cosine function, shown in Figure 5-9. Incorporating the sign correction by hard-limiting the w_{II} correlation in the discriminator allows the PLL to function with no knowledge of the navigational data state.

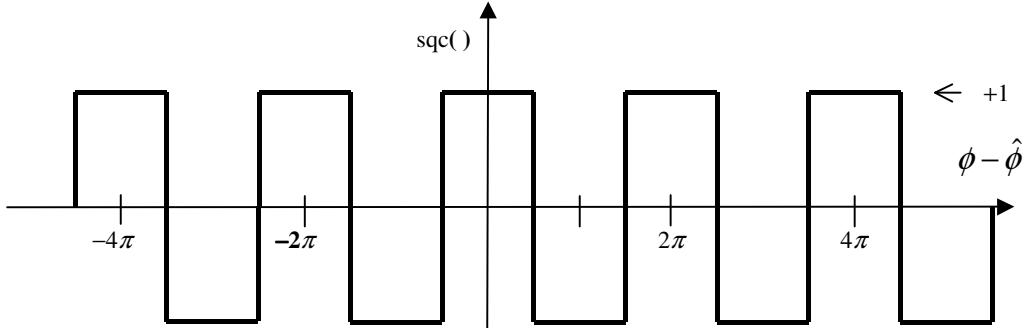


Figure 5-9, Square wave cosine function

It can be seen that e_ϕ tends to zero as $\sin(\phi - \hat{\phi})$ tends to zero, which occurs at integer n multiples of π radians as $\hat{\phi} \rightarrow \phi + n\pi$. This 180° ambiguity is caused sign correction in the discriminator but can be resolved by inspection of the incoming navigational data. The discriminator characteristic is shown in Figure 5-10.

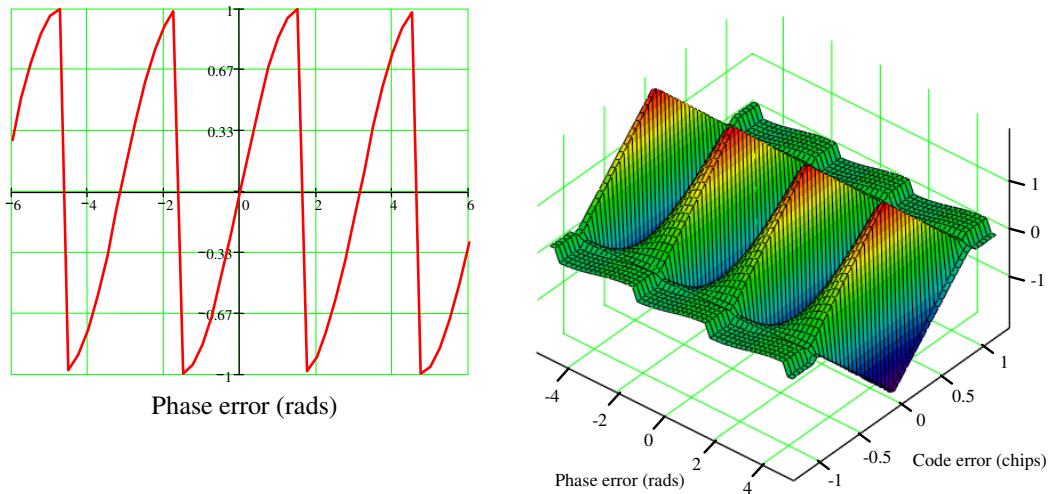


Figure 5-10, Costas PLL discriminator characteristic

The decision-directed discriminator is dependant on amplitude A , a number of other PLL discriminators can also be used, each with different dependencies and

computational loads. Table 5-1 shows the most commonly used PLL discriminators [Kaplan and Hegarty 2006], their error signals and dependencies.

Table 5-1, Costas PLL discriminators

Discriminator	Error signal	Dependency
Decision-corrected	$e_\phi = w_{QI} \times \text{sgn}(w_{II})$ $\approx A \times \sin(\phi - \hat{\phi}) \times \text{sqc}(\phi - \hat{\phi}) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A
Dot product	$e_\phi = w_{QI} \times w_{II}$ $\approx \frac{A^2}{2} \times \sin[2 \times (\phi - \hat{\phi})] \times \Lambda^2(\hat{\tau} - \tau)$	Slope proportional to A^2
Normalised	$e_\phi = w_{QI} / w_{II}$ $\approx \tan(\phi - \hat{\phi})$	Slope independent of amplitude
2 quadrant arc tangent	$e_\phi = \arctan(w_{QI} / w_{II})$ $\approx (\phi - \hat{\phi})$	Slope independent of amplitude

The PLL is generally updated using a second order loop as follows.

$$\begin{aligned} f_\phi &\leftarrow f_\phi + e_\phi \\ \hat{\phi} &\leftarrow \hat{\phi} + k_1 \times f_\phi + k_2 \times e_\phi \end{aligned} \quad \text{5-13}$$

f_ϕ is the integrated phase error and k_1 and k_2 are loop gains which can be adjusted by the designer.

An incoherent system holds frequency lock by maintaining a constant or near constant phase difference across the correlation interval. The rate of change of carrier phase can be determined by comparing w_{II} and w_{QI} with the correlation results from the next epoch w'_{II} and w'_{QI} . The frequency error can then be determined using the cross-product discriminator as follows.

$$e_\omega = w'_{QI} \times w_{II} - w'_{II} \times w_{QI} = A^2 \times \sin(\Delta\hat{\phi} - \Delta\phi) \times \Lambda^2(\hat{\tau} - \tau) \times d \times d' \quad \text{5-14}$$

The phase difference and estimated phase difference between epochs is

$$\begin{aligned}\Delta\phi &= \phi' - \phi \\ \Delta\hat{\phi} &= \hat{\phi}' - \hat{\phi}\end{aligned}\quad \text{5-15}$$

As e_ω tends to zero, $\Delta\hat{\phi} - \Delta\phi$ tends to zero. This discriminator only gives a true frequency error when no data transitions have occurred. FLL discriminators only perform well when short integration periods are used to restrict the number of data transitions affecting the error characteristic. Filtering of the discriminator output is also required to reduce the impact of the data transitions. It is common to use a second order loop to update the carrier phase estimate by the frequency error as follows.

$$\begin{aligned}e_\phi &\leftarrow e_\phi + e_\omega \\ f_\phi &\leftarrow f_\phi + e_\phi \\ \hat{\phi} &\leftarrow \hat{\phi} + k_1 \times f_\phi + k_2 \times e_\phi\end{aligned}\quad \text{5-16}$$

e_ϕ is the estimated phase error derived by the integrating frequency error e_ω , k_1 and k_2 are loop gains which can be adjusted by the designer. The cross-product discriminator has a dependence on A^2 , a number of other FLL discriminators can also be used, each with different dependencies and computational loads. Table 5-2 shows the most commonly used FLL discriminators, their error signals and dependencies.

Table 5-2, FLL discriminators

Discriminator	Error signal	Dependency
Cross-product	$\begin{aligned}e_\omega &= w'_{QI} \times w_{II} - w'_{II} \times w_{QI} \\ &\approx A^2 \times \sin(\Delta\hat{\phi} - \Delta\phi) \times \Lambda^2 (\hat{\tau} - \tau)\end{aligned}$	Slope proportional to A^2
4 quadrant arc tangent (cross-product)	$\begin{aligned}e_\omega &= \arctan 2 \left(\frac{w'_{QI} \times w_{II} - w'_{II} \times w_{QI}}{w'_{II} \times w_{II} + w'_{QI} \times w_{QI}} \right) \\ &\approx (\Delta\hat{\phi} - \Delta\phi)\end{aligned}$	Slope independent of amplitude
4 quadrant arc tangent (decision-corrected)	$\begin{aligned}e_\omega &= \arctan 2 \left(\frac{w'_{QI} \times \text{sgn}(w_{II}) - w'_{II} \times \text{sgn}(w_{QI})}{w'_{II} \times \text{sgn}(w_{II}) + w'_{QI} \times \text{sgn}(w_{QI})} \right) \\ &\approx (\Delta\hat{\phi} - \Delta\phi)\end{aligned}$	Slope independent of amplitude

Common practice is for the PRN code sequence to be acquired and tracked using a Delay Locked Loop (DLL). This can be achieved when implementing either incoherent FLL or coherent PLL carrier tracking. However, different correlations and discriminators are required for each system. A common discriminator suitable for tracking with both coherent and incoherent systems is the dot-product discriminator, formed as follows.

$$e_\tau = w_{IQ} \times w_{II} + w_{QI} \times w_{QQ} = A^2 \times \sqrt{\Lambda(\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau)} \quad 5-17$$

The ' $\sqrt{\Lambda}$ ' symbol represents the code tracking error equivalent to subtracting separate early and late correlations, written as follows.

$$\sqrt{\Lambda(\hat{\tau} - \tau)} = \Lambda\left(\hat{\tau} - \tau - \frac{T_{DC}}{2}\right) - \Lambda\left(\hat{\tau} - \tau + \frac{T_{DC}}{2}\right) \quad 5-18$$

The dot-product discriminator characteristic is shown in Figure 5-11. It can be seen that this discriminator has no phase dependence and is therefore suitable for an incoherent system.

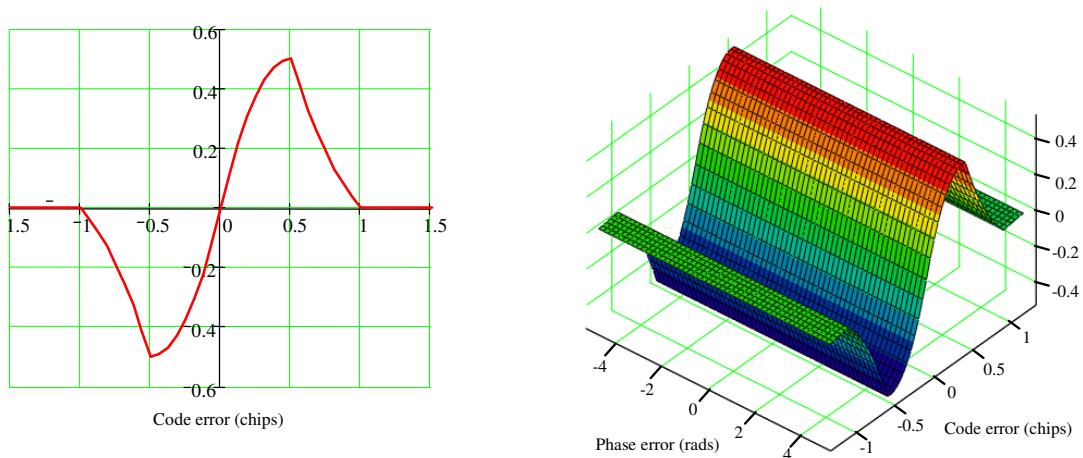


Figure 5-11, Dot product discriminator characteristic

It is common to use a first order loop to update the code phase estimate. This is only made possible by the use of the Doppler aiding from the carrier tracking loop. The carrier loop is generally a second or third order loop, which accurately tracks the

dynamics of the system. Therefore, the system dynamics can be effectively removed by applying the Doppler estimated by the carrier loop to the DLL with sufficient scaling. The first order code loop update equation with carrier Doppler aiding can be written as follows.

$$\hat{\tau} = \hat{\tau} + k_\phi \times f_\phi + k_\tau \times e_\tau \quad \text{5-19}$$

k_ω and k_ϕ are constants calculated to provide the necessary open loop correction of Doppler shift appropriately scaled down to the code rate and k_τ is a loop gain which can be adjusted by the designer. The dot-product discriminator is dependant on amplitude A^2 , a number of other DLL discriminators can also be used, each with different dependencies and computational loads. A number of discriminators used to remove the amplitude dependence require generation of signals individually multiplied by early and late replica code sequences as follows.

$$\begin{aligned} v_{IE}(t) &= v_I(t) \times a \left(t - \hat{\tau} \pm \frac{T_{DC}}{2} \right) \\ v_{IL}(t) &= v_I(t) \times a \left(t - \hat{\tau} \pm \frac{T_{DC}}{2} \right) \\ v_{QE}(t) &= v_Q(t) \times a \left(t - \hat{\tau} \pm \frac{T_{DC}}{2} \right) \\ v_{QL}(t) &= v_Q(t) \times a \left(t - \hat{\tau} \pm \frac{T_{DC}}{2} \right) \end{aligned} \quad \text{5-20}$$

The resulting early and late correlations are written as

$$\begin{aligned} w_{IE} &\approx A \times \cos(\phi - \hat{\phi}) \times \Lambda \left(\hat{\tau} \mp \frac{T_{DC}}{2} - \tau \right) \\ w_{IL} &\\ w_{QE} &\approx A \times \sin(\phi - \hat{\phi}) \times \Lambda \left(\hat{\tau} \mp \frac{T_{DC}}{2} - \tau \right) \\ w_{QL} & \end{aligned} \quad \text{5-21}$$

Table 5-3 shows the most commonly used DLL discriminators, their error signals and dependencies. The choice of discriminator must be made depending on the computational capability of the receiver and the signal environments in which it will operate. Removing the sensitivity of the receiver to signal amplitude provides the most robust solution but maximises the microprocessor loading.

Table 5-3, DLL discriminators

Discriminator	Error signal	Dependency
Coherent		
Dot product	$e_\tau = w_{IQ} \times w_{II}$ $\approx A^2 \times \cos^2(\phi - \hat{\phi}) \times V^\Lambda (\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A^2
Decision-directed	$e_\tau = w_{IQ} \times \text{sgn}(w_{II})$ $\approx A \times \cos(\phi - \hat{\phi}) \times V^\Lambda (\hat{\tau} - \tau)$	Slope proportional to A
Incoherent		
Dot product	$e_\tau = w_{IQ} \times w_{II} + w_{QI} \times w_{QQ}$ $\approx A^2 \times V^\Lambda (\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A^2
Decision-directed	$e_\tau = w_{IQ} \times \text{sgn}(w_{II}) + w_{QQ} \times \text{sgn}(w_{QI})$ $\approx A \times (\left \cos(\phi - \hat{\phi}) \right + \left \sin(\phi - \hat{\phi}) \right) \times V^\Lambda (\hat{\tau} - \tau)$	Slope proportional to A
Power	$e_\tau = w_{IE}^2 + w_{QE}^2 - w_{IL}^2 - w_{QL}^2$ $\approx A^2 \times V^\Lambda (\hat{\tau} - \tau)$	Slope proportional to A^2
Normalised envelope	$e_\tau = \frac{\sqrt{w_{IE}^2 + w_{QE}^2} - \sqrt{w_{IL}^2 + w_{QL}^2}}{\sqrt{w_{IE}^2 + w_{QE}^2} + \sqrt{w_{IL}^2 + w_{QL}^2}}$ $\approx \frac{V^\Lambda (\hat{\tau} - \tau)}{\left(\Lambda \left(\hat{\tau} - \frac{T_{DC}}{2} - \tau \right) + \Lambda \left(\hat{\tau} + \frac{T_{DC}}{2} - \tau \right) \right)}$	Slope independent of amplitude

Although listing discriminators may seem an exhaustive it is essential that receiver designers account for incoming signal amplitude variation in the loop designs. These tables provide designers with essential information for providing robust tracking loop design. Equivalent tables are given for BOC signals tracking in Chapter 6. Appendix D shows practical examples of how these considerations can be critical to reliable receiver operation.

5.3 Searching for BOC signals

A BOC signal is a square wave sub-carrier modulation of the coding sequence and can be written

$$b(t) = a(t) \times s(t)$$

where $s(t)$ is the sub-carrier, which can have any phasing relative to the code sequence, although sine and cosine are the most common. An integer or integer and a half number of cycles are allowed in each chip interval. The received BOC signal can be modelled as follows.

$$u_{BOC}(t) = A \times \cos(\omega_0 t + \phi) \times b(t - \tau) \times d \quad 5-23$$

For simplicity we consider receiving only a single noiseless BOC signal with no other signal in phase quadrature. The BOC correlator architecture when employing correlation techniques used for conventional PSK receivers is shown in Figure 5-12.

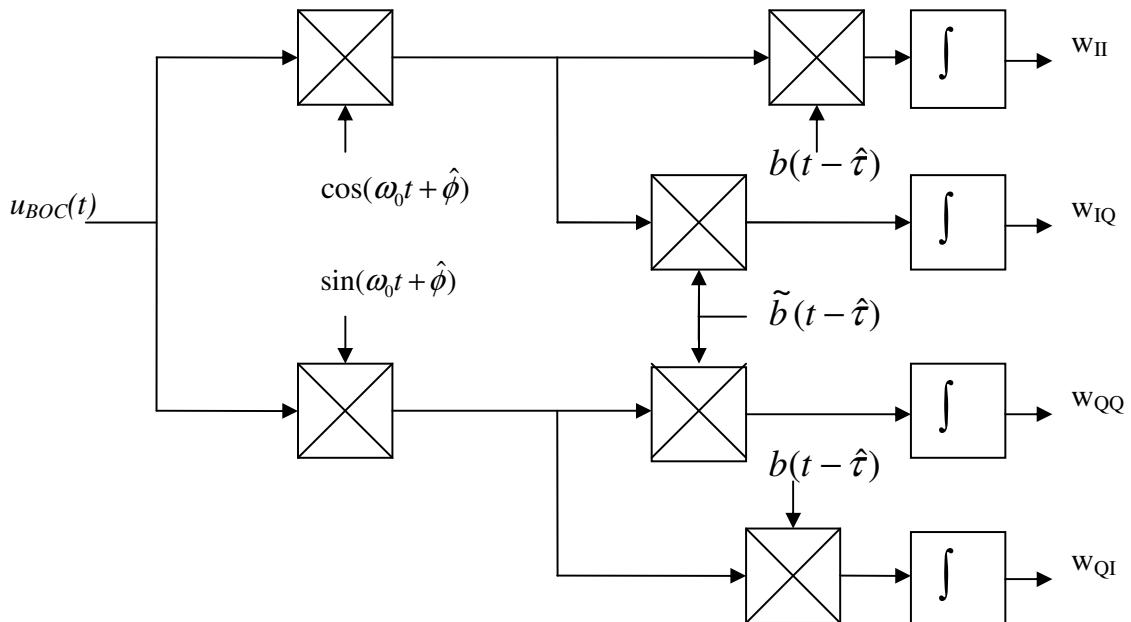


Figure 5-12, BOC correlator using conventional PSK architecture

The correlation results can be written compactly as

$$\mathbf{W} = \begin{pmatrix} w_{II} & w_{IQ} \\ w_{QI} & w_{QQ} \end{pmatrix} = \frac{1}{T} \int_0^T u_{BOC}(t) \begin{pmatrix} \cos(\omega_0 t + \hat{\phi}) \\ \sin(\omega_0 t + \hat{\phi}) \end{pmatrix} \begin{pmatrix} b(t - \hat{\tau}) \\ \tilde{b}(t - \hat{\tau}) \end{pmatrix}^T dt \quad 5-24$$

where the orthogonal BOC code sequence is defined as

$$\tilde{b}(t - \hat{\tau}) = b\left(t - \hat{\tau} + \frac{T_{DC}}{2}\right) - b\left(t - \hat{\tau} - \frac{T_{DC}}{2}\right) \quad 5-25$$

The result of the integrals in Equation 5-24 can be written as follows.

$$\begin{aligned} w_{II} &\approx A \times \cos(\phi - \hat{\phi}) \times \mathcal{W}(\hat{\tau} - \tau) \times d \\ w_{IQ} &\approx A \times \cos(\phi - \hat{\phi}) \times \mathcal{W}(\hat{\tau} - \tau) \times d \\ w_{QI} &\approx A \times \sin(\phi - \hat{\phi}) \times \mathcal{W}(\hat{\tau} - \tau) \times d \\ w_{QQ} &\approx A \times \sin(\phi - \hat{\phi}) \times \mathcal{W}(\hat{\tau} - \tau) \times d \end{aligned} \quad 5-26$$

The ' \mathcal{W} ' symbol represents the multi-peaked BOC correlation function which can be written as

$$\mathcal{W}(\hat{\tau} - \tau) = \text{trc}(\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau) \quad 5-27$$

where the $\text{trc}()$ function is a continuous triangular cosine waveform where $\text{trc}(\hat{\tau} - \tau) \rightarrow \pm 1$ as $\hat{\tau} \rightarrow \tau + n \times T_s$, shown in Figure 5-13.

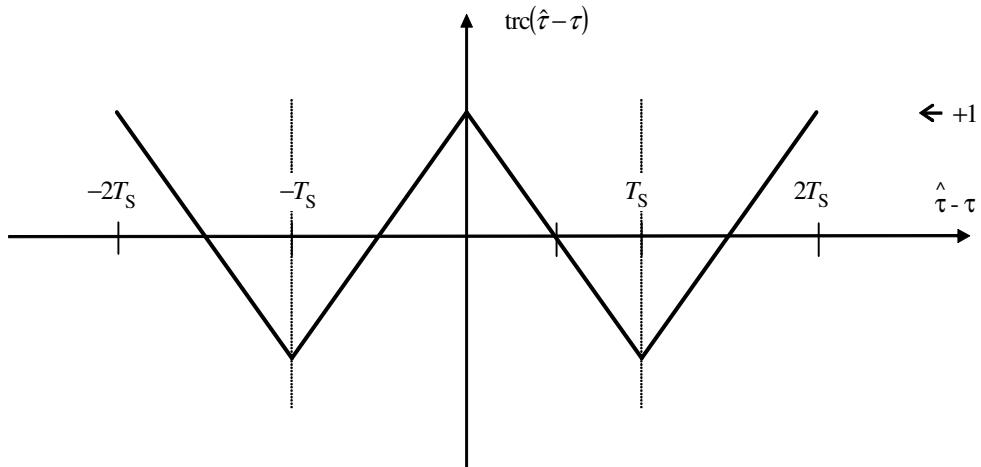


Figure 5-13, Triangular cosine function

The ' \mathcal{W} ' symbol represents the BOC discriminator function, equivalent to subtracting separate early and late correlations, written as follows.

$$\mathbb{W}(\hat{\tau} - \tau) = \mathbb{W}\left(\hat{\tau} - \tau - \frac{T_{DC}}{2}\right) - \mathbb{W}\left(\hat{\tau} - \tau + \frac{T_{DC}}{2}\right) \quad 5-28$$

The w_H correlation for a BOC($2 \times f_C, f_C$) modulated signal is shown in Figure 5-14. In order to locate the BOC signal the search process must remove the dependency on carrier phase error, this can be accomplished using the conventional PSK search correlation given in Equation 5-9. However, the multiple peaks and troughs of the BOC correlation function introduce nulls across the correlation interval, which reduce the probability of detection. For PSK $\frac{1}{2}$ chip code search bins results in a minimum correlation gain of -6dB from the peak gain. For BOC system a minimum correlation gain of -6dB is only achieved with search bins of $\frac{1}{2}$ a sub-chip.

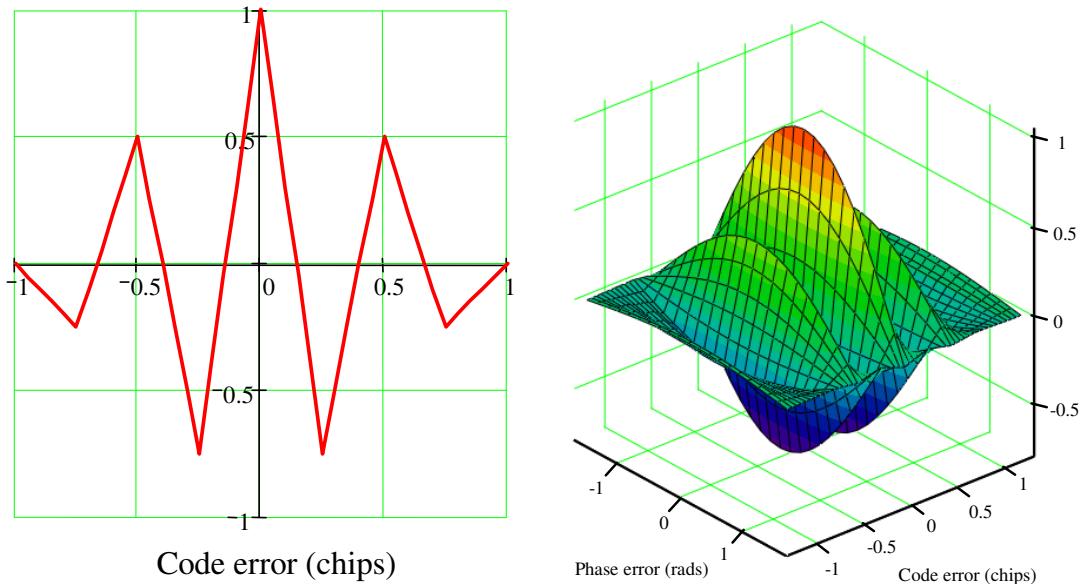


Figure 5-14, w_H for BOC($2 \times f_C, f_C$) against code error (chips) and carrier phase error(rads)

Implementing a standard serial search technique BOC modulation increases the search time compared to PSK by a factor of twice the ratio of sub-carrier frequency to code rate (a factor of 4 for BOC($2 \times f_C, f_C$), or a factor of 12 for BOC($6 \times f_C, f_C$)). When FFT acquisition is employed BOC modulation has an equivalent impact on the number of points required. Again compared to PSK the number of FFT points required to achieve equivalent correlation loss increases by a factor of twice the ratio of sub-

carrier frequency to code rate. Along with increasing code lengths and sampling rates this poses an unacceptable overhead on the receiver hardware. Therefore, for reliable fast acquisition of BOC signals it is necessary to form a single peak across the correlation interval for the search process.

Creating a single correlation peak for BOC search requires additional receiver hardware. To achieve this we consider two different approaches proposed in the literature, each with different receiver hardware requirements.

The first technique ‘single sideband (SSB) acquisition’ was first proposed by Betz in [Betz 1999]. This method treats each of the two BOC sidebands as separate PSK signals. This requires independent filtering of each sideband. In addition, each sideband must have a separate carrier demodulation stage, requiring an additional local oscillator to be implemented in the receiver’s correlator architecture. Figure 5-15 shows the receiver hardware required for BOC acquisition using the SSB technique. The BOC sidebands can be separated using analogue filters. However, either a multiplexed or additional ADC stage will be required. Using digital filters imposes considerable demands on the receiver’s correlator resources.

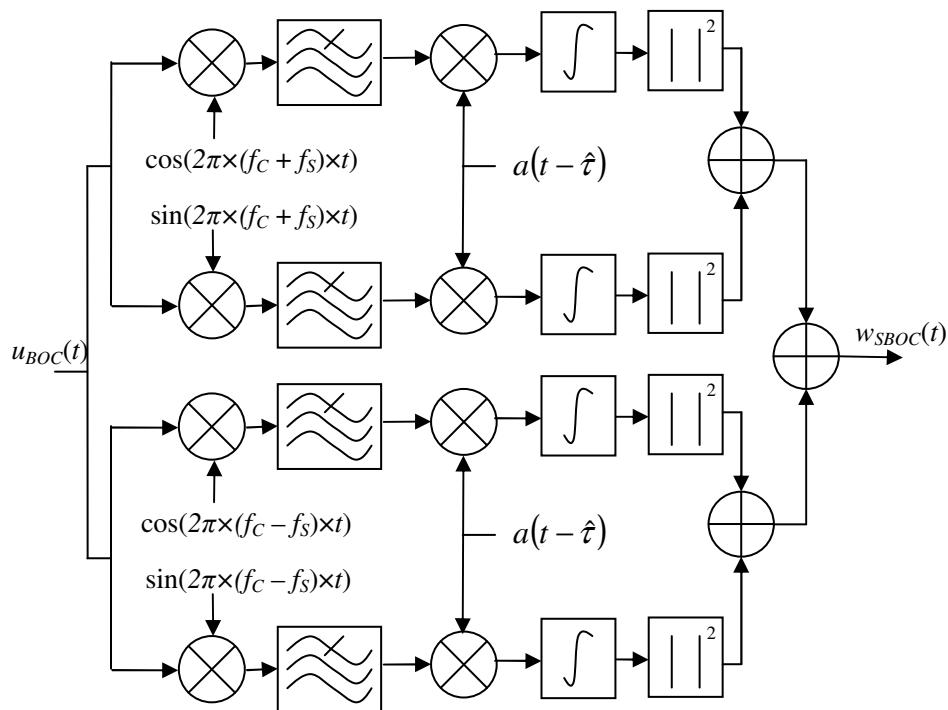


Figure 5-15, Single sideband search of BOC modulated signals

The result of a SSB search is a unambiguous PSK correlation peak as shown in Figure 5-4. If only one sideband is tracked, a 3dB or greater reduction in signal power is inevitable. It has been shown [Martin *et al* 2003] that the signal power loss can be compensated for by applying the single sideband technique to each side-lobe and combining non-coherently. This technique can easily be implemented to BOC signals which are well separated from the centre frequency, but would require an extremely sharp filter roll-off (Nyquist filtering) for narrowly spaced signals, such as $\text{BOC}(f_c, f_c)$. Therefore, the SSB technique is only suitable for BOC signals whose sub-carrier frequency is greater than the code rate.

The second approach to providing a single BOC search is to synthesise an unambiguous search function by using quadrature or orthogonal BOC correlations. This search technique first proposed by Ward in [Ward 2003] and subsequently has been coined the ‘sub-carrier cancellation’ (SCC) technique [Heiries *et al* 2004]. We define an orthogonal BOC subcarrier, $\tilde{s}(\cdot)$. If $s(\cdot)$ is a sine sub-carrier then $\tilde{s}(\cdot)$ is a cosine waveform. If $s(\cdot)$ is a cosine sub-carrier then $\tilde{s}(\cdot)$ is a sine waveform. Figure 5-16 shows the correlator structure required for using the SCC technique for BOC search.

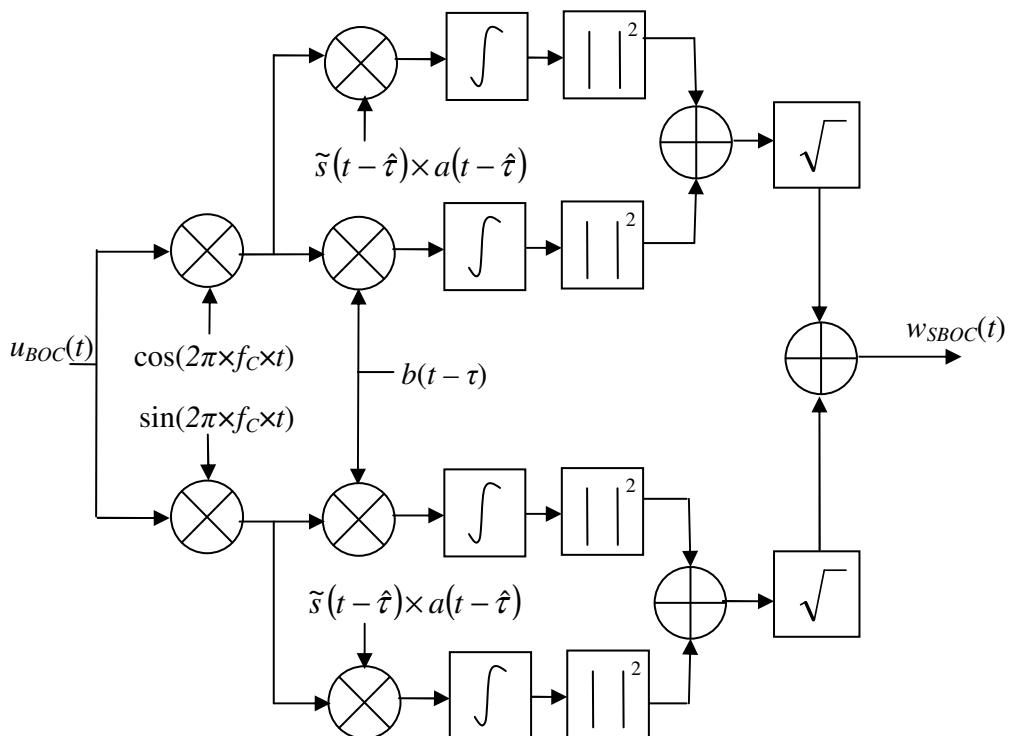


Figure 5-16, Sub-carrier cancellation BOC search technique

The correlations required for the SSC technique can be written as follows.

$$\begin{aligned}
 w_{III} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \cos(\omega_0 t + \hat{\phi}) \times b(t - \hat{\tau}) dt \\
 &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\
 w_{IQI} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \cos(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}) \times a(t - \hat{\tau}) dt \\
 &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trs}(\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\
 w_{QII} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \sin(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}) \times a(t - \hat{\tau}) dt \\
 &\approx A \times \sin(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\
 w_{QOI} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \sin(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}) \times a(t - \hat{\tau}) dt \\
 &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trs}(\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau) \times d
 \end{aligned} \tag{5-29}$$

The $\text{trs}(\cdot)$ function is a continuous triangular sine waveform where $\text{trs}(\hat{\tau} - \tau) \rightarrow 0$ as $\hat{\tau} \rightarrow \tau + n \times T_s$, shown in Figure 5-17.

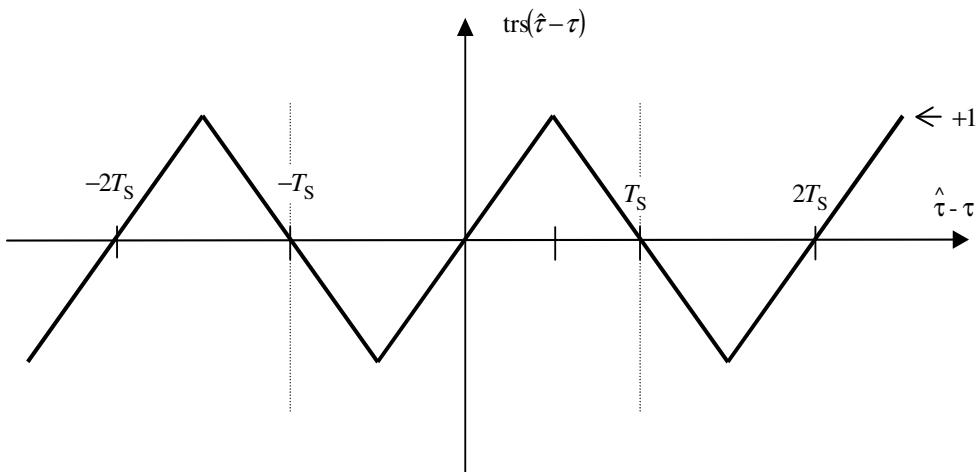


Figure 5-17, Triangular sine function

The first subscript denotes mixing with an in-phase (I) or quadrature (Q) carrier replica, the second subscript denotes mixing with an in-phase (I) or quadrature (Q) sub-carrier replica and the third subscript denotes mixing with in-phase or quadrature

(orthogonal) code replica. The BOC search correlation using the SCC technique can then be written as follows.

$$w_{SBOC} = \sqrt{w_{III}^2 + w_{QII}^2} + \sqrt{w_{IQI}^2 + w_{QQI}^2} \quad 5-30$$

The resulting SCC BOC search correlation is shown in Figure 5-18 for BOC($2 \times f_c, f_c$) signal.

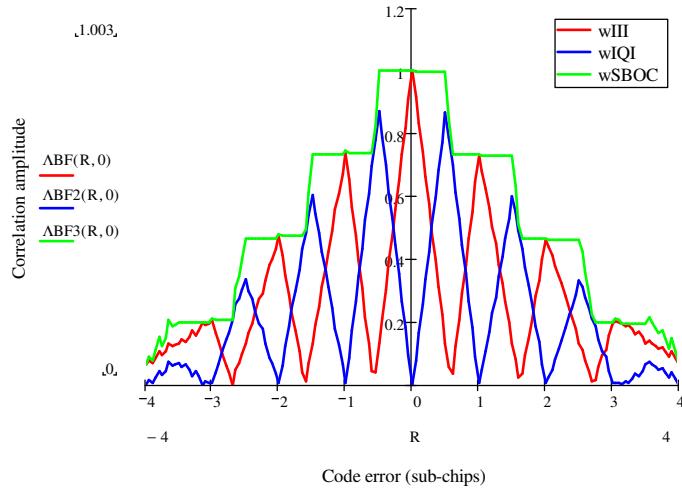


Figure 5-18, Magnitude envelopes of the w_{III} , w_{IQI} and w_{SBOC} correlations for a BOC($2 \times f_c, f_c$) signal

A comparison between the PSK search correlation and equivalent BOC search correlation is shown in Figure 5-19. The SCC technique creates a stepped correlation function which adequately approximates a single correlation peak. Including the quadrature carrier correlations w_{QII} and w_{QQI} removes the phase dependency of the search correlation, allowing location with only a coarse frequency lock. Extensive analysis and comparison of SSB and SCC search techniques is given via Monte-Carlo simulations in [Heiries *et al* 2004]. The SCC technique is shown to deliver equivalent performance to SSB search across a range of carrier to noise densities (22 to 32 dB-Hz).

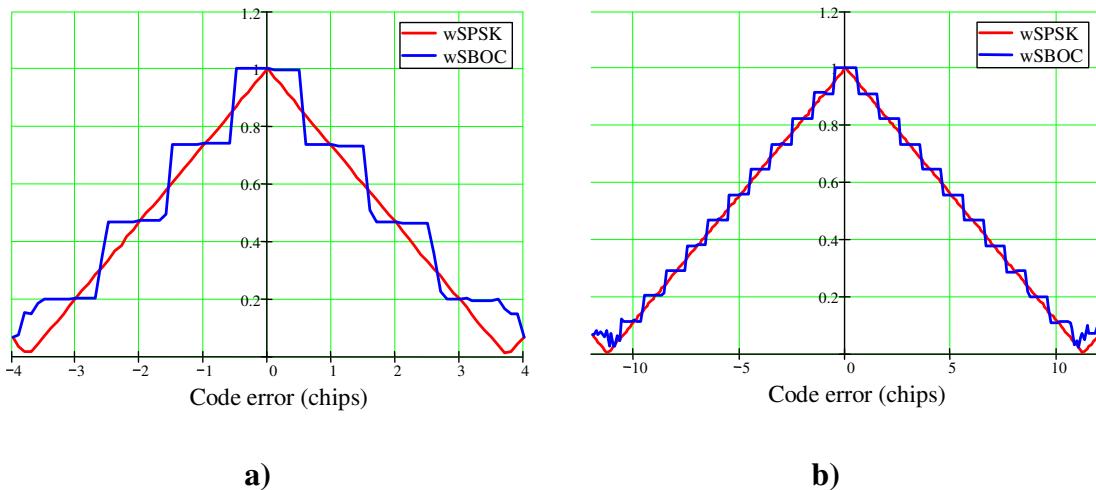


Figure 5-19, Comparison of PSK and BOC search correlations using the SCC search technique:
a) BOC($2 \times f_c, f_c$) b) BOC($6 \times f_c, f_c$)

The hardware requirements of the SSB and SCC techniques over conventional PSK architectures are shown in Table 5-4. Clearly the SSB technique requires considerably more receiver architecture than the SCC technique. This is due the necessity to isolate individual BOC sidebands. If analogue filters are implemented with the SSB technique a multiplexed or additional ADC stage will also be required. Using digital filters imposes considerable demands on the receiver's correlator resources.

Isolating individual sidebands provides no performance improvement and requires additional hardware requirements when compared to the SCC technique. The SSB technique is also incompatible with BOC tracking schemes providing precise timing location (detailed discussion in the following section). Therefore, SSB is only a feasible technique for low performance receivers with small front-end bandwidths, receiving only a single BOC sideband.

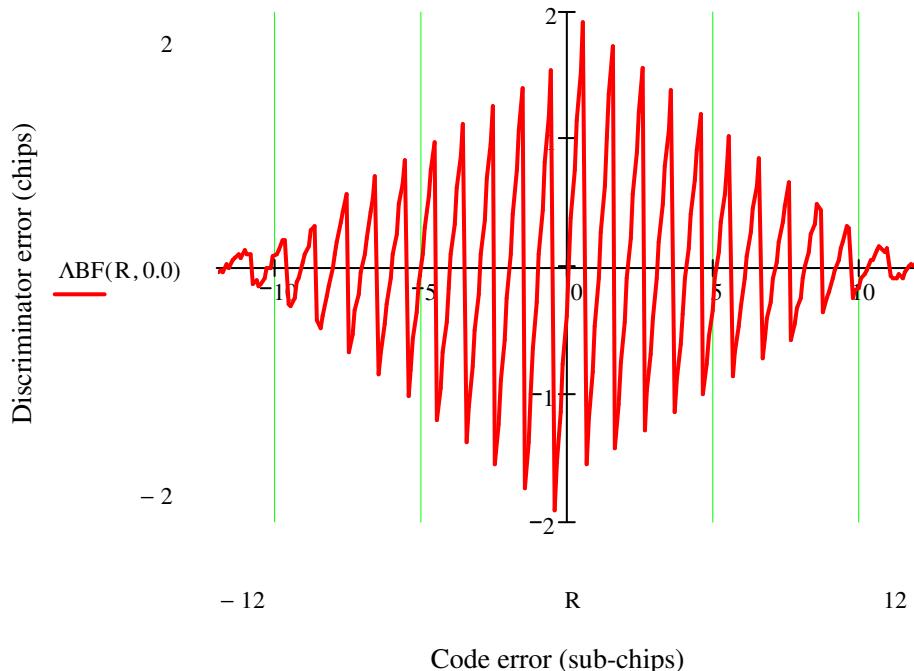
The SCC search technique provides correlator architecture compatible with precise BOC tracking schemes including the double-estimation BOC tracking loop (see chapter 6) developed during this research. Demonstrations of receivers using the SCC search technique are given in chapter 8 and chapter 10.

Table 5-4, Hardware requirements of BOC search techniques

Receiver type	Multipliers	Integrators	Local oscillators	Low pass filters
PSK	2×Carrier, 2×Code	2	1×Carrier, 1×Code	0
SSC	2×Carrier, 4×Code	4	1×Carrier, 1×Code	0
SSB	4×Carrier, 4×Code	4	2×Carrier, 1×Code	4

5.4 Tracking BOC signals

The standard BOC early minus late discriminator curve contains multiple zero crossings only one of which corresponds to the correct timing location (Figure 5-20). A GNSS BOC receiver aims to achieve and maintain lock on the incoming signal at the correct timing location. In order to do so the receiver must action an algorithm or mitigation technique to achieve valid timing information, effectively removing the influence of the secondary peaks in the BOC correlation. Ideally, the receiver will achieve this with no loss of tracking sensitivity.

**Figure 5-20, BOC($6 \times f_c, f_c$) discriminator curve**

Here we consider three standard approaches for solving the ambiguity in tracking BOC signals. *Single sideband* (SSB) tracking, *multiple gate delay* (MGD)

discriminators and the *bump-jumping* algorithm (BJ). Firstly we will compare the relative performance of each approach and then assess the impact of each to the receiver hardware.

5.4.1 BOC tracking using a single sideband

The first approach is to use the SSB technique described in the previous section. Treating each BOC sideband as a separate PSK signal creates an unambiguous PSK correlation peak ' Λ '. Then, correlating early and late replica signals (Figure 5-21) an unambiguous discriminator curve ' $\sqrt{\Lambda}$ ' can be formed using the standard PSK discriminators (Table 5-3).

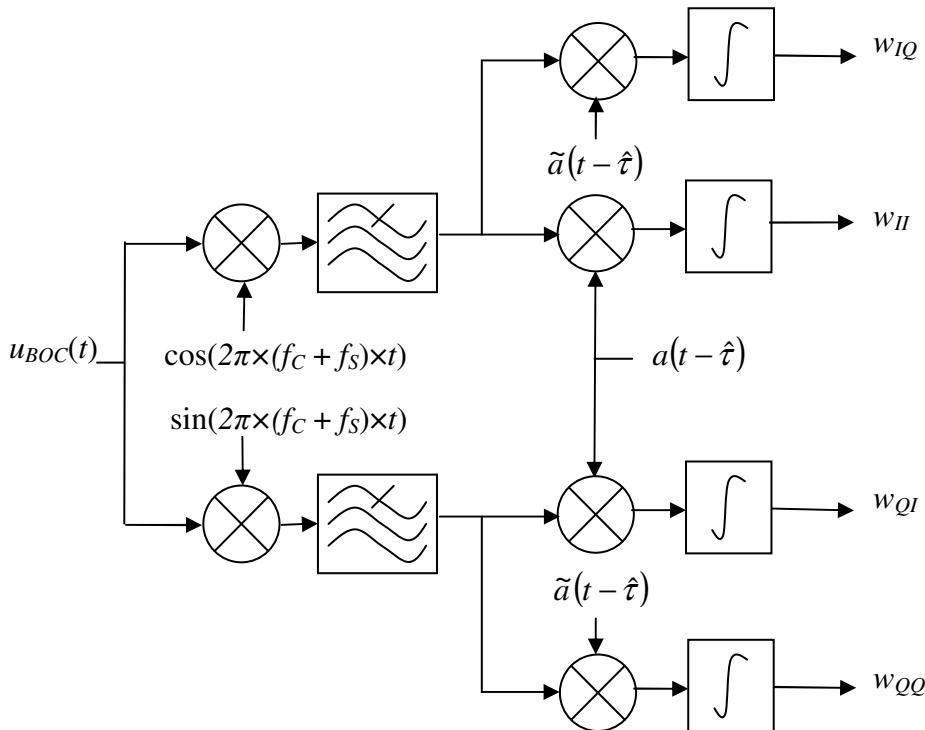


Figure 5-21, Single-sideband BOC tracking

This approach provides a robust solution. However, the receivers r.m.s. timing jitter is now dependant on the underlying PSK chipping rate and not the subcarrier rate. This degrades the receivers timing sensitivity by a factor of $4f_s/f_c$ [Bello and Fante 2005]. Therefore, this approach is only suitable for low precision receivers.

5.4.2 BOC tracking with multiple gate discriminators

The second approach is to synthesise an unambiguous discriminator curve by using a combination of multiple correlator channels. This approach, first proposed in [Fante 2004] and commonly termed the Multiple Gate Delay (MGD) discriminator. This technique proposes the use of K early and K late signals forming the following correlations.

$$\mathbf{W} = \begin{pmatrix} \mathbf{w}_{Ip}^{(E)} & \mathbf{w}_{Ip}^{(L)} \\ \mathbf{w}_{Qp}^{(E)} & \mathbf{w}_{Qp}^{(L)} \end{pmatrix} = \frac{1}{T} \int_0^T u_{BOC}(t) \begin{bmatrix} \cos(\omega_0 t + \hat{\phi}) \\ \sin(\omega_0 t + \hat{\phi}) \end{bmatrix} \begin{bmatrix} \mathbf{b}_E(t) \\ \mathbf{b}_L(t) \end{bmatrix}^T dt \quad 5-31$$

Where

$$\begin{aligned} \mathbf{b}_E(t) &= b \left(t - \hat{\tau} + \left(p - \frac{1}{2} \right) \times T_{DC} \right) \\ \mathbf{b}_L(t) &= b \left(t - \hat{\tau} - \left(p - \frac{1}{2} \right) \times T_{DC} \right) \end{aligned} \quad 5-32$$

T_{DC} is the early to late spacing and p is a integer count from 1 to K. The resulting correlations can be written as follows.

$$\begin{aligned} \mathbf{w}_{Ip}^{(E)} &\approx A \times \cos(\hat{\phi} - \phi) \times \mathbb{M} \left(\hat{\tau} - \tau - \left(p - \frac{1}{2} \right) \times T_{DC} \right) \times d \\ \mathbf{w}_{Ip}^{(L)} &\approx A \times \cos(\hat{\phi} - \phi) \times \mathbb{M} \left(\hat{\tau} - \tau + \left(p - \frac{1}{2} \right) \times T_{DC} \right) \times d \\ \mathbf{w}_{Qp}^{(E)} &\approx A \times \sin(\hat{\phi} - \phi) \times \mathbb{M} \left(\hat{\tau} - \tau - \left(p - \frac{1}{2} \right) \times T_{DC} \right) \times d \\ \mathbf{w}_{Qp}^{(L)} &\approx A \times \sin(\hat{\phi} - \phi) \times \mathbb{M} \left(\hat{\tau} - \tau + \left(p - \frac{1}{2} \right) \times T_{DC} \right) \times d \end{aligned} \quad 5-33$$

A vector of coefficients can then used to weight the influence of each of early and late correlations in an attempt to shape an unambiguous BOC discriminator. The

composite MGD discriminator is formed using of the non-coherent early-late power discriminator whose error function can be written as

$$e_\tau(\tau) = \sum_{p=1}^K c_p \times \left(\mathbf{w}_{Ip}^{(E)2} + \mathbf{w}_{Qp}^{(E)2} - \mathbf{w}_{Qp}^{(L)2} - \mathbf{w}_{Ip}^{(L)2} \right) \quad 5-34$$

$$e_\tau(\tau) \approx \sum_{p=1}^K c_p \times \left(\mathbb{W} \left[\tau - \left(p - \frac{1}{2} \right) \times T_{DC} \right]^2 - \mathbb{W} \left[\tau + \left(p - \frac{1}{2} \right) \times T_{DC} \right]^2 \right)$$

where c_p is the coefficient vector used to form the shape of the discriminator. Different combinations of coefficients are compared in [Fante 2004] to determine the best possible discriminator synthesis. Two classes of synthesised discriminators are defined, *smooth* and *bumpy*. *smooth* discriminators synthesise a discriminator approaching a monotonic error function, which provides a single shallow zero crossing. *bumpy* discriminators synthesise a single steep zero crossing with many undulations across the discriminator characteristic. Assuming a BOC($2 \times f_C, f_C$) signal and using four early-late discriminator combinations ($K = 4$) the use of coefficients [1 1.25 1.5 1.75] and $T_{DC} = 0.525 \times T_s$ creates a smooth discriminator, the use of coefficients [1 1.125 1.25 1.375] and $T_{DC} = 0.2 \times T_s$ creates a bumpy discriminator.

The composite smooth and bumpy discriminator curves are shown in Figure 5-22. Clearly the smooth discriminator more closely reflects the shape of a PSK ' \wedge ' discriminator providing robust acquisition of the correct timing location. The bumpy discriminator has a number of nulls in the envelope which will slow down the acquisition process and potentially cause false-lock states. It is argued that thermal noise will prevent false-lock occurring as the code error polarity is true either side of each null. Also, it is feasible to envisage a scheme which may acquire with a smooth envelope and transition to the bumpy discriminator for precise timing location.

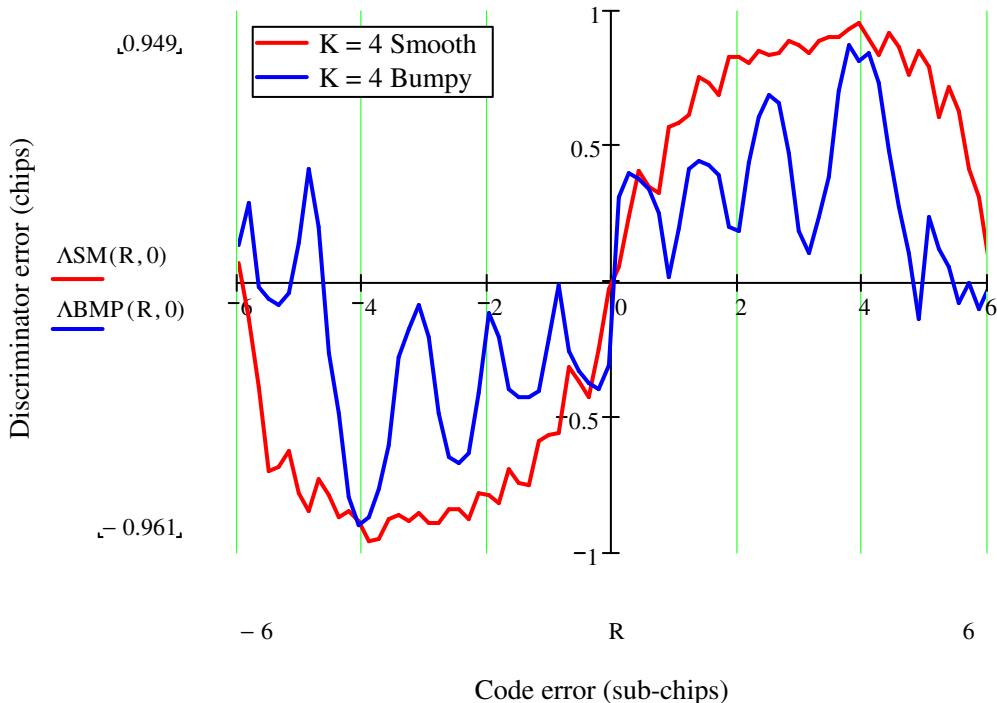


Figure 5-22, Composite MGD discriminators for a BOC($2 \times f_c, f_c$) signal

Assuming lock at the correct location the bumpy discriminator can deliver considerably less timing jitter than the smooth discriminator due to its steep zero crossing. In [Bello and Fante 2005] the r.m.s. timing jitter of these composite discriminators are compared to that given by the conventional BOC discriminator (Equation 4–20) and the SSB technique. Considering a BOC($2 \times f_c, f_c$) signal, the paper concludes that the SSB technique degrades the receivers timing sensitivity by a factor of 8 compared to the conventional BOC discriminator. This is because the timing jitter is now proportional to the discriminator formed from the underlying PSK modulation which is less sensitive by a factor of $4f_s/f_c$. The bumpy ($K = 4$) discriminator shown in Figure 5-22 is considered to be the best choice of composite discriminator for precise timing, as the timing jitter is only slightly (0.14 dB) worse than the conventional BOC discriminator. We have verified this result by inspection of the slope of the resulting bumpy discriminator curve whose zero crossing is shallower by a factor of 1.017, which equates to 0.146 dB worse timing jitter.

The bumpy discriminator suffers a slow response time for acquisition and large error steps due to the nulls present in its discriminator envelope. An example acquisition of the bumpy and smooth discriminator is shown in Figure 5-23 (derived from Mathcad

simulation). The loop bandwidth and noise conditions are set equal for both cases, $B_L = 1$ Hz, $C/N_0 = 30$ dB-Hz. The response of the bumpy discriminator flattens at sub-chip intervals as it passes a null in the discriminator significantly lengthening the loop settling time. Also, the jitter of the bumpy discriminator can be seen to be considerably less than that of the smooth discriminator.

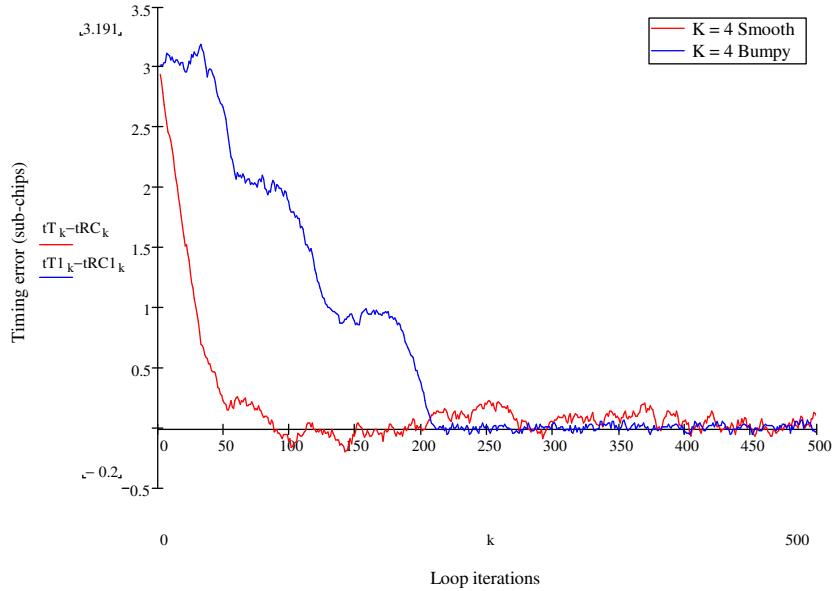


Figure 5-23, Acquisition example of MGD discriminators ($B_L = 1$ Hz , $C/N_0 = 30$ dB-Hz)

Running multiple acquisitions across different initial time offsets provides a comparison of the acquisition time of the MGD discriminators with the equivalent acquisition times using the SSB technique.

Table 5-5 shows the acquisition times of the MGD discriminators and the SSB technique, assuming a BOC(2, 1) signal, a carrier to noise density of $C/N_0 = 24$ dB-Hz, a loop bandwidth of $B_L = 1$ Hz and averaging across 20 acquisitions at each time step. We find agreement with the results presented in [Bello and Fante 2005] which compare the average loop settling time of the MGD discriminators. The smooth discriminator closely follows that of the equivalent SSB discriminator characteristic, with an acquisition performance only 1.23 times worse than the SSB technique. The bumpy MGD discriminator is worse by at least factor of 2 across the dataset. Therefore, composite MGD discriminators can potentially remove the ambiguity of BOC tracking. However, the receiver designer must make a trade-off between the receiver's response time and timing jitter.

**Table 5-5, Acquisition times of the MGD discriminators and the SSB technique for BOC(2, 1),
 $B_L = 1 \text{ Hz}$, $C/N_0 = 24 \text{ dB-Hz}$**

Initial chip offset	1/4	1/2	3/4
Smooth MGD acquisition time (ms)	730	1051	1623
Bumpy MGD acquisition time (ms)	906	1919	3065
SSB acquisition time (ms)	611	889	1216
SSB / Smooth	1.19	1.18	1.33
SSB / Bumpy	1.48	2.16	2.52

5.4.3 The bump-jumping algorithm

The final *state of the art* approach we consider in solving the BOC ambiguity problem is the ‘*bump-jumping*’ algorithm (BJ), proposed by in [Fine and Wilson 1999]. This algorithm determines whether or not the correct correlation peak is being tracked by comparing the amplitude of the peak currently being tracked to the amplitude of the adjacent peaks. This is achieved through the correlation of two additional offset replica codes called very early (VE) and very late (VL). These replicas are separated from the prompt (P) replica by a sub-chip, $\pm T_S$.

The algorithm is achieved by using three counters, each associated with the VE, P or VL samples. The amplitudes of VE, P and VL in-phase samples are compared at the end of each integrate-and-dump period. If the VE sample is larger then its counter is incremented and the VL counter decremented, if VL is larger the opposite occurs.

When P is the larger both VE and VL counters are decremented. A jump to a new peak occurs only if the VE or VL counters reach a specified threshold before the prompt counter. The counters are never decremented below zero and are reset when a threshold is reached. An example of a false-lock condition is shown in Figure 5-24 for a BOC($2 \times f_C, f_C$) with the appropriate gates required to implement the BJ algorithm. The narrowly spaced early-late gates provide fine tracking on the signal preserving the BOC discriminator with no sensitivity loss.

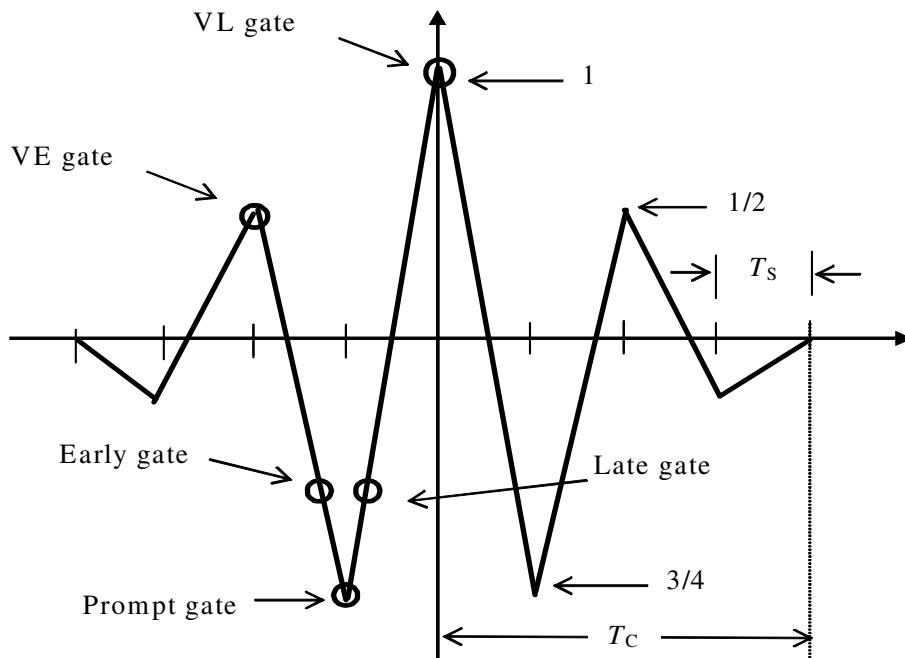


Figure 5-24, BOC($2 \times f_c, f_c$) false-lock example with BJ gates

The BJ algorithm can only correct one peak at a time, shifting the tracking point by a sub-chip each jump and resetting all counters. Conventional search processes acquire the signal with an accuracy of $\pm T_c/2$, therefore a number of corrections (jumps) may be necessary before a valid lock is established. Assuming search accuracy of $\pm T_c/2$, the maximum number of jumps required is equal to the ratio of sub-carrier to code ratio f_s/f_c . Therefore, a major drawback to the BJ algorithm can be the time taken to reach the correct timing location either from acquisition or from a slip in tracking. The BJ algorithm is effectively ‘blind’ to the number of sub-chips required to find the valid timing location, it must correct one at a time in sub-chip steps. In contrast, techniques providing a discriminator similar to that of a PSK signal, such as the SSB technique and the smooth MGD discriminators can make corrections across the whole discriminator characteristic in a single step.

The acquisition or slip correction time of the BJ algorithm is not only dependant on the discriminator curve and loop setting time but also depends on the time taken determine a false lock. The receiver’s VE or VL counter must pass a predetermined threshold in order to determine a false lock state. This threshold must be set sufficiently high so that the level of noise on the VE and VL correlations will not cause a false lock to be declared when in fact the receiver is tracking the correct

timing location. Therefore, the threshold must be designed for the most severe noise environment the receiver will operate in, with some margin. The relative amplitude between the main BOC correlation peak and its adjacent peaks decreases with the sub-carrier to code ratio. Hence the threshold for detecting a false lock condition increases for high rate BOC signal in turn increasing the acquisition and correction time.

In [Fine and Wilson 1999] a figure of $C/N_0 = 24$ dB-Hz is used to represent in a minimum signal to noise density, which is reasonable for weak signal applications at approximately 15 dB less than the representative minimum GPS signal to noise density (38.9dB-Hz in [Kaplan and Hegarty 2006]). Considering a 20ms integration period this equates to a minimum signal to noise of 10 dB per correlation. An uncorrelated noise threshold level can then be calculated by assuming uncorrelated Gaussian noise on the VE and VL correlations. Figure 5-25 shows the worse case of many trials assuming an uncorrelated 10 dB signal to noise on each correlation for a BOC($2 \times f_c, f_c$). A threshold of 8 is identified with corresponds to the analysis and threshold choice in [Fine and Wilson 1999]. See Appendix E for details of the BJ threshold calculation and algorithm simulation in Mathcad.

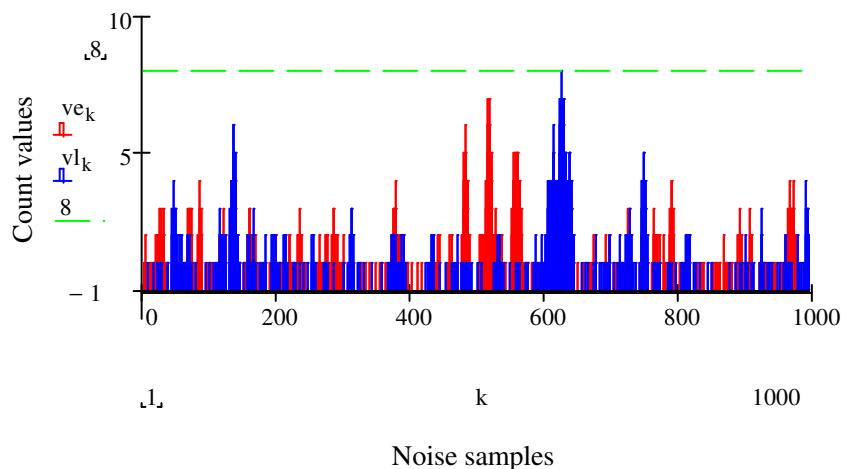


Figure 5-25, Worse case VE and VL count values for BOC($2 \times f_c, f_c$) with uncorrelated signal to noise of 10 dB per correlation

However, as identified by Dr Hodgart, the noise samples are in fact strongly correlated which actually improves the performance of the BJ algorithm. For BOC($2 \times f_c, f_c$) the correlation coefficient between noise separated by T_S and therefore

between VE and P and between VL and P is $\rho = -0.75$. The correlation coefficient of noise between the VE and VL samples is $\rho = -0.5$. The resulting worse case noise induced count values for correlated noise are shown in Figure 5-26, which finds a required threshold of 5.

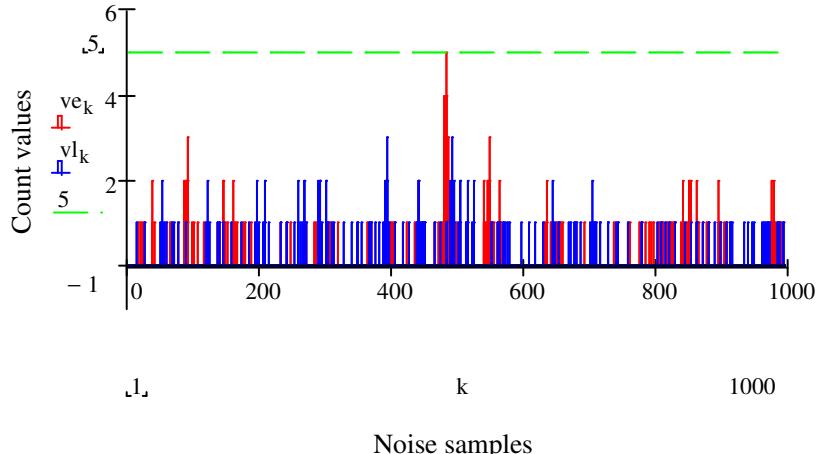


Figure 5-26, Worse case VE and VL count values for BOC($2 \times f_c, f_c$) with correlated noise samples, signal to noise of 10 dB per correlation

Clearly if the correlation or integration time is reduced from 20 ms the threshold must be increased accordingly because the signal to noise per correlation will be reduced. An example acquisition of a BOC(2, 1) signal is shown in Figure 5-27, with $B_L = 1$ Hz and noise, $C/N_0 = 30$ dB-Hz. The BJ threshold level has been calculated for a minimum carrier to noise density of $C/N_0 = 24$ dB-Hz. It can be seen that the acquisition time is not dependant only on the loop settling time but on the time taken to reach the required threshold level and declare an invalid tracking state.

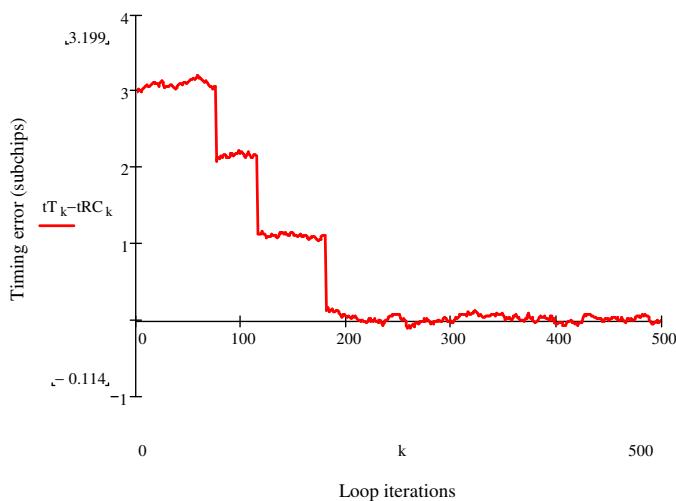


Figure 5-27, Acquisition example of BJ algorithm for BOC(2, 1) signal ($B_L = 1$ Hz, $C/N_0 = 30$ dB-Hz, $T_D = T_S$)

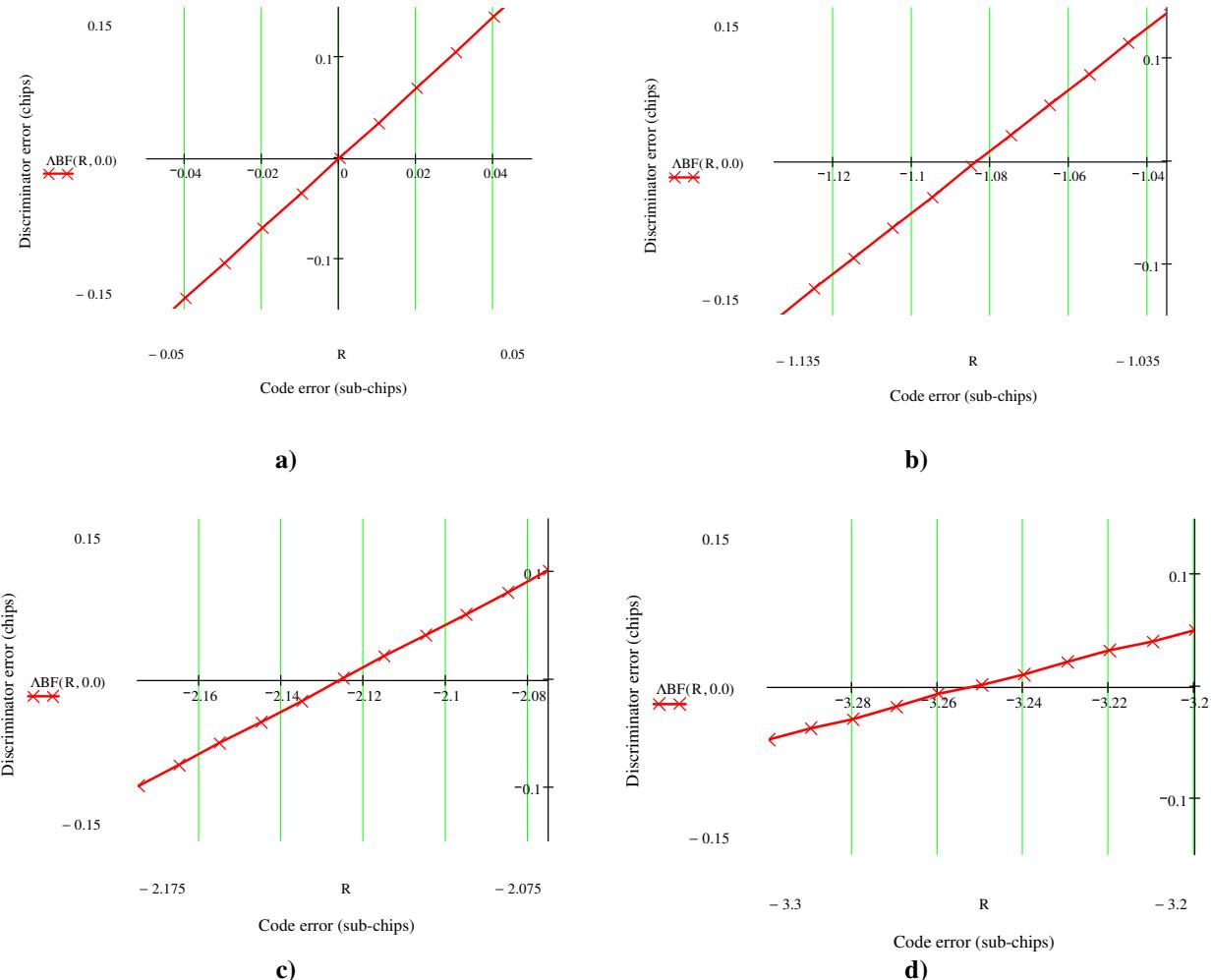
The average time to make a correction can be formulated counting the number of times the threshold level is reached while in a false-lock condition. Starting at an offset of 1 sub-chip and applying the BJ counters over 2000 correlations without timing correction, Mathcad simulation finds the number of thresholds reached is 99 with an equivalent $C/N_0 = 24$ dB-Hz. This gives an average of 20.2 correlations per correction. This results in a correction time of 303 ms for a sub-chip correction (for integration time, $T = 15$ ms).

Running multiple acquisitions across different initial time offsets provides a comparison of the acquisition time of the BJ algorithm with the equivalent acquisition times using the SSB technique. Table 5-6 shows the acquisition times of the BJ algorithm and SSB technique, assuming a BOC(2, 1) signal, a carrier to noise density of $C/N_0 = 24$ dB-Hz, a loop bandwidth of $B_L = 1$ Hz and averaging across 20 acquisitions at each time step. For the BOC(2, 1) signal the BJ algorithm shows approximately equivalent performance to the SSB technique across all initial offsets.

Table 5-6, Acquisition times of the BJ and SSB for BOC(2, 1), $B_L = 1$ Hz, $C/N_0 = 24$ dB-Hz

Initial chip offset	1/4	1/2	3/4
BJ acquisition time (ms)	413	655	1639
Jumps required	1	2	3
Correction time (ms)	303	606	909
SSB acquisition time (ms)	611	889	1216
BJ / SSB	0.676	0.737	1.348

The BJ poor performance at large initial offsets ($>1/2$ chip) can be explained by examining the discriminator curve at different false locking points. It is assumed at the discriminator will settle at integer sub-chip offsets, however this is not true. There is an offset between discriminator's zero crossings and the integer sub-chip, which increases with each integer sub-chip due to the different gradients of the discriminator either side of each peak. The discriminator zero crossings of a $\text{BOC}(2 \times f_c, f_c)$ signal are shown in Figure 5-28.


 Figure 5-28, Zero crossings of a BOC($2 \times f_c, f_c$) signal

At integer multiples of sub-chip offsets the difference in amplitude between the P correlation and VE or VL correlations used for BJ correction is assumed constant at T_s/T_c . However, shifting the false-lock location away from the integer sub-chip reduces the relative amplitude difference between the peaks required for the BJ comparison. The zero-crossing locations and respective P, VE and VL correlations for early false-lock conditions of a BOC($2 \times f_c, f_c$) signal are shown in Table 5-7. The amplitude difference between the P and VE correlation decreases with the sub-carrier offset, which in turn increases the time taken to detect a false-lock condition under the same noise conditions. The effect band limiting by the receiver front-end filter will round off the peaks and exacerbate this problem by further reducing the relative peak amplitude.

Table 5-7, BJ parameters for BOC($2 \times f_c, f_c$) under false-lock conditions

Early false-lock points	1	2	3
Zero crossing location (T_S)	1.085	2.125	3.25
P correlation amplitude	-0.644	0.406	-0.186
VE correlation amplitude	0.851	-0.594	0.312
VL correlation amplitude	0.436	-0.219	-0.002
Comparison amplitude $ VE - P $	0.207	0.188	0.126

The BJ BOC($2 \times f_c, f_c$) receiver threshold is designed for a peak amplitude difference of $A/4$. The reduction of this comparison amplitude results in the potential for the receiver to make a wrong decision while in a false lock condition. For example, at the 3rd false lock point the BOC(2,1) receiver occasionally decides that valid tracking is occurring and remains in its current position. This results in increased acquisition time of the BOC(2,1) BJ simulation at large initial offsets. The effect becomes more pronounced for high rate BOC modulations.

Table 5-8 shows the simulated acquisition times for a BOC(6, 1) signal under the same conditions. For the high rate BOC(6, 1) the BJ is significantly worse over all initial offsets. This is mostly due to the small difference between the central correlation peak and its adjacent pairs, now only 1/12 compared to 1/4 for BOC(2, 1). This results in a significant increase in threshold level, which in turn increases the correction time. Simulating with an initial offset of 1 sub-chip and applying the BJ counters over 2000 correlations without timing correction, we find the number of thresholds reached is 54 with an equivalent $C/N_0 = 24$ dB-Hz. This results in a correction time of 810 ms for a sub-chip correction (for integration time, $T = 15$ ms).

Compared with the SSB technique the acquisition performance of BJ algorithm becomes worse as the initial offset is increased. Again this is due to a reduction in the comparison amplitude because the tracking loops do not settle at integer sub-chip offsets. With larger initial offsets the reduction in comparison amplitude is greater resulting in increased acquisition time from the nominal correction time.

Table 5-8, Acquisition times of the BJ and SSB for BOC(6, 1), $B_L = 1$ Hz, $C/N_0 = 24$ dB-Hz

Initial chip offset	1/12	2/12	3/12	4/12
BJ acquisition time (ms)	1009	2327	3481	4754
Jumps required	1	2	3	4
Correction time (ms)	810	1620	2430	3240
SSB acquisition time (ms)	276	527	611	736
BJ / SSB	3.65	4.42	5.69	6.46

5.4.4 The effect of distortion on the BJ algorithm

Observations of the wide band BOC(15, 2.5)-cosine Galileo PRS signal transmitted from the Giove-A satellite have shown an asymmetry in the spectrum [Montenbruck *et al* 2006]. No significant asymmetry was observed before the amplification by high power ‘travelling-wave tube’ (TWT) amplifiers. It is assumed that the asymmetry is due either to the amplitude dependant phase distortion of TWTs or in the final stage RF filters. In [Graf and Günther 2006] a model of the phase distortion of TWTs is shown to result in similar distortion to that of the Giove-A signals. It has been argued that this asymmetry is a result of filter designs intended for a slightly narrower BOC(14,2) modulation. However, a certain amount of asymmetry has been observed in all BOC transmissions from Giove-A. Even observations of the narrow band BOC(1,1) modulation show an asymmetry which although small may still compromise receiver operation under weak signal conditions.

Although a certain amount of asymmetry correction may be possible in the transmitter, distortion may be an inherent problem with BOC transmissions. Even if the distortion is perfectly corrected in transmission, the large bandwidths occupied by many of the future BOC transmissions may result in significant asymmetry from consumer-grade receiver front-end filters.

This asymmetry in the spectrum translates into an asymmetric correlation, which has been observed to potentially cause tracking errors in BOC receivers using the BJ algorithm [Falcone 2006]. This is due to the reduction in magnitude difference between the central correlation peak and its adjacent peaks. The BJ algorithm relies of the difference in peak magnitudes in order to determine the correct tracking state.

In order to assess the effect on receiver tracking schemes we can model a received asymmetry in BOC by introducing a fixed offset between the received code and sub-carrier. For example Figure 5-29 shows an correlation of an asymmetric correlation BOC($2 \times f_C, f_C$) created by introducing a quarter sub-chip offset between the code and sub-carrier.

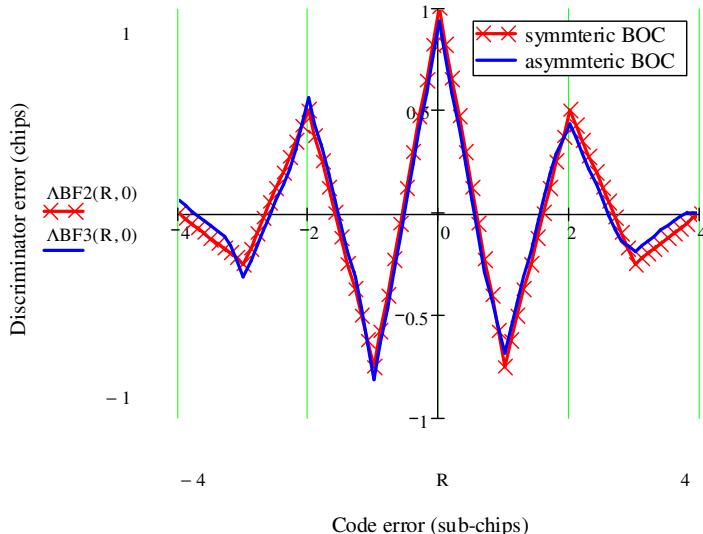


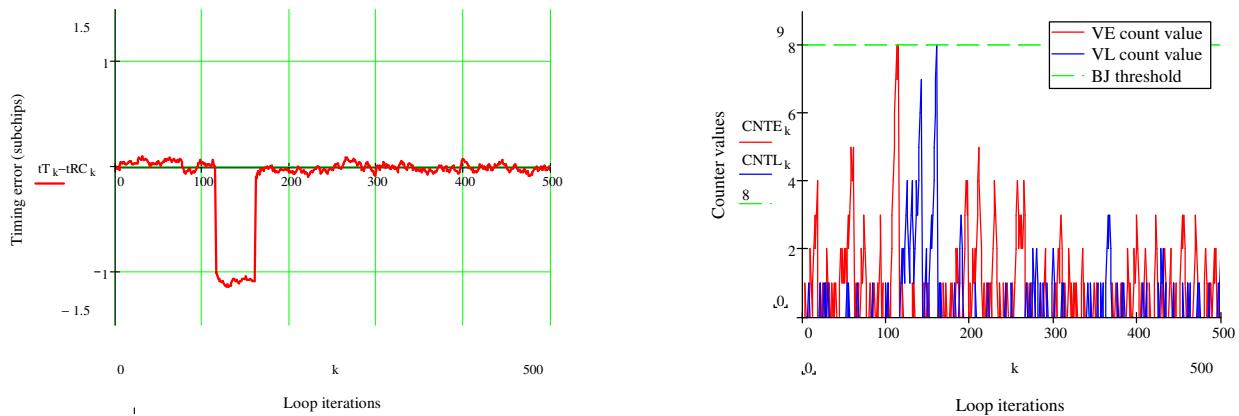
Figure 5-29, Symmetric and asymmetric BOC($2 \times f_C, f_C$) correlations, sub-carrier to code offset $= T_S / 4$

An asymmetric correlation function has a significant effect on the integrity of tracking using the BJ algorithm. The asymmetry reduces the relative difference in peak amplitudes (see Table 5-9), which is vital for the BJ algorithm to correctly identify a valid tracking state. Therefore, the BJ threshold must be increased to ensure stable tracking.

Table 5-9, Symmetric and asymmetric BOC($2 \times f_c, f_c$) peak values

Peak	Symmetric amplitude	Asymmetric amplitude (sub-carrier to code offset = $T_S / 4$)
P	1	0.937
VE	-0.75	-0.812
VL	-0.75	-0.687
P - VE	0.25	0.125

The BJ tracking algorithm requires careful tuning. If a BJ threshold is set too low to account for the noise conditions or asymmetry in the signal the BJ algorithm can cause the receiver to jump out of correct lock to an invalid tracking state. An example of this is shown in Figure 5-30. Here the BJ threshold has been calculated for a symmetric BOC(2,1) signal operating at a carrier to noise of 24 dB-Hz with an equivalent integration time of 15 ms. An asymmetric correlation is created by introducing a quarter sub-chip offset between the sub-carrier and the code in the received signal (see Figure 5-29). It can be seen that noise induced increments of the very early counter pass the BJ threshold, causing a jump to an invalid tracking state. The tracking estimate remains in error until correction by the very late counter passing the BJ threshold. The threshold must be increased to a stage where noise induced increments of the counters should never cause a jump from the correct tracking state. The increase in threshold results in an increase acquisition and correction time.

**Figure 5-30, Example jump to invalid tracking state, BOC(2,1), $C/N_0 = 24$ dB-Hz, sub-carrier to code offset = $T_S / 4$**

The effect of asymmetry is more significant for BOC signals with high ratios of sub-carrier frequency to code rate. The BJ algorithm relies on the ability to determine the magnitude difference between the central and secondary BOC correlation peaks. As the ratio of sub-carrier frequency to code rate increases the magnitude difference decreases. For example, the magnitude difference Galileo BOC(15,2.5) signal is only 1/12 compared with 1/2 for BOC(1,1). Therefore, any further reduction due to asymmetry can completely compromise the receiver's ability to determine a valid tracking state. Asymmetry has been observed to compromise the operation of the Septentrio GETR implementation of the BJ algorithm with the BOC(15,2.5) signal from Giove-A.

In addition to compromising the receiver's tracking integrity, asymmetry in the received BOC signal causes a bias in the receiver's delay estimate when operating the BJ algorithm. The reason for the tracking bias is obvious when examining the correlation envelope of an asymmetric signal. An exaggerated asymmetry correlation is depicted in Figure 5-31. The slope of the symmetric correlation is equal on both sides and has no tracking bias. However, the asymmetric slope is steeper on one side. Therefore, with equally spaced early-late gates the asymmetry causes a bias in the receiver estimated delay.

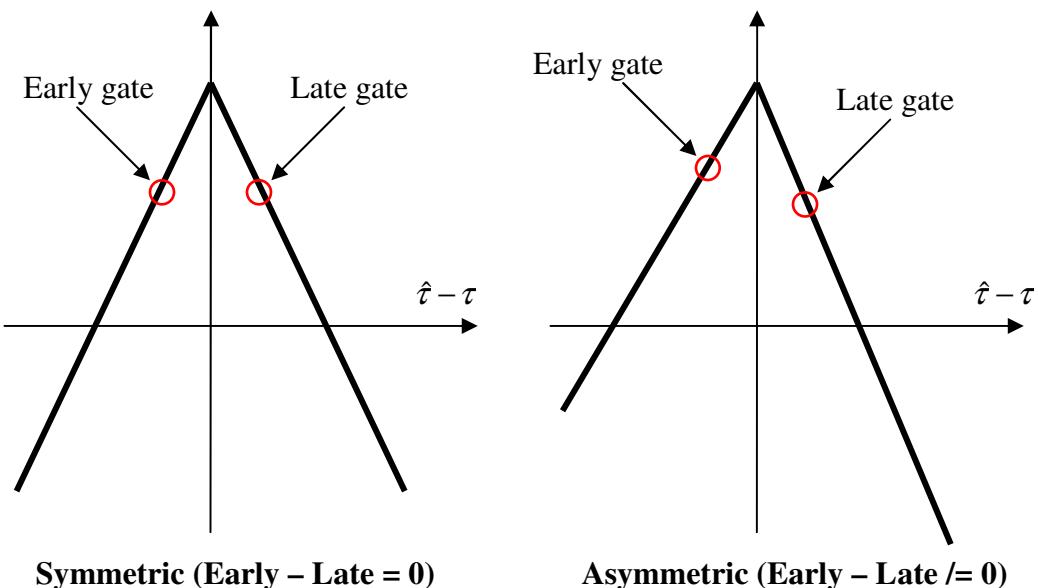


Figure 5-31, Depiction of asymmetric tracking bias

5.4.5 The effect of multipath on the BJ algorithm

The BJ algorithm relies on the ability to detect whether or not the receiver has settled to a valid tracking state through comparison of the adjacent correlation peaks. The central BOC correlation peak must be sufficiently greater in amplitude than its adjacent peaks to enable valid tracking in the presence of noise. In Section 5.4.3 it was shown that the comparison amplitude between the peaks, required for the BJ algorithm to make a correction, reduces the further the false-lock point is from the centre of the correlation function. This degrades the performance of the peak detection and poses a potential integrity risk to the receiver. Inference from multipath signals can further reduce the comparison amplitude and therefore further degrades the performance of the BJ algorithm.

Figure 5-32 shows the effect of multipath interference on a BOC(2,1) signal. The multipath is assumed to be of half amplitude relative to the direct signal with an in-phase carrier and therefore provides a worst-case scenario. It is assumed that the receiver maintains lock on the central peak of the BOC correlation. The comparison amplitude is the difference between either the prompt, P and very-early, VE correlations or the prompt and the very-late, VL correlations. Reducing either of these comparison amplitudes will result in an increased chance jump away from the valid timing location in the presence of noise. The receiver designer must then increase the BJ threshold to account for noise induced increments of the VE and VL counters or risk the integrity of the receiver under strong multipath.

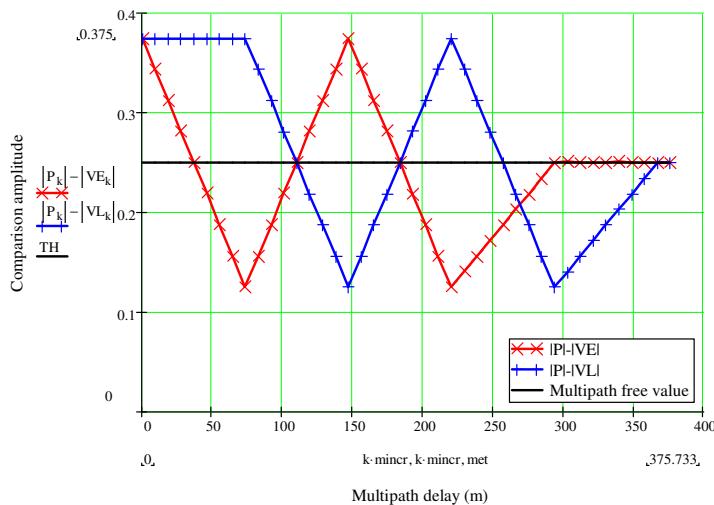


Figure 5-32, BJ comparison amplitude of BOC(2, 1) correlations against relative multipath delays (in-phase carrier, central correlation peak tracking)

The results show that when the relative delay of the multipath interference is at integer sub-chip (73 m) intervals the comparison amplitude is halved from the nominal value (no multipath interference present). At short multipath delays however, the comparison amplitude is actually 3/2 times greater than the nominal value, actually improving the performance of the BJ peak detection. In this case the multipath is constructive to the BOC correlation at short delay because the multipath is in-phase with the direct carrier signal. Simulating a multipath which is 180° out of phase with the direct signal results in the opposite effect as shown in Figure 5-33.

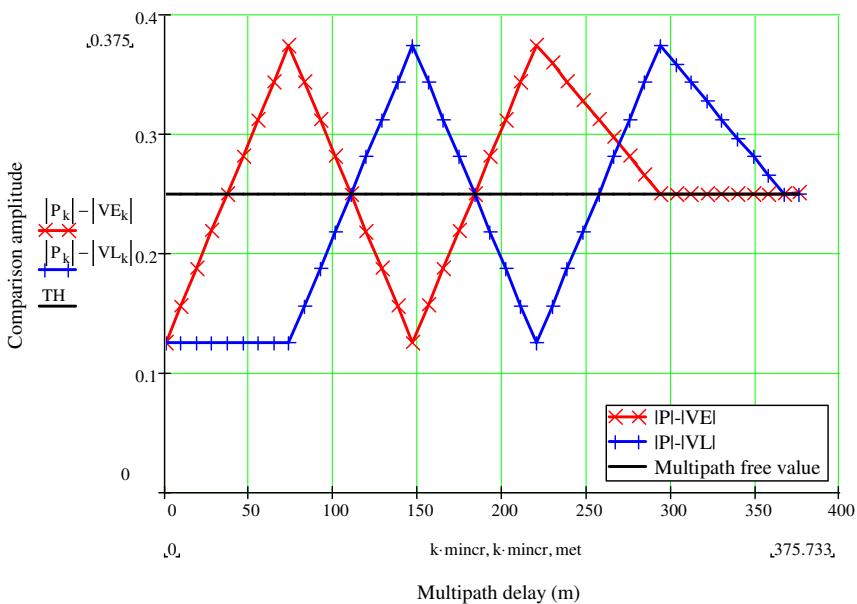


Figure 5-33, BJ comparison amplitude of BOC(2, 1) correlations against relative multipath delays (180° out of phase, central correlation peak tracking)

Clearly the presence of strong multipath can significantly compromise the ability of the BJ algorithm to determine the valid tracking location. This problem becomes worse for higher ratios of sub-carrier frequency to code rate such as BOC(15,2.5) where the BJ comparison amplitude is already very small.

In Chapter 6 we describe an entirely new approach to tracking BOC signals which is believed to be robust to distortions in the received signal.

5.4.6 Hardware requirements of BOC tracking techniques

In order to fully evaluate and compare the BOC tracking techniques presented here we must also look at the impact to the receiver hardware. Table 5-10 shows the hardware requirements of the BOC tracking techniques, for achieving incoherent carrier and code tracking. The MGD discriminator is formed from 4 early and 4 late correlations, requiring 16 code multipliers and integrators for incoherent code tracking. An additional 2 multipliers and integrators are required for carrier tracking making a total of 18, a significant overhead for each tracking channel. The filtering required for the SSB technique is undesirable and can significantly impact the size and complexity of the receiver. Hence, the best choice in terms of hardware requirements is the BJ algorithm.

Table 5-10, Hardware requirements of BOC tracking techniques

Receiver type	Multipliers	Integrators	Local oscillators	Low pass filters
SSB	2×Carrier, 4×Code	4	1×Carrier, 1×Code	2
MGD (K=4)	2×Carrier, 18×Code	18	1×Carrier, 1×Code	0
BJ	2×Carrier, 8×Code	8	1×Carrier, 1×Code	0

5.4.7 Comparison of BOC tracking schemes

The BJ algorithm has been implemented on the Septentrio GETR [De Wilde *et al* 2004]. This receiver was built under contract from ESA to demodulate and evaluate new Galileo signals. Analysis contained in this chapter shows that although the use of a peak detection algorithm (*bump-jumping*) seems a logical engineering approach to solving BOC tracking ambiguity it is sensitive to noise, signal distortion and multipath. Therefore, the use of the BJ algorithm is not recommended for high integrity or safety of life applications.

The BJ jumping algorithm provides the receiver designer with a similar trade-off to the bumpy MGD discriminator, delivering apparent unambiguous BOC tracking with little or no sensitivity loss at the cost of acquisition and slip correction time. The SSB

technique provides the best acquisition and slip correction performance at the cost of a loss in tracking sensitivity. In Chapter 6 we describe a novel technique developed during this research which is believed to solve the problem of BOC tracking ambiguity. This technique removes the ambiguity in BOC tracking with no tracking sensitivity loss and with no degradation of acquisition or slip correction time.

In this chapter we have detailed the current approaches given in the literature for PSK and BOC signals. A comparison of three leading BOC tracking techniques was given based on their tracking sensitivity, acquisition time and receiver hardware impact. A design trade off has been identified between high precision receivers using the BJ algorithm or *bumpy* MGD technique and the rapid reliable acquisition of the SSB or *smooth* MGD techniques.

6 BOC tracking with double estimation receiver

This chapter discusses the implementation and benefits of BOC tracking using the double estimator (DE). This technique was conceived during the course of this research and a patent has recently been filed for protection of the inventors, Dr MS Hodgart and PD Blunt. Coherent and incoherent implementations are given along with an extension to apply the DE technique to AltBOC signals. Details of our simulations of the DE technique are given including analysis of noise induced tracking jitter, acquisition and slip correction times and multipath analysis. Comparison is given to the BOC tracking schemes described in Chapter 5.4 and the relative benefits detailed.

6.1 The coherent BOC double estimator

Once again we model the received BOC signal (neglecting additive noise and other interfering GNSS signals) as follows.

$$u_{BOC}(t) = A \times \cos(\omega_0 t + \phi) \times a(t - \tau) \times s(t - \tau) \times d \quad \text{6-1}$$

A is amplitude, $\cos(\omega_0 t + \phi)$ represents the carrier signal after down conversion to an intermediate frequency (IF) ω_0 and phase ϕ , $s(t - \tau)$ is the sub-carrier modulation in the received signal comprising the sub-carrier modulation function $s(t)$ at delay τ , $a(t - \tau)$ is the code modulation in the received signal comprising the code modulation $a(t)$ at delay τ and $d \in (-1,+1)$ is a polarity.

This technique depends essentially on the fact that sub-carrier is half-periodic over a relatively short sub-chip width T_S and that Equation 6-1 is mathematically identical to

$$u(t) = A \times \cos(\omega_0 t + \phi) \times s(t - \tau^*) \times a(t - \tau) \times d^* \quad \text{6-2}$$

where

$$\tau^* = \tau + nT_S \quad \text{6-3}$$

is a multi-valued offset delay which has a number of values each offset from the delay τ by a different integer shift n times the sub-chip width T_S . The equivalent polarity $d^* = d$ for even number of shifts and $d^* = -d$ for an odd integer shift. It should be understood that the actual sub-carrier delay and the code delay for any received signal are still the same τ . The receiver must always estimate this actual non-ambiguous delay τ in the code function $a(\cdot)$. It is however only necessary for the receiver to seek to estimate the ambiguous τ^* in the sub-carrier function $s(\cdot)$ and achieve the same result as if it were estimating the actual delay τ . Accordingly, the offset delay τ^* and delay τ are treated as independent quantities, without regard to Equation 6-3, and two independent estimates may be generated. Only in a final correction stage is it admitted that an estimate of offset delay τ^* and delay τ are related as in Equation 6-3, and the value of estimate $\hat{\tau}$ used to remove the ambiguities in the value of estimate $\hat{\tau}^*$.

In a BOC transmission the sub-carrier is necessarily locked to the code sequence. Indeed it is usually seen as part of the code sequence. The time delay τ must obviously be the same in both the code and the sub-carrier. However, there is nothing to stop us multiplying by component multiplicative structures with independent time delay estimates. The DE technique is a three-loop receiver. The innermost delay-locked loop (DLL) tracks the code phase of the received signal. The middle sub-carrier locked loop (SLL) tracks the sub-carrier phase of the received signal. The third loop tracks the carrier frequency and / or phase of the received signal. The general schematic of the coherent DE receiver is shown in Figure 6-1.

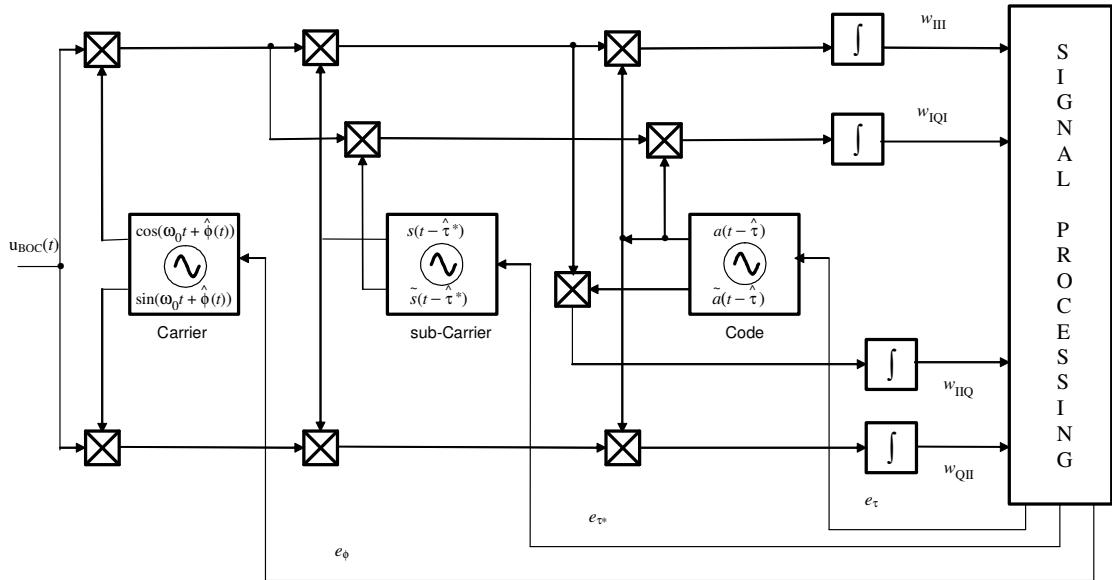


Figure 6-1, General schematic of a coherent DE BOC receiver

The DE BOC receiver requires three local oscillators, which generate continuous carrier, sub-carrier and code waveforms respectively. The carrier oscillator generates in-phase replica carrier $\cos(\omega_0 t + \hat{\phi})$ and an orthogonal replica carrier $\sin(\omega_0 t + \hat{\phi})$, where $\hat{\phi}$ is the estimate of the received carrier phase ϕ . The sub-carrier oscillator generates in-phase replica sub-carrier $s(t - \hat{\tau}^*)$ and an orthogonal replica carrier $\tilde{s}(t - \hat{\tau}^*)$, where $\hat{\tau}^*$ is the SLL estimate of the time delay τ . The code oscillator generates in-phase replica code $a(t - \hat{\tau})$ and an orthogonal replica code $\tilde{a}(t - \hat{\tau})$, where $\hat{\tau}$ is the DLL estimate of the time delay τ .

We define an orthogonal sub-carrier as the difference between early and late time shifts of the sub-carrier, which can be written as follows.

$$\tilde{s}(t - \hat{\tau}^*) = s\left(t - \hat{\tau}^* + \frac{T_{DS}}{2}\right) - s\left(t - \hat{\tau}^* - \frac{T_{DS}}{2}\right) \quad 6-4$$

T_{DS} is the total separation between ‘early’ and ‘late’ sub-carrier waveforms, bounded by $0 < T_{DS} \leq T_s$.

After mixing and integration over time T the resulting correlations can be written as follows.

$$\begin{aligned}
 w_{III} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \cos(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}^*) \times a(t - \hat{\tau}) dt & \text{6-5} \\
 &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\
 w_{IIO} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \cos(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}^*) \times \tilde{a}(t - \hat{\tau}) dt \\
 &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times v^\Delta(\hat{\tau} - \tau) \times d \\
 w_{IQI} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \cos(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}^*) \times a(t - \hat{\tau}) dt \\
 &\approx A \times \cos(\phi - \hat{\phi}) \times \text{Trs}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\
 w_{QII} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \sin(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}^*) \times a(t - \hat{\tau}) dt \\
 &\approx A \times \sin(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d
 \end{aligned}$$

The single peaked $\Lambda()$ function and the tracking $v^\Delta()$ function are the same as defined for the PSK GNSS receiver in Equation 5-8 and Equation 5-18 respectively. The $\text{trc}()$ function is a continuous triangular cosine waveform where $\text{trc}(\hat{\tau}^* - \tau) \rightarrow \pm 1$ as $\hat{\tau}^* \rightarrow \tau + n \times T_s$. The $\text{Trs}()$ function is a continuous trapezium shaped sine waveform where $\text{Trs}(\hat{\tau}^* - \tau) \rightarrow 0$ as $\hat{\tau}^* \rightarrow \tau + n \times T_s$, shown in Figure 6-2. The $\text{Trs}()$ function is identical to the result of early minus late correlations of the $\text{trc}()$ function as follows.

$$\text{Trs}(\hat{\tau}^* - \tau) = \text{trc}\left(\hat{\tau}^* - \tau - \frac{T_{DS}}{2}\right) - \text{trc}\left(\hat{\tau}^* - \tau + \frac{T_{DS}}{2}\right) \quad \text{6-6}$$

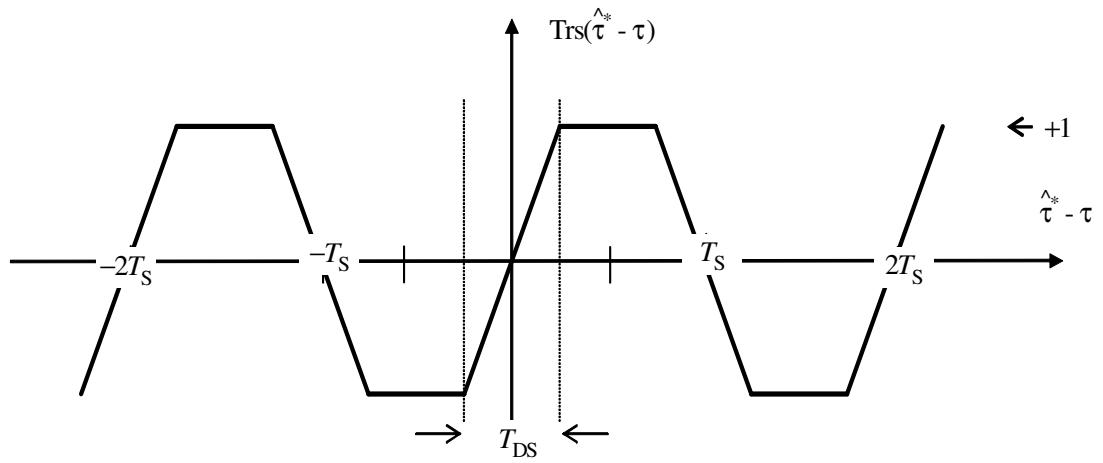
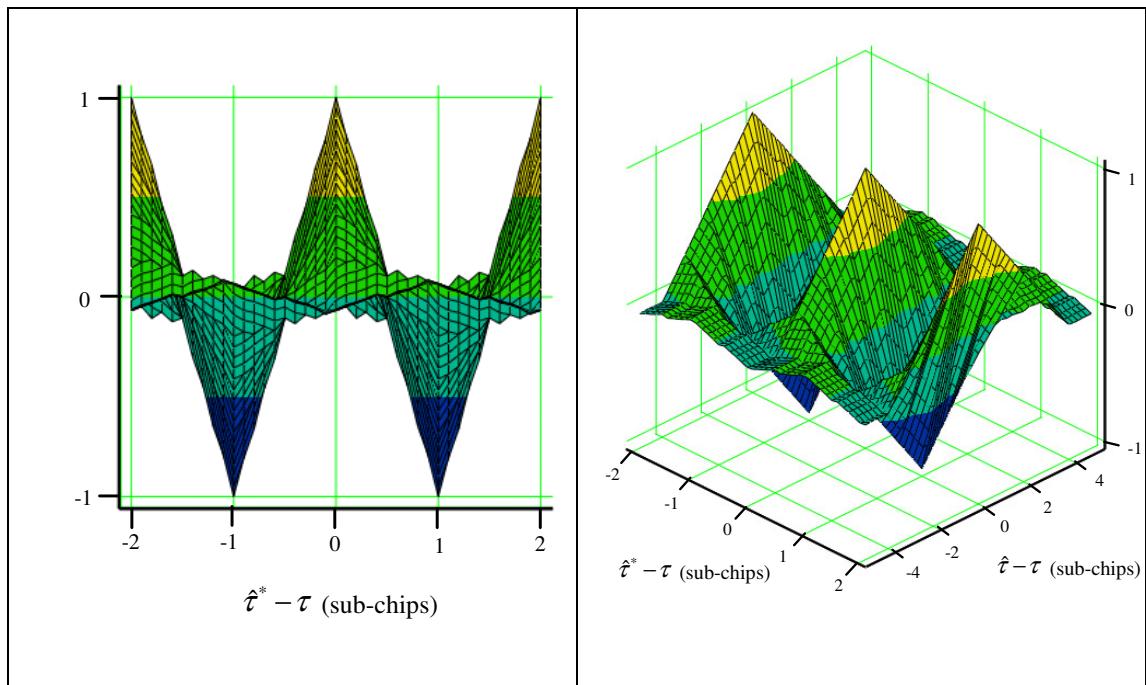


Figure 6-2, Trapezoidal sine function

The easiest way to visualise the effect of realising independent sub-carrier and code delay estimates in the DE BOC correlations is assume perfect carrier demodulation, $\phi = \hat{\phi}$. Figure 6-3, Figure 6-4 and Figure 6-5 show the w_{III} , w_{IIQ} and w_{IQI} correlations respectively against code error, $\hat{\tau} - \tau$ and sub-carrier error $\hat{\tau}^* - \tau$ assuming $\phi = \hat{\phi}$.

These plots are derived from Mathcad simulations of a BOC($2 \times f_c, f_c$) signal and provide a graphical perspective to the correlations given in Equation 6-5.

Figure 6-3, w_{III} correlation with independent sub-carrier and code delay estimates

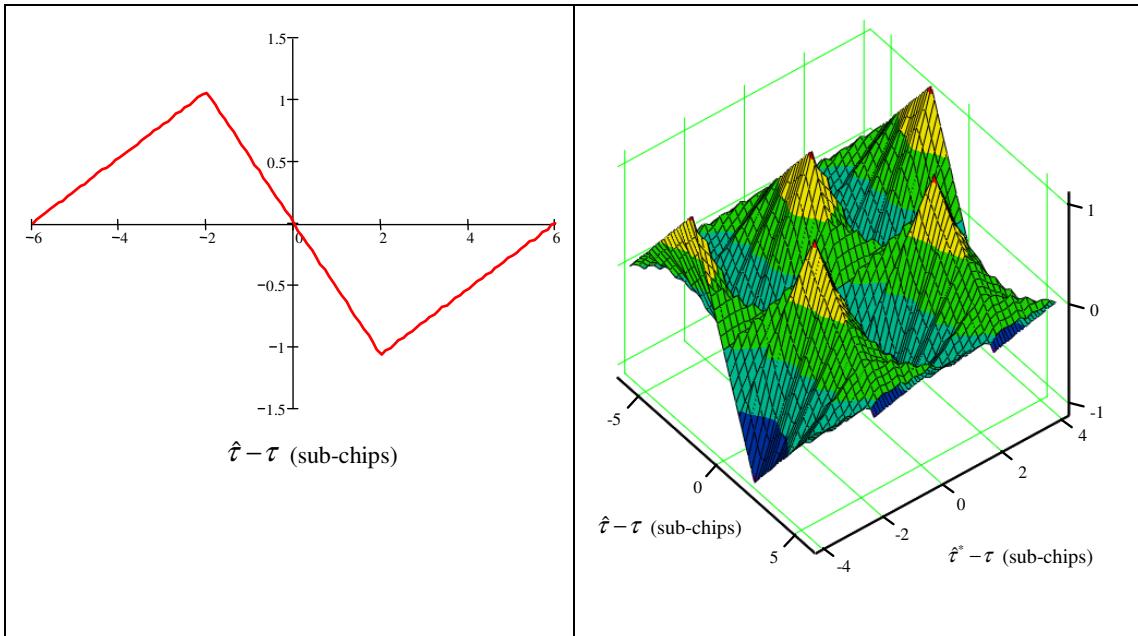


Figure 6-4, w_{HQ} correlation with independent sub-carrier and code delay estimates $T_{DC} = T_C$

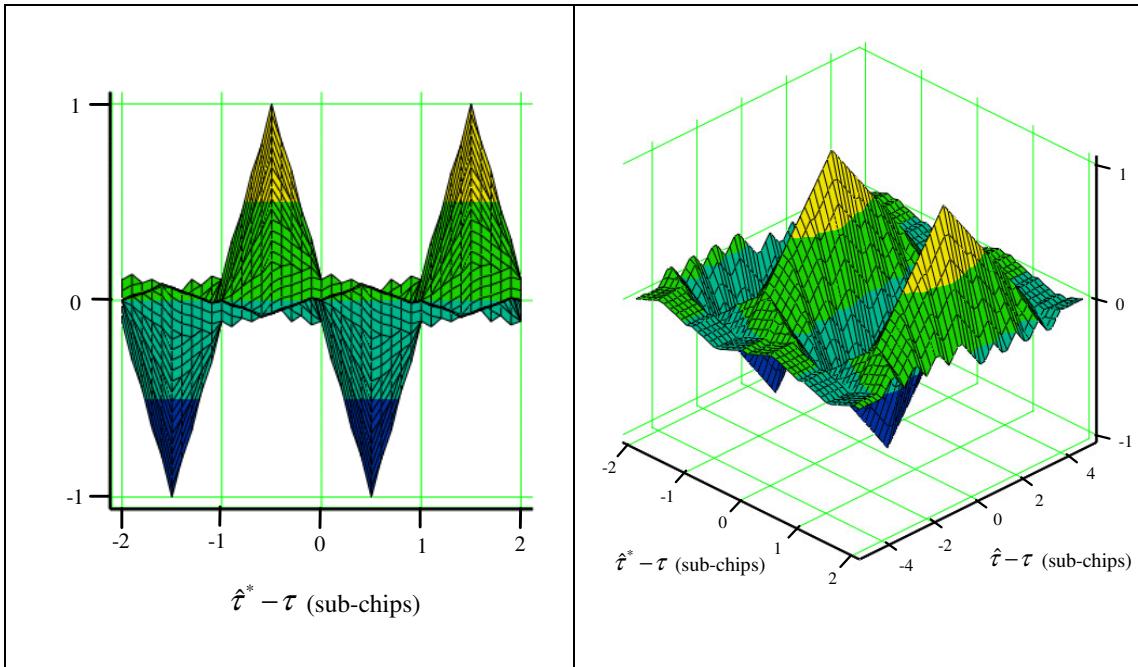


Figure 6-5, w_{IQI} correlation with independent sub-carrier and code delay estimates $T_{DS} = T_S$

A number of discriminators used to remove the amplitude dependence require generation of signals individually multiplied by early and late replica code sequences. Equivalent early and late code correlations may be generated as

$$\begin{aligned}
 w_{IIE} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \cos(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}^*) \times a\left(t - \hat{\tau} \pm \frac{T_{DC}}{2}\right) dt \\
 w_{ILL} &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda\left(\hat{\tau} - \tau \mp \frac{T_{DC}}{2}\right) \times d
 \end{aligned} \tag{6-7}$$

where the equivalent early minus late correlation is

$$w_{IIL} = w_{IIE} - w_{ILL} \tag{6-8}$$

In order to achieve convergence of the DE triple loop system three error signals must be generated from the correlations in Equation 6-5. Firstly addressing the outer carrier loop, we are considering a coherent DE BOC receiver, therefore implying phase tracking with a PLL. The carrier phase error is commonly determined using a Costas decision-directed discriminator, which can be applied to the DE BOC receiver as follows.

$$e_\phi = w_{QII} \times \text{sgn}(w_{III}) \approx A \times \sin(\phi - \hat{\phi}) \times \text{sqc}(\phi - \hat{\phi}) \times |\text{trc}(\hat{\tau}^* - \tau)| \times \Lambda(\hat{\tau} - \tau) \tag{6-9}$$

$\text{sqc}()$ is a square wave cosine function. Incorporating the sign correction by hard-limiting the w_{III} correlation in the discriminator allows the PLL to function with no knowledge of the navigational data state. It can be seen that e_ϕ tends to zero as $\sin(\phi - \hat{\phi})$ tends to zero, which occurs at integer n multiples of π radians as $\hat{\phi} \rightarrow \phi + n\pi$. The most common Costas PLL discriminators for the DE BOC receiver are shown in Table 6-1.

Table 6-1, Costas PLL discriminators for the DE BOC receiver

Discriminator	Error signal	Dependency
Decision-corrected	$e_\phi = w_{QII} \times \text{sgn}(w_{III})$ $\approx A \times \sin(\phi - \hat{\phi}) \times \text{sqc}(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A
Dot product	$e_\phi = w_{QII} \times w_{III}$ $\approx \frac{A^2}{2} \times \sin[2 \times (\phi - \hat{\phi})] \times \text{trc}^2(\hat{\tau}^* - \tau) \times \Lambda^2(\hat{\tau} - \tau)$	Slope proportional to A^2
Normalised	$e_\phi = w_{QII} / w_{III}$ $\approx \tan(\phi - \hat{\phi})$	Slope independent of amplitude
2 quadrant arc tangent	$e_\phi = \arctan(w_{QII} / w_{III})$ $\approx (\phi - \hat{\phi})$	Slope independent of amplitude

The sub-carrier phase error for the coherent DE BOC receiver can also be determined using a decision-directed discriminator as follows.

$$e_{\tau^*} = w_{IQI} \times \text{sgn}(w_{III}) \approx A \times |\cos(\phi - \hat{\phi})| \times \text{Trs}(\hat{\tau}^* - \tau) \times \text{sqc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \quad 6-10$$

It can be seen that e_{τ^*} tends to zero as $\text{Trs}(\hat{\tau}^* - \tau)$ tends to zero, which occurs at integer n multiples of sub-chips as $\hat{\tau}^* \rightarrow \tau + n \times T_s$. Alternative coherent SLL discriminators for the DE BOC receiver are shown in Table 6-2.

Table 6-2, SLL discriminators for the DE BOC receiver

Discriminator	Error signal	Dependency
Decision-corrected	$e_{\tau^*} = w_{IQI} \times \text{sgn}(w_{III})$ $\approx A \times \cos(\phi - \hat{\phi}) \times \text{Trs}(\hat{\tau}^* - \tau) \times \text{sqc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A
Dot product	$e_{\tau^*} = w_{IQI} \times w_{III}$ $\approx A^2 \times \cos^2(\phi - \hat{\phi}) \times \text{Trs}(\hat{\tau}^* - \tau) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda^2(\hat{\tau} - \tau)$	Slope proportional to A^2
Normalised	$e_{\tau^*} = w_{IQI} / w_{III}$ $\approx \frac{\text{Trs}(\hat{\tau}^* - \tau)}{\text{trc}(\hat{\tau}^* - \tau)} = \text{Trt}(\hat{\tau}^* - \tau)$	Slope independent of amplitude

The code phase error for the coherent DE BOC receiver can also be determined using a decision-directed discriminator as follows.

$$e_\tau = w_{IIQ} \times \text{sgn}(w_{III}) \approx A \times |\cos(\phi - \hat{\phi})| \times |\text{trc}(\hat{\tau}^* - \tau)| \times V^\Lambda (\hat{\tau} - \tau) \quad 6-11$$

It can be seen that e_τ tends to zero as $V^\Lambda(\hat{\tau} - \tau)$ tends to zero, which occurs as $\hat{\tau} \rightarrow \tau$. Alternative coherent DLL discriminators for the DE BOC receiver are shown in Table 6-3.

Table 6-3, Coherent DLL discriminators for the DE BOC receiver

Discriminator	Error signal	Dependency
Decision-corrected	$e_\tau = w_{IIQ} \times \text{sgn}(w_{III})$ $\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times V^\Lambda (\hat{\tau} - \tau)$	Slope proportional to A
Dot product	$e_\tau = w_{IIQ} \times w_{III}$ $\approx A^2 \times \cos^2(\phi - \hat{\phi}) \times \text{trc}^2(\hat{\tau}^* - \tau) \times V^\Lambda (\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A^2
Power	$e_\tau = w_{IE}^2 - w_{IL}^2$ $\approx A^2 \times \cos^2(\phi - \hat{\phi}) \times \text{trc}^2(\hat{\tau}^* - \tau) \times \left(\Lambda^2 \left(\hat{\tau} - \frac{T_{DC}}{2} - \tau \right) - \Lambda^2 \left(\hat{\tau} + \frac{T_{DC}}{2} - \tau \right) \right)$	Slope proportional to A^2

Following common practice we update the carrier phase estimate with a second order loop as follows.

$$\begin{aligned} f_\phi &\leftarrow f_\phi + e_\phi \\ \hat{\phi} &\leftarrow \hat{\phi} + k_1 \times f_\phi + k_2 \times e_\phi \end{aligned} \quad 6-12$$

f_ϕ is the integrated phase error and k_1 and k_2 are loop gains which can be adjusted by the designer. The SLL and DLL loop are updated with independent first order loops for the sub-carrier and code delay estimates respectively with an appropriate carrier aiding term as follows.

$$\begin{aligned} \hat{\tau} &= \hat{\tau} + k_\phi \times f_\phi + k_\tau \times e_\tau \\ \hat{\tau}^* &= \hat{\tau}^* + k_{\phi^*} \times f_\phi + k_{\tau^*} \times e_{\tau^*} \end{aligned} \quad 6-13$$

k_ϕ and k_{ϕ^*} are constants calculated to provide the necessary open loop correction of Doppler shift appropriately scaled down to the code rate and sub-carrier rate respectively. k_τ and k_{τ^*} are a loop gains which can be adjusted by the designer.

Assuming the loops are in lock the data estimate, \hat{d} for a coherent DE BOC receiver is determined as follows.

$$\hat{d} = \text{sgn}(w_{III}) \quad 6-14$$

An example acquisition of the DE BOC receiver is shown in Figure 6-6 for a BOC($2 \times f_C, f_C$) signal, derived from Mathcad simulation with equal DLL and SLL loop bandwidths, $B_{DLL} = B_{SLL} = 1$ Hz and noise, $C/N_0 = 30$ dB-Hz. The initial delay offset is set at 2.5 sub-chips and initial phase error of $\pi/4$.

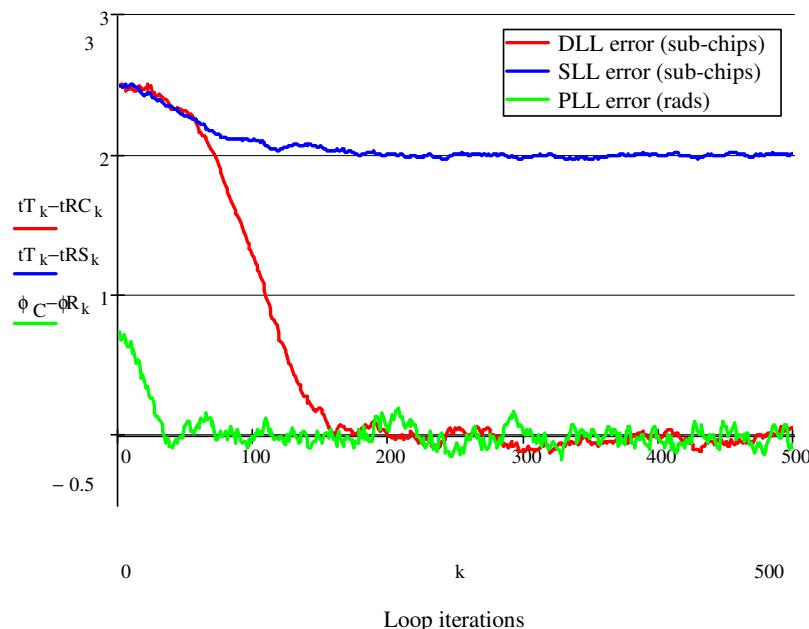


Figure 6-6, Example acquisition of the DE BOC receiver ($B_{DLL} = B_{SLL} = 1$ Hz, $C/N_0 = 30$ dB-Hz)

Under loop operations the DLL delay estimate provides unambiguous tracking with timing jitter equivalent to that of the underlying PSK modulation (see Equation 4-16). The SLL delay estimate $\hat{\tau}^*$ delivers the full tracking accuracy of the BOC modulation given by Equation 4-20, it is however ambiguous, locking to integer sub-chip values.

Once the loops have settled the ambiguity of the SLL estimate can be resolved through the noisier but unambiguous DLL estimate as follows.

$$\hat{\tau}^+ = \hat{\tau}^* - \text{round}\left(\frac{\hat{\tau}^* - \hat{\tau}}{T_s}\right) \times T_s \quad 6-15$$

$\hat{\tau}^+$ is the corrected delay estimate. Figure 6-7 shows an example acquisition with the corrected delay estimate.

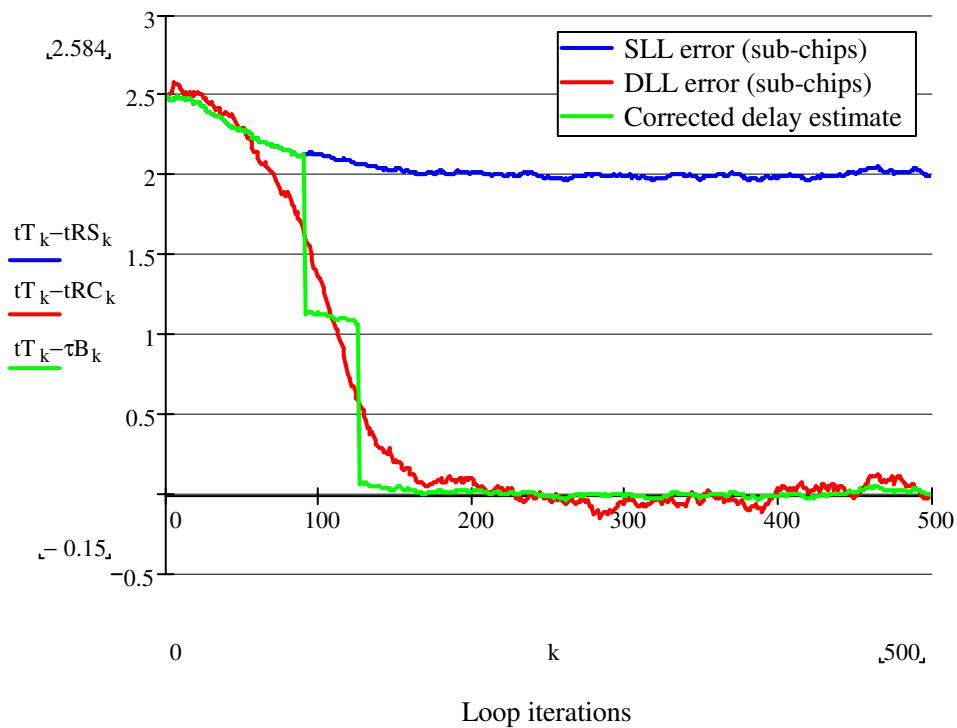


Figure 6-7, Corrected delay estimate of the DE BOC receiver

($B_{DLL} = B_{SLL} = 1 \text{ Hz}$, $C/N_0 = 30 \text{ dB-Hz}$)

6.2 The incoherent BOC double estimator

Incoherent systems are commonly used to deliver robust acquisition and tracking of GNSS signals, particularly in weak signal environments. An incoherent system locks on to the frequency of the incoming carrier and not the phase. This is achieved by maintaining a constant or near constant carrier phase difference across the correlation interval. The concept of double estimation, generating sub-carrier and code waveforms with independent timing estimates can still be applied. A general

schematic of the DE BOC receiver is shown in Figure 6-8. Two additional correlations are required to enable all three loops to operate with no carrier phase dependence.

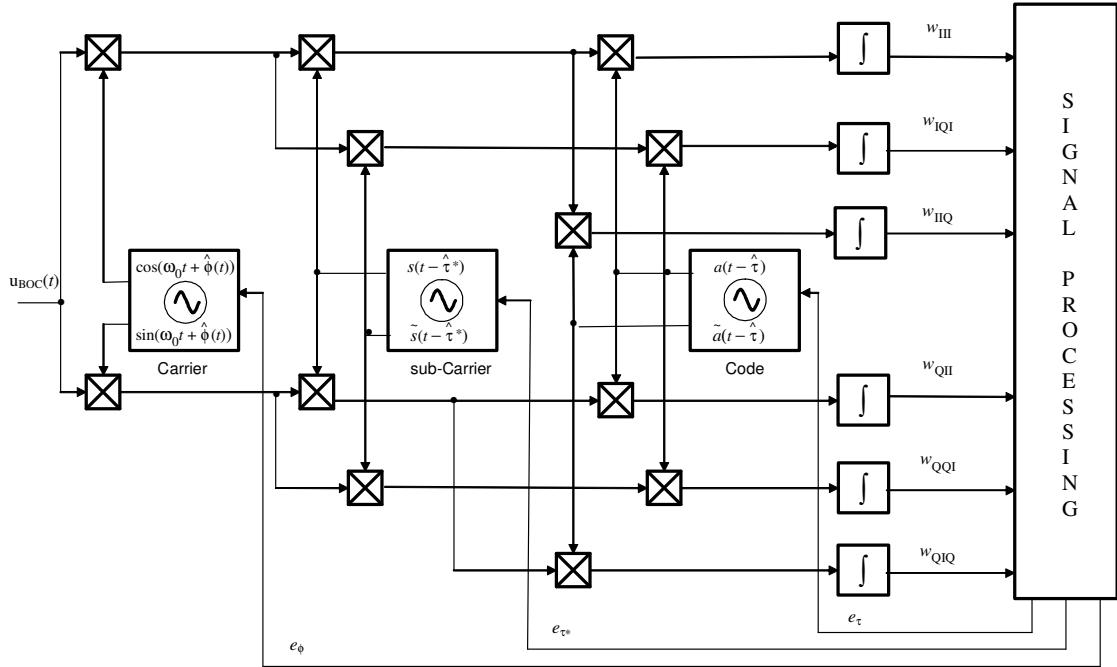


Figure 6-8, Incoherent DE BOC receiver

After mixing and integration over time T the additional two correlations required for an incoherent DE BOC receiver can be written as follows.

$$\begin{aligned}
 w_{QIQ} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \sin(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}^*) \times \tilde{a}(t - \hat{\tau}) dt \\
 &\approx A \times \sin(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times V^\Lambda(\hat{\tau} - \tau) \times d \\
 w_{QQI} &= \frac{1}{T} \int_0^T u_{BOC}(t) \times \sin(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}^*) \times a(t - \hat{\tau}) dt \\
 &\approx A \times \sin(\phi - \hat{\phi}) \times \text{Trs}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d
 \end{aligned} \tag{6-16}$$

The rate of change of carrier phase can be determined by comparing w_{III} and w_{QII} with the correlation results from the next epoch w_{III}' and w_{QII}' . The frequency error can be determined using the cross-product discriminator as follows.

$$e_\omega = w'_{QII} \times w_{III} - w'_{III} \times w_{QII} \approx A^2 \times \sin(\Delta\hat{\phi} - \Delta\phi) \times \text{trc}^2(\hat{\tau}^* - \tau) \times \Lambda^2(\hat{\tau} - \tau) \times d \times d' \quad \text{6-17}$$

Where the phase difference and estimated phase difference between epochs is

$$\begin{aligned} \Delta\phi &= \phi' - \phi \\ \Delta\hat{\phi} &= \hat{\phi}' - \hat{\phi} \end{aligned} \quad \text{6-18}$$

It can be seen that e_ω tends to zero with $\Delta\hat{\phi} - \Delta\phi$. Incoherent SLL tracking can be achieved by expanding the decision directed discriminator as follows.

$$\begin{aligned} e_{\tau^*} &= w_{IQI} \times \text{sgn}(w_{III}) + w_{QQI} \times \text{sgn}(w_{QII}) \\ &\approx A \times (\cos(\phi - \hat{\phi}) + |\sin(\phi - \hat{\phi})|) \times \text{Trs}(\hat{\tau}^* - \tau) \times \text{sqc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \end{aligned} \quad \text{6-19}$$

It can be seen that e_{τ^*} tends to zero as $\text{Trs}(\hat{\tau}^* - \tau)$ tends to zero, which occurs at integer n multiples of sub-chips as $\hat{\tau}^* \rightarrow \tau + n \times T_s$. This is achieved while allowing for an arbitrary offset between ϕ and $\hat{\phi}$. Incoherent DLL tracking can be achieved by expanding the decision directed discriminator as follows.

$$\begin{aligned} e_\tau &= w_{IIQ} \times \text{sgn}(w_{III}) \times w_{QIQ} \times \text{sgn}(w_{QII}) \\ &\approx A \times (\cos(\phi - \hat{\phi}) + |\sin(\phi - \hat{\phi})|) \times |\text{trc}(\hat{\tau}^* - \tau)| \times V^\Lambda(\hat{\tau} - \tau) \end{aligned} \quad \text{6-20}$$

It can be seen that e_τ tends to zero as $V^\Lambda(\hat{\tau} - \tau)$ tends to zero, which occurs as $\hat{\tau} \rightarrow \tau$.

For updating the loops we assume second-order FLL tracking and first order SLL and DLL tracking with appropriate carrier Doppler aiding as follows.

$$\begin{aligned}
e_\phi &\leftarrow e_\phi + e_\omega & 6-21 \\
f_\phi &\leftarrow f_\phi + e_\phi \\
\hat{\phi} &\leftarrow \hat{\phi} + k_1 \times f_\phi + k_2 \times e_\phi & \text{FLL update} \\
\hat{\tau}^* &\leftarrow \hat{\tau}^* + k_{\phi^*} \times f_\phi + k_{\tau^*} \times e_{\tau^*} & \text{SLL update} \\
\hat{\tau} &\leftarrow \hat{\tau} + k_\phi \times f_\phi + k_\tau \times e_\tau & \text{DLL update}
\end{aligned}$$

e_ϕ is the estimated phase error derived by the integrating frequency error e_ω , k_1 and k_2 are loop gains which can be adjusted by the designer. Figure 6-9 shows the convergence of all three of the DE loops with an initial frequency error of 1 radian per code epoch and a two sub-chip error on the SLL estimate. The DLL estimate is then used to correct the SLL estimate in exactly the same way as the coherent DE BOC receiver (Equation 6-15).

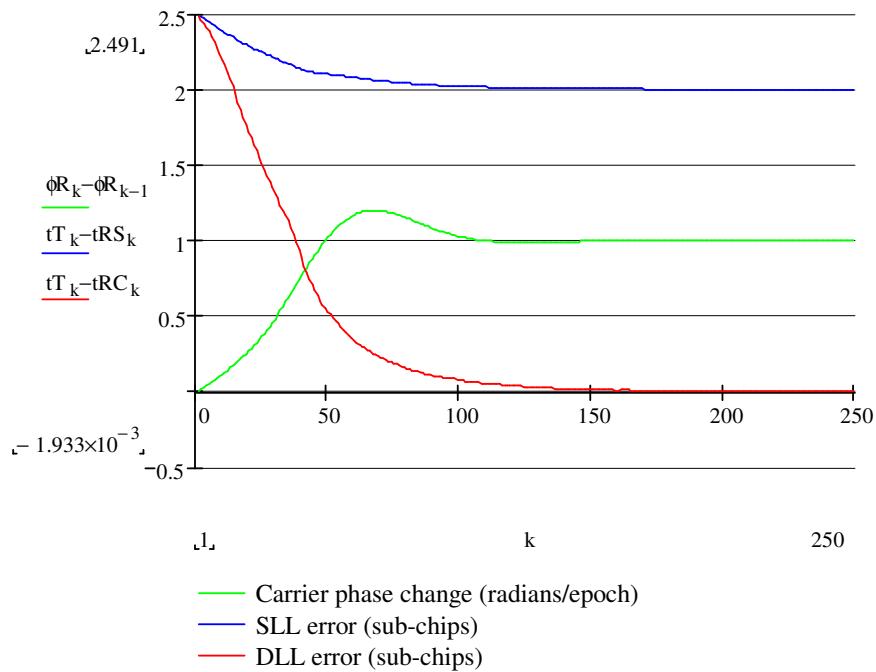


Figure 6-9, Example incoherent acquisition $\Delta\phi = 1 \text{ rad}$

6.3 The DE AltBOC receiver

The extension of DE principle to Alternate BOC (AltBOC) signals provided by Dr MS Hodgart requires little change to the theory of the DE BOC receiver. An AltBOC(15, 10) signal modulation is intended to combine four PRN code signals in

the Galileo E5 band. Omitting the data modulation for simplicity the AltBOC signal can be written as follows.

$$\begin{aligned} u_{\text{AltBOC}}(t) = & A_1 \times [a_1(t-\tau) + a_2(t-\tau)] \times s(t-\tau) \times \cos(\omega_c t + \phi) + \\ & A_1 \times [a_1(t-\tau) - a_2(t-\tau)] \times \tilde{s}(t-\tau) \times \sin(\omega_c t + \phi) + \\ & A_2 \times [a_3(t-\tau) + a_4(t-\tau)] \times \tilde{s}(t-\tau) \times \cos(\omega_c t + \phi) - \\ & A_2 \times [a_3(t-\tau) - a_4(t-\tau)] \times s(t-\tau) \times \sin(\omega_c t + \phi) \end{aligned} \quad \text{6-22}$$

The upper and lower sidebands of the AltBOC signal can be individually processed as separate PSK signals because the code combinations modulate separate upper and lower side bands respectively. However, to achieve the full potential of this wideband modulation the full bandwidth must be processed. Tracking the full AltBOC modulation can be achieved using either the sum of the $a_1()$ and $a_2()$ codes or the sum of the $a_3()$ and $a_4()$ codes. Correlating the sum of the $a_3()$ and $a_4()$ codes the resulting correlations for a coherent DE AltBOC receiver are as follows.

$$\begin{aligned} w_{III} &= \frac{1}{T} \int_0^T u_{\text{AltBOC}}(t) \times \cos(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}^*) \times [a_3(t - \hat{\tau}) + a_4(t - \hat{\tau})] dt \\ &\approx 2A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\ w_{IIQ} &= \frac{1}{T} \int_0^T u_{\text{AltBOC}}(t) \times \cos(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}^*) \times [\tilde{a}_3(t - \hat{\tau}) + \tilde{a}_4(t - \hat{\tau})] dt \\ &\approx 2A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\ w_{IQI} &= \frac{1}{T} \int_0^T u_{\text{AltBOC}}(t) \times \cos(\omega_0 t + \hat{\phi}) \times s(t - \hat{\tau}^*) \times [a_3(t - \hat{\tau}) + a_4(t - \hat{\tau})] dt \\ &\approx 2A \times \cos(\phi - \hat{\phi}) \times \text{Trs}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \\ w_{QII} &= \frac{1}{T} \int_0^T u_{\text{AltBOC}}(t) \times \sin(\omega_0 t + \hat{\phi}) \times \tilde{s}(t - \hat{\tau}^*) \times [a_3(t - \hat{\tau}) + a_4(t - \hat{\tau})] dt \\ &\approx 2A \times \sin(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \end{aligned} \quad \text{6-23}$$

These correlations provide equivalent error signals to the DE BOC receiver allowing control of all three loops into lock. The SLL delay estimate can then be corrected by the DLL estimate as in Equation 6-15.

6.4 Simulated performance of DE BOC

In Section 5.4 a comparison of the BOC tracking techniques in the literature is given. From this analysis, a design trade-off is identified between receiver settling time and timing jitter of the delay estimate. Techniques approximating a PSK single correlation peak provide an unambiguous rapid loop settling time but at the cost of significantly worse receiver timing jitter. Other techniques, such as the BJ algorithm can provide the full potential of BOC tracking precision but suffer in terms of loop settling times.

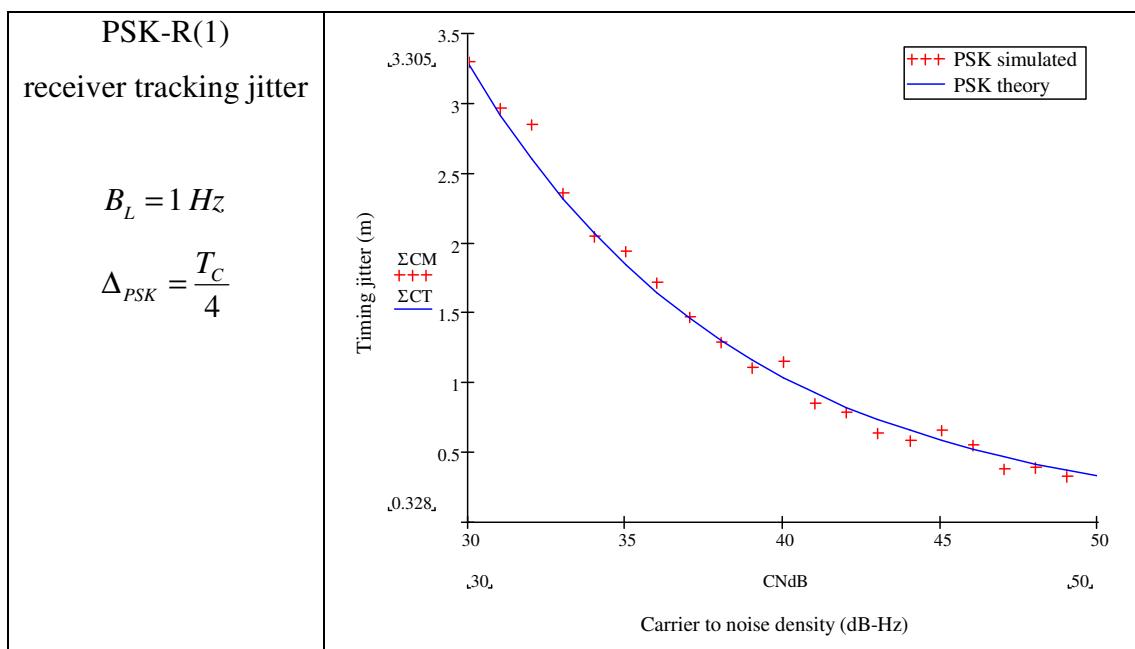
The DE BOC receiver is believed to provide the best of both worlds, an unambiguous rapid loop settling time while providing the full timing precision available from the BOC characteristic. The settling time of the DLL loop follows the desirable single correlation peak synonymous with PSK modulation, while the SLL loop simply settles to the nearest sub-chip offset. The maximum precision of the BOC modulation is then achieved by correcting the SLL estimate using the DLL estimate as in Equation 6-15.

From Section 5.4 the SSB technique has been shown to provide the best acquisition performance and the BJ algorithm the best timing precision. Table 6-4 shows the acquisition times of the DE BOC receiver in comparison to the SSB technique and BJ algorithm. We are assuming a BOC(6, 1) signal, a carrier to noise density of $C/N_0 = 24$ dB-Hz, equal DLL and SLL loop bandwidths of $B_{DLL} = B_{SLL} = 1$ Hz and averaging across 20 acquisitions at each time step. The DE BOC receiver is shown to deliver acquisition speed equivalent to that of the SSB technique.

Table 6-4, Acquisition times of the DE BOC receiver, BJ algorithm and the SSB technique for BOC(6, 1), $B_L = 1 \text{ Hz}$, $C/N_0 = 24 \text{ dB-Hz}$

Initial chip offset	1/12	2/12	3/12	4/12
DE BOC acquisition time (ms)	272	523	620	776
BJ acquisition time (ms)	1009	2327	3481	4754
SSB acquisition time (ms)	276	527	611	736
DE / SSB	0.99	0.99	1.01	1.05
BJ / SSB	3.65	4.42	5.69	6.46

Using Mathcad simulations we can evaluate the timing jitter of the DE in the presence of additive Gaussian noise and give comparisons with the theoretical equations given in Chapter 4. In all cases we simulate a ‘spacing-limited’ receiver. Figure 6-10 shows the theoretical and simulated timing jitter for PSK and DE BOC receivers across carrier to noise densities from 30 to 50 dB-Hz. We find strong agreement with the theoretically derived equations, proving that the precision of DE BOC tracking delivers the full potential accuracy of BOC modulation.



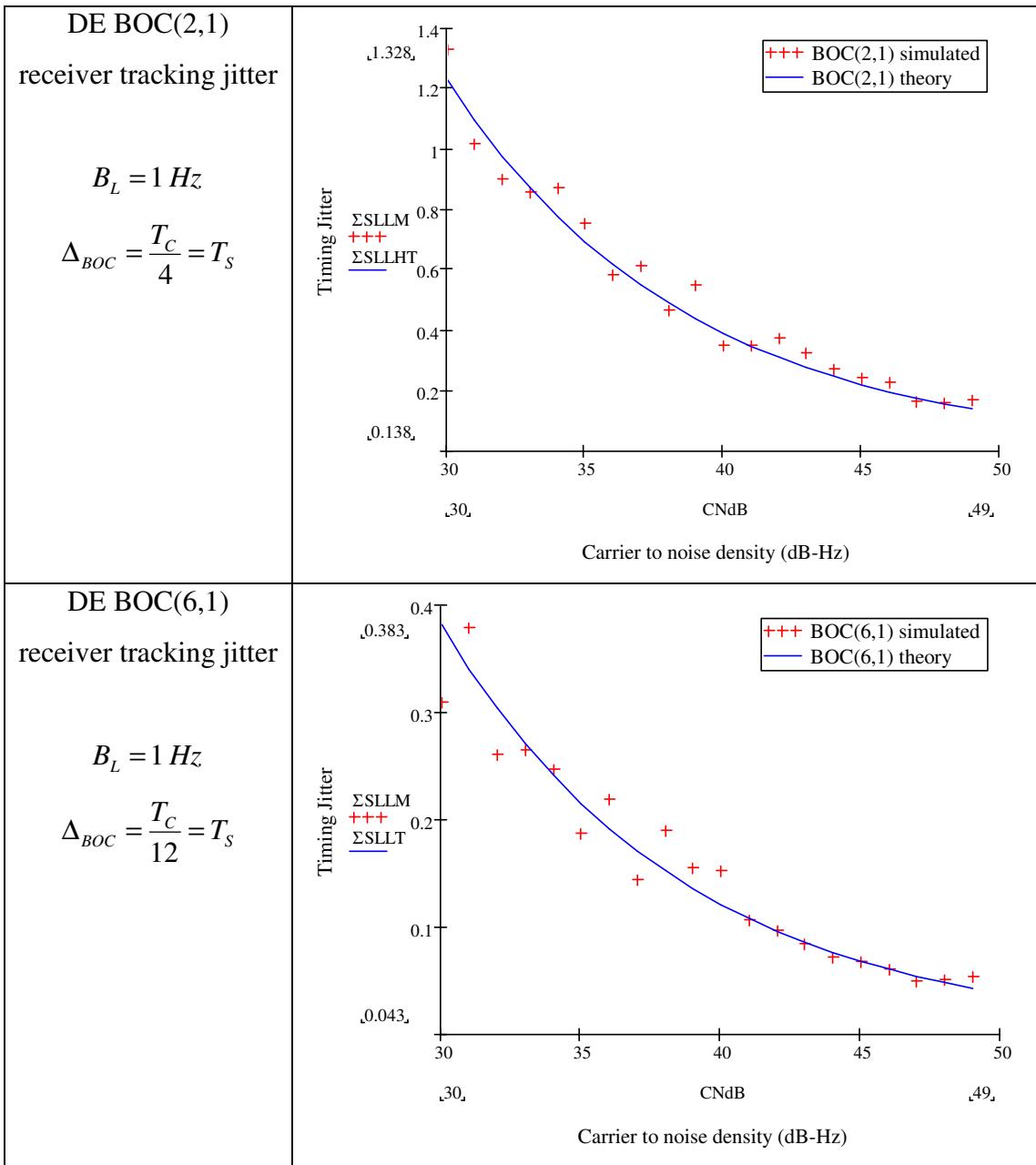


Figure 6-10, Simulations of PSK and DE BOC timing jitter with comparison to theory

Another key performance measure of particular interest is that of the multipath performance of the DE BOC receiver. As shown in Section 4.5 the simplest method of evaluating the multipath error performance is to consider the effect of a single interfering multipath signal with various relative time delays. This provides only a worse case analysis of error due to multipath but does provide an adequate performance measure with which we can compare BOC tracking schemes. The result of this analysis is a multipath error envelope which for conventional receivers is dependant on the correlation function and the type of discriminator implemented for

code tracking. Therefore, to provide a fair comparative basis on which to evaluate multipath error envelopes it is important to set equal discriminator spacing.

Figure 6-11 shows the multipath error envelopes of a conventional BOC receiver and the DE BOC receiver for a BOC(2,1) signal. The DE BOC error envelope is computed by analyzing the error of the corrected SLL delay estimate with multipath interference. The relative performance of each scheme can be seen by computing the running average error across the dataset, shown in Figure 6-12. The pattern of the DE BOC multipath envelope broadly follows that of the conventional receiver but does show a small improvement (8.2%) across the whole dataset.

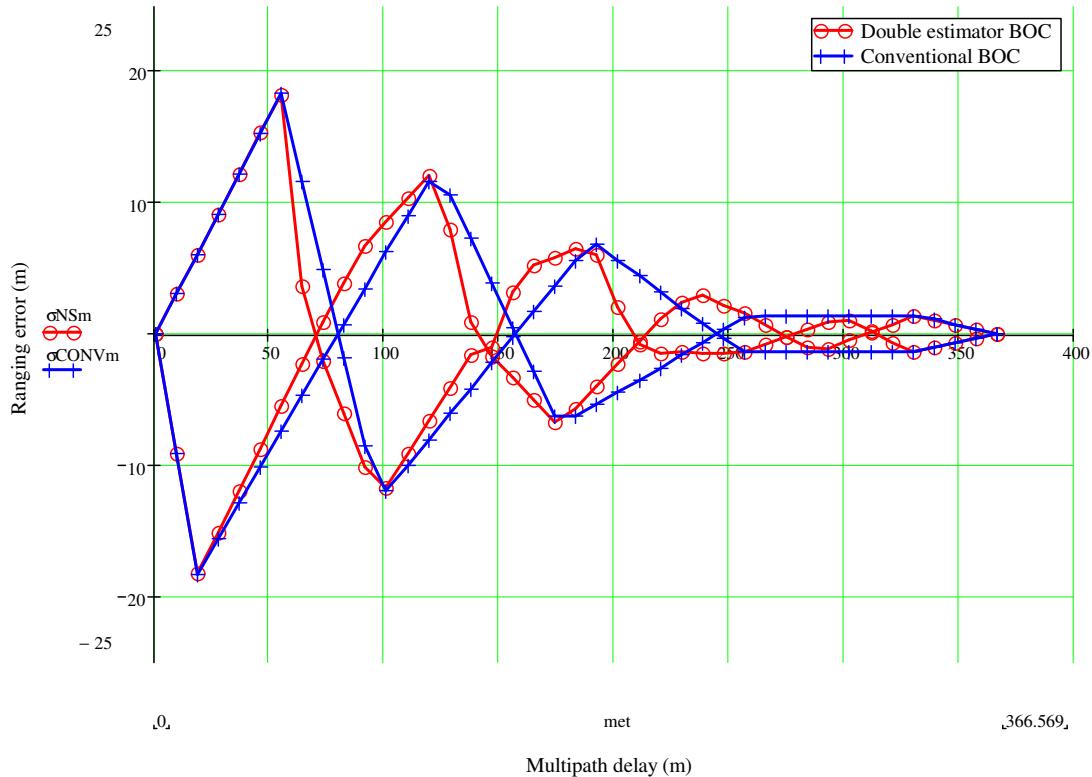


Figure 6-11, Multipath error envelope of a conventional and DE BOC receiver,

$$\text{BOC}(2,1) \Delta_{BOC} = T_s$$

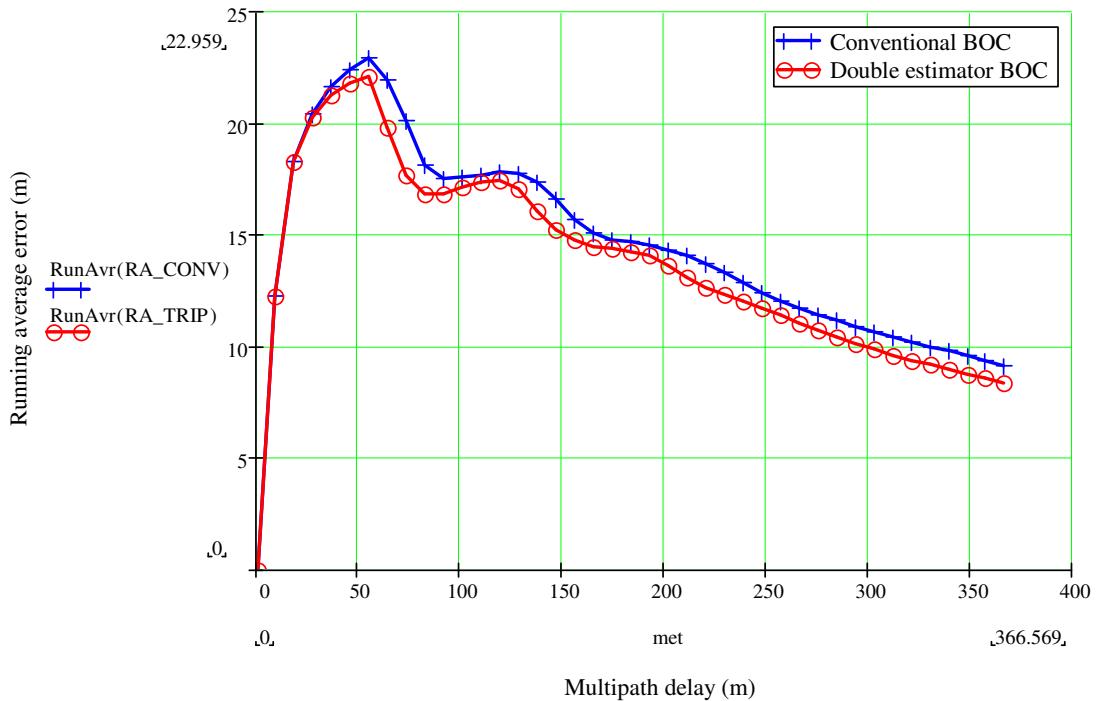


Figure 6-12, Running average multipath error of a conventional and DE BOC receiver

$$\text{BOC}(2,1) \Delta_{BOC} = T_s$$

6.5 The effect of asymmetry

In contrast to the BJ algorithm, asymmetry in the received signal is not believed to pose a severe problem for the DE BOC receiver. This is because a DE BOC receiver does not rely on peak discrimination and tracks the sub-carrier of the incoming signal independently of the code. The DE BOC receiver has no false-lock conditions because sub-chip offsets are automatically accounted for in the corrected delay estimate. Therefore, asymmetry has no significant effect on the integrity or acquisition performance of the DE BOC receiver.

Figure 6-13 shows an example acquisition of the DE BOC receiver with a distorted signal created by introducing a quarter sub-chip offset between the sub-carrier and the code in the received signal. The received code delay is set to $-1/4$ of a sub-chip. Therefore, the SLL estimate is biased from the correct delay. However, the effect of the sub-carrier is removed from the DLL loop which therefore converges to the correct timing location. The SLL bias can be calibrated and corrected by using the DLL estimate, which is assumed to be correct. The bias in the BJ algorithm can only

be resolved if the receiver has the capability of receiving other signals from the same satellite or through a complex calibration campaign.

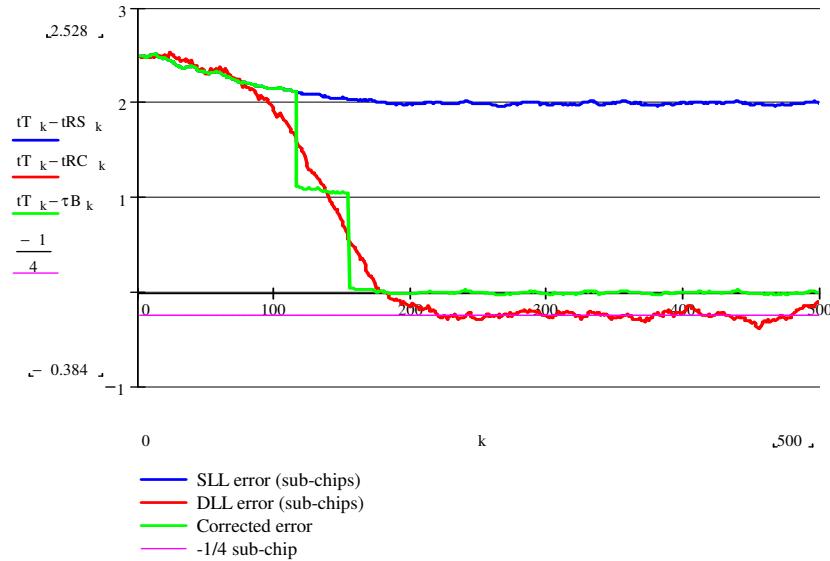


Figure 6-13, Example acquisition of the DE BOC receiver with asymmetric correlation, BOC(2,1), $C/N_0 = 24\text{dB-Hz}$, sub-carrier to code offset = $T_S / 4$

The DE BOC receiver can very accurately measure the sub-carrier to code offset, in order to correct for asymmetry in the received signal. This is achieved simply by averaging the difference between SLL and DLL estimates to remove timing jitter. An example of receiver calibration for asymmetric signals is shown in Section 9.2. Although calibration of the receiver tracking bias for the BJ algorithm is possible, it is certainly more complicated to achieve than calibration of the DE BOC receiver. This combined with the risk to BJ receiver integrity proves the DE BOC receiver to be the preferred choice, particularly for BOC transmissions with high ratios of sub-carrier frequency to code rate.

Further detailed work is continuing at SSTL in order to demonstrate the advantages of the DE BOC receiver with the significantly distorted BOC(15,2.5) signal from Giove-A.

6.6 Integrity of the DE BOC receiver

The DE BOC receiver provides two independent estimates of the incoming signal delay. These estimates can be used to improve the integrity of the receiver's tracking. This is of particular interest in the use of BOC receivers for safety critical

applications, where an incorrect tracking state due to a signal dropout or slip in BOC receiver tracking could have catastrophic results.

The receiver estimated signal to noise ratio is used to indicate when a receiver has lost lock on the incoming signal. An example of a signal drop out from an SNR of 15dB is shown in Figure 6-14. The raw SNR values are filtered in the receiver to avoid dropping the signal while tracking in weak signal conditions. This example uses the SSTL SGR receiver's SNR filter and loss of lock threshold (3dB). The receiver declares loss of lock almost half a second after the actual dropout has occurred due to the effect of the SNR filtering.

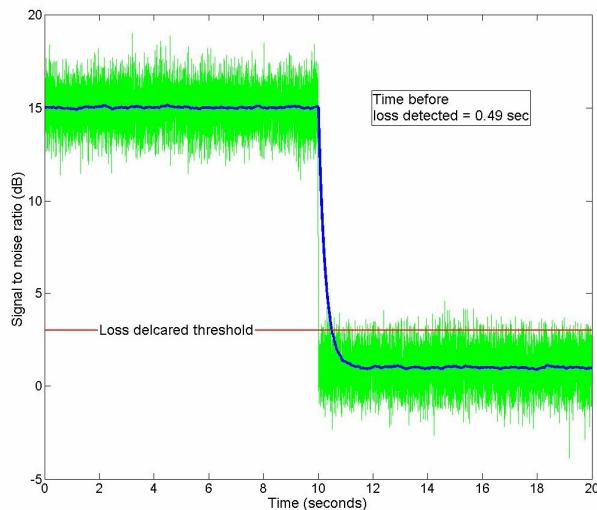


Figure 6-14, Loss of lock from 15 dB SNR (SGR filter)

A slip to an incorrect BOC tracking state cannot be reliably detected using the change in the receiver estimated SNR. This is because the difference in peak amplitude from the central BOC peak to its adjacent peak can be as small as 0.75 dB for a $\text{BOC}(6 \times f_C, f_C)$ modulation. This small variation in SNR takes a significant amount of filtering resulting in a long time to detect an invalid tracking state. In addition, a 0.75 dB variation in SNR could easily occur through variations in the receiver environment, multipath or antenna pattern under dynamics.

Figure 6-15 provides an illustration of SNR estimation of a single sub-chip slip after a 100ms signal outage. After the outage the receiver locks onto an invalid timing location with only a small SNR difference (0.75 dB).

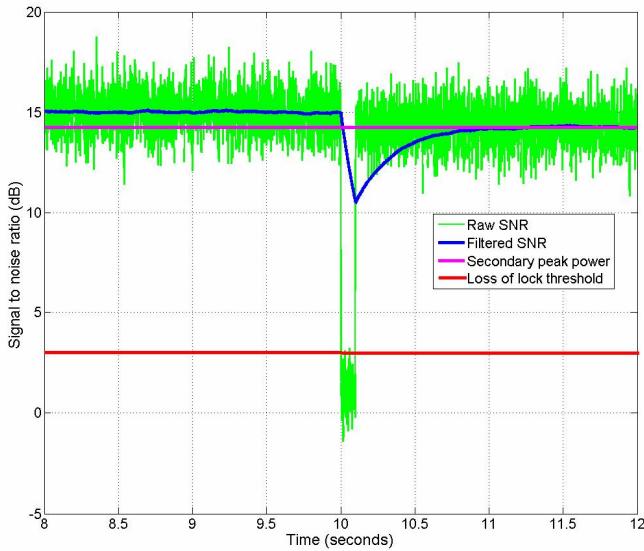


Figure 6-15, Example of receiver SNR estimation of a slip in tracking

The BJ algorithm provides a method by which a receiver can detect a false tracking condition. However, the relative peak values also require a significant amount of filtering in order to make a correct decision in the presence of noise. As shown in Chapter 5.4 the BJ algorithm takes 303 ms to detect a slip in tracking for a $\text{BOC}(2 \times f_c, f_c)$ modulation and 810 ms for a $\text{BOC}(6 \times f_c, f_c)$ modulation. Hence, BOC receivers using the BJ algorithm can be in a false lock condition for a significant amount of time before it can detect it.

False lock in a BOC receiver causes significant errors in the receiver's position estimate. For example when attempting to receive a $\text{BOC}(15, 2.5)$ modulated signal, false lock conditions can cause errors ranging from a minimum of 10 m to greater than 100 m in the worse case. Therefore, the BJ algorithm is essentially an *aposteriori* test because it must maintain a false condition for an amount of time before detection and potential correction of invalid tracking is possible. In our opinion the BJ algorithm is therefore unsafe for safety critical applications where the integrity of the receiver's tracking is of vital importance.

The existence of two estimates of the received signal delay present in the DE BOC receiver solves the problem of integrity in a BOC receiver. There are no false lock or invalid tracking states when operating the DE BOC receiver. The SLL settles to

integer sub-chip offsets from the correct, valid delay estimate. The delay estimate derived from the DLL allows correction of the SLL delay estimate wherever the SLL has settled to. Therefore, the DE BOC receiver corrected delay estimate, $\hat{\tau}^+$ is instantaneously corrected for tracking slips of integer sub-chips and the integrity of the receiver is never compromised.

6.7 Hardware requirements of the DE BOC receiver

The simplicity of the DE BOC receiver architecture provides an attractive choice of the GNSS receiver designer. The DE BOC receiver provides correlator architecture compatible with the leading unambiguous BOC search technique with no changes required to the receiver hardware. By locking the sub-carrier delay estimate $\hat{\tau}^*$ to the code estimate $\hat{\tau}$ during search (i.e. aligned code and sub-carrier) the preferred SCC search technique can be implemented (see Section 5.3). All other proposed BOC tracking techniques will require additional hardware resources to become compatible with the SCC BOC search technique.

The correlator hardware required for the leading BOC tracking techniques are shown in Table 6-5. The DE BOC receiver and BJ algorithm are both considerably more efficient with a receiver's hardware resource. The DE receiver uses two additional multipliers and an additional local oscillator when compared to the BJ algorithm. However, the additional multipliers are one-bit and therefore the limiting factor in designs will be the number of storage elements used (integrators). The DE receiver uses two less integrators per channel than the BJ algorithm and hence provides the most efficient use of hardware. An example of hardware resource utilization in a prototype DE BOC receiver is given in Section 8.4.

Table 6-5, Hardware requirements of BOC tracking techniques

Receiver type	Multipliers	Integrators	Local oscillators	Low pass filters
SSB	2×Carrier, 4×Code	4	1×Carrier, 1×Code	2
MGD (N=4)	2×Carrier, 18×Code	18	1×Carrier, 1×Code	0
BJ	2×Carrier, 8×Code	8	1×Carrier, 1×Code	0
DE	2×Carrier, 4×Sub-carrier, 6×Code	6	1×Carrier, 1×Sub-carrier, 1×Code	0

6.8 Summary of the advantages of a DE BOC receiver

As detailed in this chapter the concept of independently tracking the incoming sub-carrier and code provides a number of performance advantages over the BOC tracking schemes given in the literature. These advantages can be summarized as follows.

- Rapid, smooth and reliable acquisition performance – The DE BOC receiver completely removes the BOC ambiguity providing rapid acquisition equivalent to that of a PSK receiver.
- Precise timing jitter – Combining independent delay estimates from its SLL and DLL the DE BOC receiver provides unambiguous BOC tracking with precision equivalent to tracking using traditional early-late gates. In [Bello and Fante 2005] the BJ algorithm [Fine and Wilson 1999] is shown to be the only other BOC tracking technique which results in no degradation of tracking jitter from early-late gates.
- No integrity issues – The DE BOC receiver provides unambiguous BOC tracking without relying on a peak detection (BJ algorithm) which requires careful threshold tuning. This provides a more robust design which can easily be corrected for distortions (asymmetry) in the transmitted signal.
- Automatic slip correction – The DE BOC receiver maintains a valid delay estimate for any sub-chip offset within the correlation interval. This removes the risk of maintaining a false-lock condition for a significant period before correction.

- Lowest hardware utilization – The DE BOC receiver provides the most efficient use of hardware resources compared to other unambiguous BOC tracking techniques.

7 GNSS signal generators and the Giove-A satellite

In this chapter we discuss hardware implementations of GNSS signal generators. The mission and payload of the Giove-A satellite is summarised with emphasis given to the SSTL built Galileo signal generator that this research has contributed towards. The design of a prototype IF GNSS signal generator is then detailed. Stemming from the original SSTL design, this signal generator has the added capability of synthesizing additive noise to the IF signal. These signal generators will be used to demonstrate and evaluate receiver performance in Chapter 9. The receiver testing using the Galileo signals from the Giove-A satellite is described in Chapter 10.

7.1 The Giove-A mission and payload

On the 11 July 2003 SSTL was awarded a 28 million euro contract to construct the first Galileo test-bed satellite Giove-A. The Giove-A satellite was successfully launched on the 28th of December 2005 from the Baikonur Cosmodrome in Kazakhstan, via a Starsem Soyuz-Fregat rocket (see Figure 7-1). Giove-A is the first SSTL mission outside low earth orbit (LEO) and was placed in a high-radiation environment at 24,000 km altitude with a 14-hour orbit. The satellite weighs in at 660 kg is 3-axis stabilisation and dimensions of 1.3 m (height) × 1.8 m (width) × 1.65 m (depth). Two sun-tracking solar arrays each 1.74 m long provide 700 Watts of electrical power to the payload.

The primary mission objectives of Giove-A were to secure the Galileo frequency filings and validate key technologies for the final Galileo constellation. The satellite carries an environmental payload to measure the radiation and spacecraft charging experienced in the Galileo orbit. Also on-board is a experimental GPS receiver manufactured by SSTL to demonstrate operation outside the GPS constellation.



Figure 7-1, Giove-A satellite: a) at ESA for environmental testing b) on the launch pad

The payload of the Giove-A satellite is shown in Figure 7-2. The primary payload is a fully space qualified signal generator commissioned by ESA. Driven by one of two rubidium atomic clocks this payload is capable of producing representative Galileo signals in three frequency bands (E1, E5, E6) although only two bands may be transmitted at any particular time. The space-qualified units were sourced by ESA and are referred to as ‘customer furnished items’ (CFI). In order to remove the schedule risk of the CFI Galileo signal generator, SSTL supplied a backup Galileo signal generator based on commercial off-the-self (COTS) components. This development consists of the navigational message generation unit (NMGU) and the modulator, frequency generator and up-converter unit (MFUU). Both units are driven by a 10.23MHz reference derived from the atomic clocks.

The NMGU controls the synchronised start of signal transmission with Galileo time and provides the navigational message data for all signals being transmitted. The MFUU generates representative Galileo spreading codes and sub-carrier modulations (BOC) synchronised with the incoming navigational data and up-converts the signal to RF. The MFUU is capable of producing representative Galileo signals in three frequency bands (E1, E5, E6), although only two bands may be transmitted at any particular time.

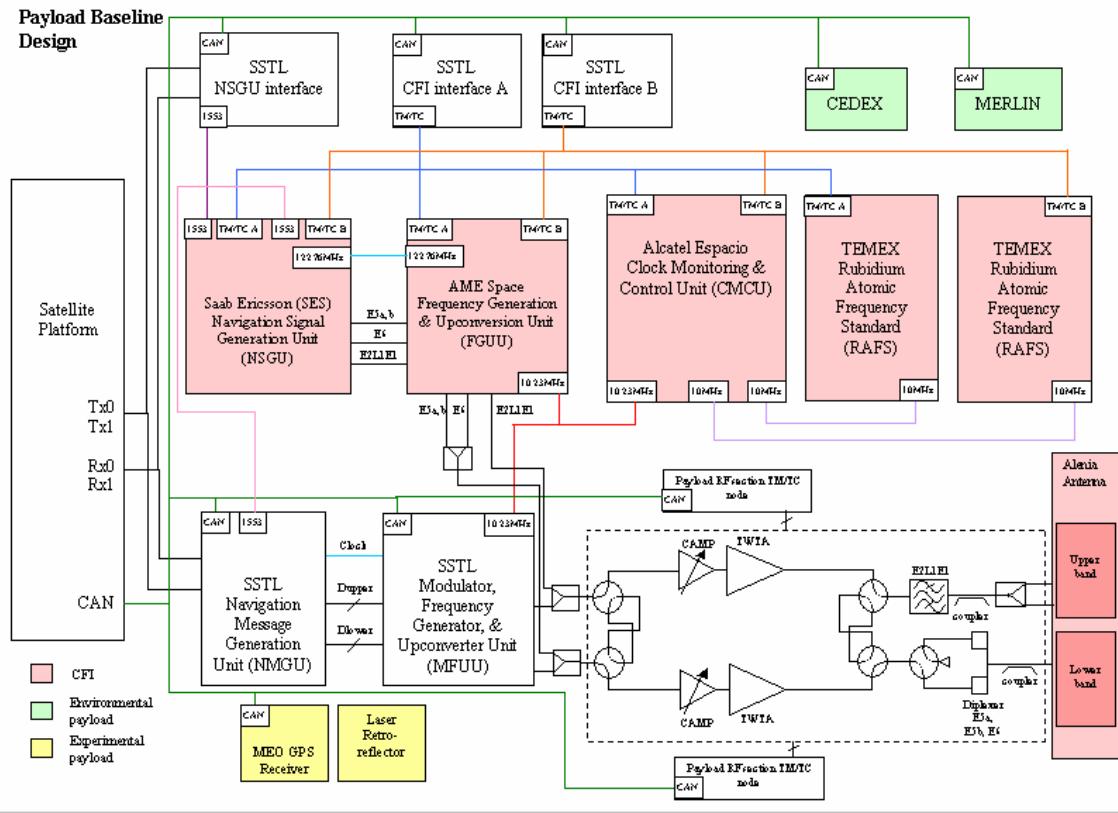


Figure 7-2, Baseline payload design for Giove-A [Falcone *et al* 2006]

The MFUU consists of a modulator and two up-converter units, shown in Figure 7-3. The modulator consists of a single radiation tolerant Actel RT54SX72S field programmable gate array (FPGA) and two Analog Devices AD9755 digital-to-analog converters (DAC), which were radiation tested. The Galileo signal at the DAC output is centred at an Intermediate Frequency (IF) of 61.38 MHz, which is then up-converted and filtered to its respective signal bandwidth.

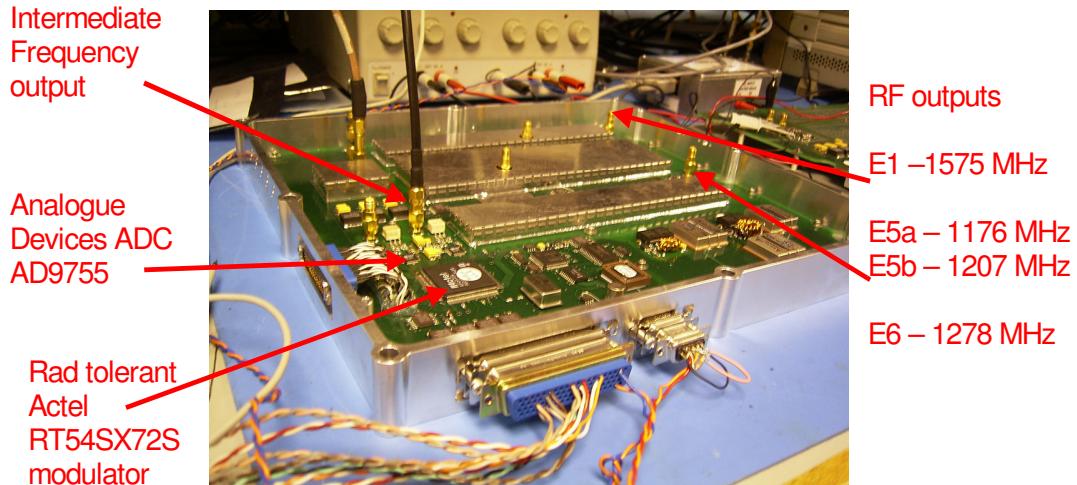


Figure 7-3, MFUU for Giove-A

The combination of an FPGA and the AD9755 was suggested by Spirent Communications, a leading supplier of GNSS signal simulations. The AD9755 has two input ports and alternately samples each port converting its value to an analogue current. If the sampling rate of the DAC is set to 4 times the desired signal IF, then the time difference between alternating samples is equivalent to 90 deg at the IF. Therefore, the in-phase (I) and quadrature (Q) modulation of the carrier can be achieved by feeding to the DAC synchronised but unique code sequences each modulated with an in-phase IF carrier.

The modulation concept is simple and provides and elegant solution for GNSS signal generators. Let there be an analogue waveform

$$u(t) = A \cos(\omega_0 t + \theta) \quad 7-1$$

or

$$u(t) = A \cos(2\pi f_0 t + \theta) \quad 7-2$$

which is then sampled at a rate $f_s = 4f_0$ (carrier frequency). Without loss of generality we write the corresponding data sequence from $t = 0$

$$\begin{aligned} u[k] &= u(t_k) = A \cos(2\pi f_0 t_k + \theta) \\ &= A \cos\left(\frac{k\pi}{2} + \theta\right) \end{aligned} \quad 7-3$$

If we look at the even numbered samples then

$$u[0], u[2], u[4], \dots = +\text{Acos}(\theta), -\text{Acos}(\theta), +\text{Acos}(\theta), \dots$$

while odd numbered samples are

$$u[1], u[3], u[5], \dots = -\text{Asin}(\theta), +\text{Asin}(\theta), -\text{Asin}(\theta), \dots$$

Even numbered samples can be identified as sign-alternating samples of an I-channel modulation. Odd numbered samples can be identified as sign-alternating samples of a Q- channel modulation

We create a parallel input stream with a sampling rate in each of $f_{Si} = 122.76$ MHz, so that

$$\begin{aligned} u[2k] &= (-1)^k m_I[k] \\ u[2k+1] &= -(-1)^k m_Q[k] \end{aligned} \quad 7-4$$

which gives us a sequence

$$+m_I[0], -m_Q[0], -m_I[1], +m_Q[1], +m_I[2], -m_Q[2], -m_I[3], +m_Q[3], +m_I[4] \dots \text{etc.}$$

Spectrally and with $f_0 = 61.38$ MHz then *output* sampling rate $f_{So} = 245.52$ MHz of the DAC supports a spectrum from dc to the Nyquist frequency $f_{No} = 122.76$ MHz.

Figure 7-4 shows a depiction of a BOC modulation being applied in I, and a PSK modulation in Q.

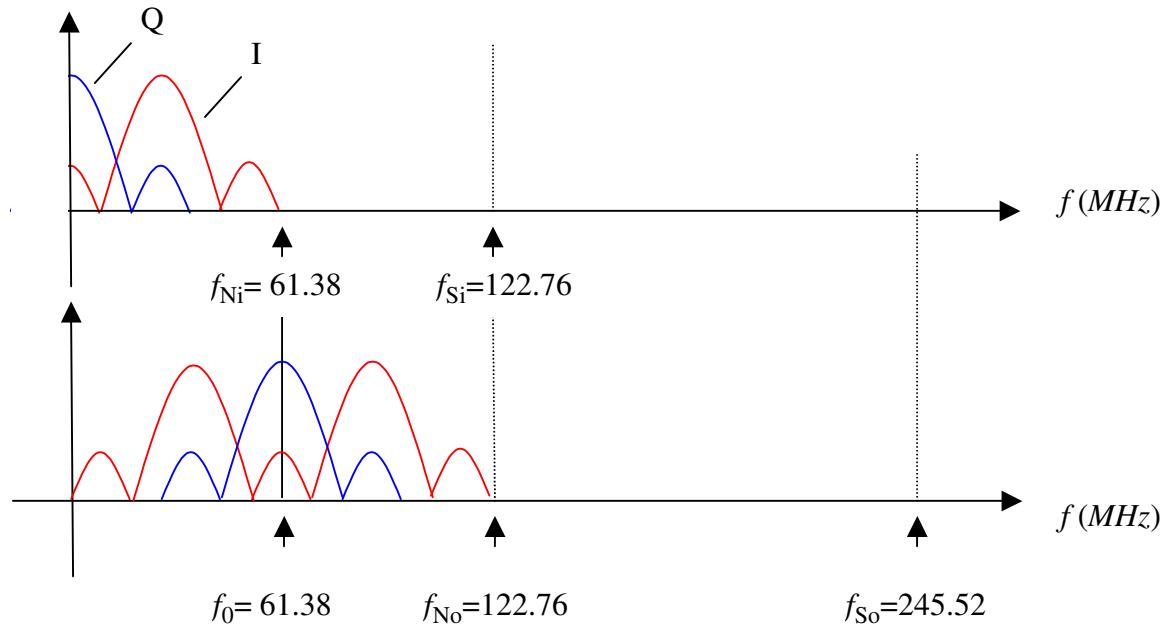


Figure 7-4

The *input* sampling rate in either channel $f_{Si} = 122.76$ MHz. supports a low pass bandwidth up to an input Nyquist rate $f_{Ni} = 61.38$ MHz.

A diagram of the code generation and IF modulation architecture of the MFUU is shown in Figure 7-5. In this case, the IF is 61.38 MHz and 122.76 MHz is fed to the

DAC, which is internally doubled to the desired sampling rate of 245.52 MHz. The great benefit of this scheme is of practical implementation. Creating I and Q components digitally within the FPGA would require clocking the FPGA at 245.52 MHz, which is impractical even with the fastest FPGA architectures. However, the AD9755 supports sampling rates up to 300 MHz and faster DACs are available. Using the DAC to introduce the I/Q modulation reduces the required FPGA clocking frequency by a factor of 2. Fine amplitude control of the signal is achieved through adjusting the 8-bit level passed to the DAC. Even greater amplitude control could be achieved if necessary as the AD9755 supports up to 14-bits of input precision.

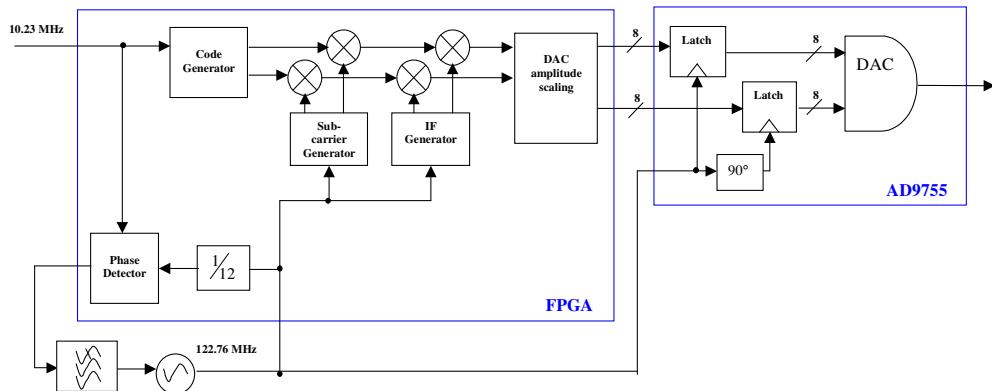


Figure 7-5, Simplified MFUU modulation architecture

The MFUU combines two Galileo navigation signals in a simple QPSK modulation, which can be represented as follows.

$$S_{QPSK}(t) = P_I \times c_1(t) \times d_1(t) \times \cos(\omega_L t) + P_Q \times c_2(t) \times d_2(t) \times \sin(\omega_L t) \quad 7-5$$

P_I and P_Q are the in-phase and quadrature signal powers respectively, $d(t)$ is the navigational data applied to the signal and ω_L is the L-band carrier frequency. If $a(t)$ is the PRN coding sequence then

$$c(t) = a(t) \times \text{sgn}[\sin(2\pi f_s t)] \quad 7-6$$

for a BOC modulated signal with sub-carrier frequency f_s and

$$c(t) = a(t)$$

7-7

for PSK modulated signals. A spectrum analyser of the plot of the MFUU Galileo E1 BOC(15, 2.5) signal is shown in Figure 7-6. The Galileo signals generated by the SSTL signal chain were verified and tested in the laboratory and in-orbit using the Septentrio Galileo experimental test receiver (GETR) [De Wilde *et al* 2004] [Rooney *et al* 2007].

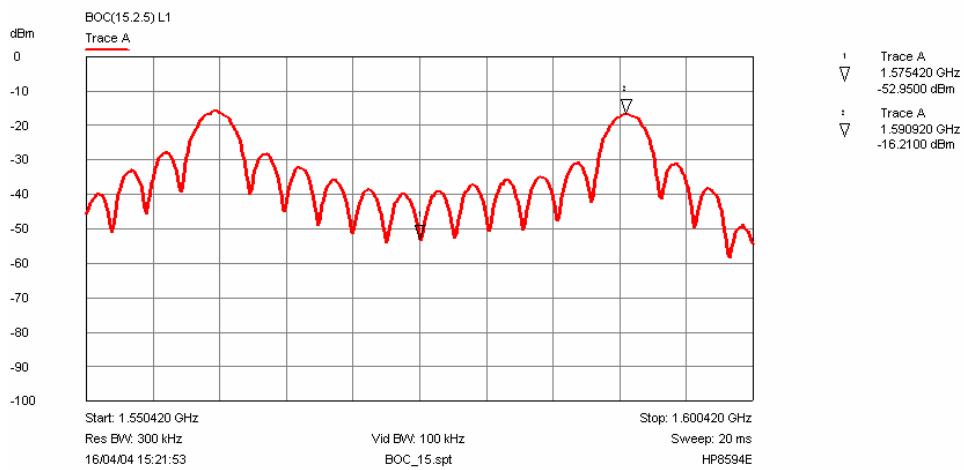


Figure 7-6, Spectrum analyser plot of the Galileo BOC(15, 2.5) –cosine signal from the MFUU

The MFUU on Giove-A will produce only QPSK signals and is based on Actel anti-fuse FPGAs, which are one-time programmable. However, this architecture is capable of producing all Galileo signals currently specified and representative GPS signals for receiver testing. Therefore, a more flexible IF signal generator based around a re-programmable FPGA has been subsequently produced for this research. This IF signal generator (see Figure 7-7), reuses the modulation technique implemented in the MFUU and can combine GNSS signals using QPSK, interplex or AltBOC modulations as desired for receiver testing.

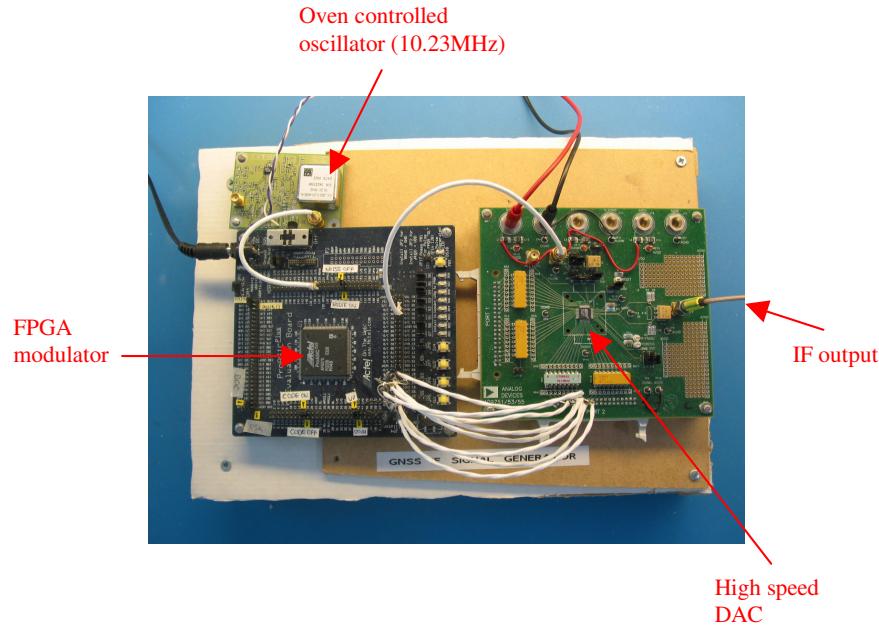


Figure 7-7, Bench IF signal generator

An equivalent to the *interplex* modulation also called *modified hexaphase* [Ries *et al* 2002] intended for Galileo [ESA and GJU 2006], can be produced by the *coherent adaptive subcarrier modulation* (CASM) technique [Dafesh *et al* 2000]. Equation 7–5 shows a representation of the combination of two signals on a single carrier. Interplex modulation introduces a third signal, θ in the form of a phase modulation as follows [Dafesh *et al* 1999].

$$\begin{aligned} S_{INT}(t) &= P_I \times c_1(t) \times \cos(\omega t + \theta(t)) - P_Q \times c_2(t) \times \sin(\omega t + \theta(t)) \\ &= [P_I \times c_1(t) \times \cos(\theta(t)) - P_Q \times c_2(t) \times \sin(\theta(t))] \cos(\omega t) \\ &\quad - [P_I \times c_1(t) \times \sin(\theta(t)) + P_Q \times c_2(t) \times \cos(\theta(t))] \sin(\omega t) \end{aligned} \quad 7-8$$

If $\theta(t)$ is another switching type signal written as

$$\theta(t) = m \times c_2(t) \times c_3(t) \quad 7-9$$

where m is the modulation index, which determines the relative distribution of the transmitter power between the signals and $c(t) \in (+1, -1)$. The resulting modulation is equivalent to interplex modulation and can be written as follows.

$$S_{INT}(t) = \begin{bmatrix} P_I \times c_2(t) \times \cos(m) \\ -P_Q \times c_3(t) \times \sin(m) \end{bmatrix} \cos(\omega t) + \begin{bmatrix} P_I \times c_1(t) \times \cos(m) \\ +P_Q \times c_1(t) \times c_2(t) \times c_3(t) \times \sin(m) \end{bmatrix} \sin(\omega t) \quad 7-10$$

The combination of all three PRN code sequence in the quadrature arm is called the *inter-modulated product* (IMP). It is generally the aim of the designer to minimise the power contribution of the IMP as most receivers will not process this combination. The relative power levels of the interplex modulated GPS and Galileo signals are shown in Table 7-1.

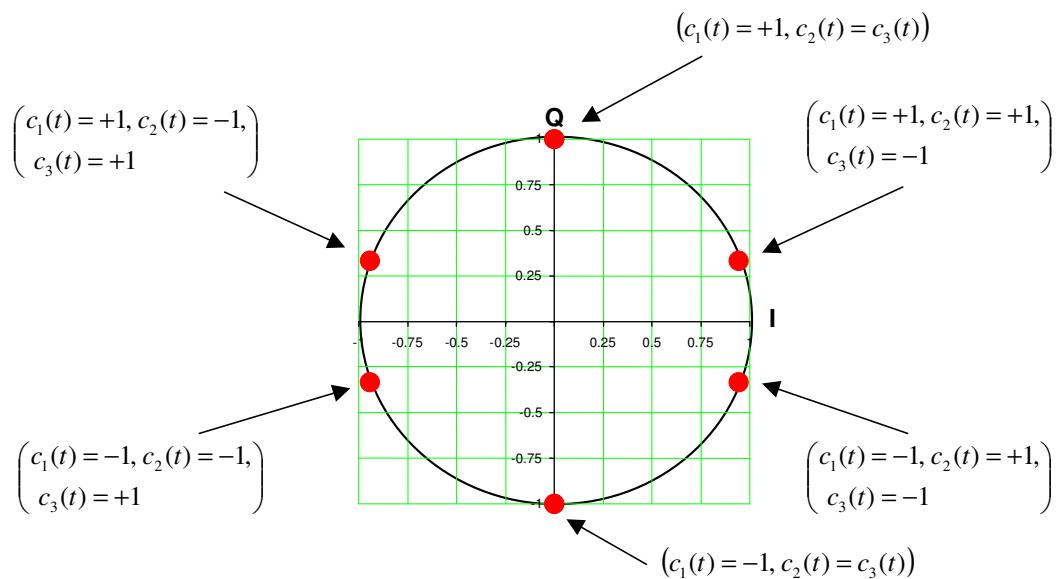
Table 7-1, Relative signal powers of interplex modulated GNSS signals

PRN code sequence	Equivalent Galileo E1 or E6 signal	Equivalent GPS L1 or L2 signal	Relative signal powers	
			Galileo E1 and E6 ($m = 0.6155$)	GPS ($m = 0.66$)
c_1	A	C/A or L2(C)	22.2%	22.2%
c_2	B	P(Y)	44.4%	40.2%
c_3	C	M	22.2%	24.2%
$c_1 \times c_2 \times c_3$	-	-	11.1%	13.4%

With regard to signal generation, the interplex modulation can be achieved simply by adjusting the I and Q levels of the DAC for each of the 8 possible states of the three input signals in accordance with the chosen modulation index. Table 7-2 shows the mapping of input signal state to 8-bit (0 to 255) DAC amplitude levels for GPS and Galileo signals1. In this representation the value of 127 should be regarded as the zero point. The I/Q plots of GPS and Galileo signal generated as a result of interplex modulation are shown in Figure 7-8 and Figure 7-9 respectively. It can be seen that the IMP controls the amplitude of the quadrature contribution in order to maintain constant envelope signal.

Table 7-2 Example DAC amplitude mapping for interplex modulated GNSS signals

Signal state				DAC input level			
				Galileo E1 and E6 ($m = 0.6155$)		GPS ($m = 0.66$)	
c_1	c_2	c_3	$c_1 \times c_2 \times c_3$	I	Q	I	Q
1	1	1	1	127	254	124	254
1	1	-1	-1	247	169	249	161
1	-1	1	-1	7	169	124	0
1	-1	-1	1	127	254	249	93
-1	1	1	-1	127	0	5	161
-1	1	-1	1	247	85	130	254
-1	-1	1	1	7	85	5	93
-1	-1	-1	-1	127	0	130	0

**Figure 7-8, I Q plots for Galileo interplex modulated signals ($m = 0.6155$)**

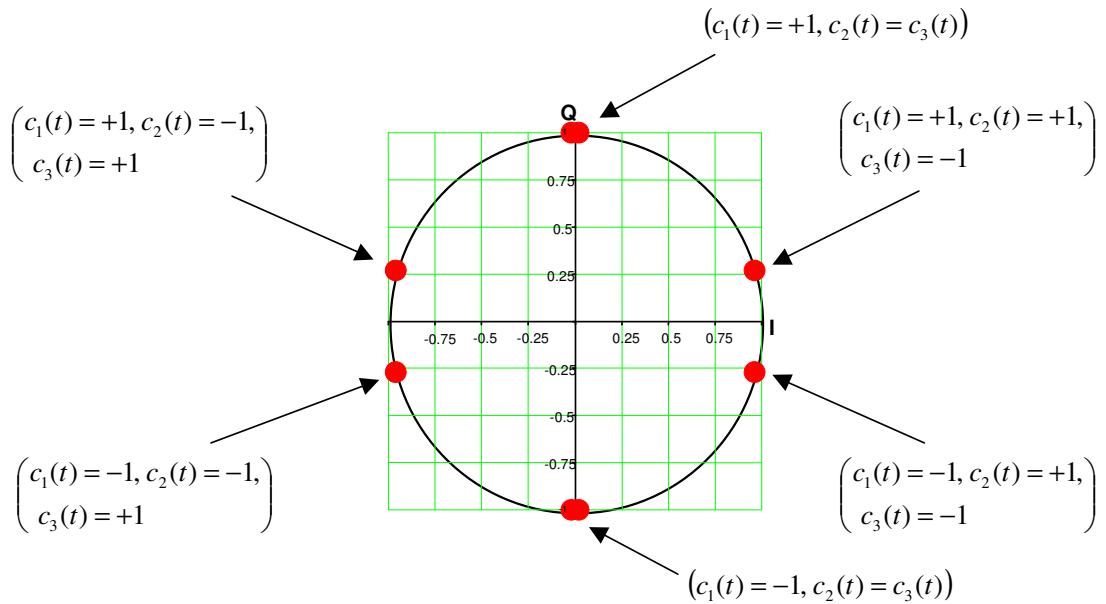


Figure 7-9, I Q plots for GPS interplex modulated signals ($m = 0.66$)

The advantage of interplex modulation is that it is in theory a constant envelope modulation. This is important because it allows a single high power amplifier to be implemented in the transmitting satellite, removing the need for inefficient combining of separate stages [Dafesh *et al* 2000]. Constant envelope signals also act to mitigate the non-linear effects of high power amplifiers, such as spectral re-growth. Therefore, despite the power lost in the IMP, interplex claims to provide a very efficient method to combine three PRN code signals onto a single carrier. Figure 7-10 shows the result of interplexing two BOC(1,1) signals (data and pilot) with a third BOC(10,5) signal, using the modulation index, $m = 0.825$.

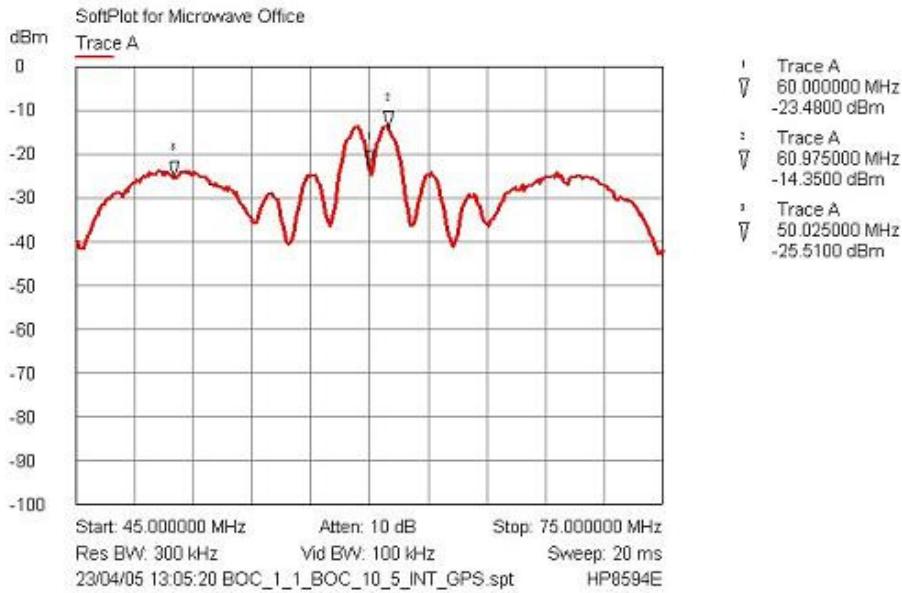


Figure 7-10, Interplex of 2*BOC(1,1) + BOC(10,5) IF signals

The AltBOC modulation will be used by future Galileo satellites to combine four PRN code signals onto a single carrier in the Galileo E5 band. The AltBOC modulation can be written as follows.

$$\begin{aligned} S_{AltBOC}(t) = & P_A \times [c_1(t) + c_2(t)] \times s(t) \times \cos(\omega_L t) \\ & + P_A \times [c_1(t) - c_2(t)] \times \tilde{s}(t) \times \sin(\omega_L t) \\ & + P_B \times [c_3(t) + c_4(t)] \times \tilde{s}(t) \times \cos(\omega_L t) \\ & - P_B \times [c_3(t) - c_4(t)] \times s(t) \times \sin(\omega_L t) \end{aligned} \quad 7-11$$

$s(t)$, is a in-phase square wave sub-carrier and $\tilde{s}(t)$ is orthogonal square wave sub-carrier. The four PRN code sequences have 16 possible combinations, which are used to control the phase of the sub-carrier waveform. This is accomplished by producing 8 phase-shifted versions of the sub-carrier waveform, where the state of the PRN sequences determines which is modulated onto the carrier. For implementation in hardware, it is simpler to view the AltBOC as an 8-PSK modulation as follows.

$$S_{AltBOC}(t) = \text{sgn} \left[\sin \left(\frac{2\pi t}{T_s} + \theta_A \right) \right] \cos(\theta_B) \cos(\omega_{L5} t) + \text{sgn} \left[\sin \left(\frac{2\pi t}{T_s} + \theta_A \right) \right] \sin(\theta_B) \sin(\omega_{L5} t) \quad 7-12$$

$\theta_A \in \left(0, \frac{\pi}{4}, \frac{\pi}{2}, \frac{3\pi}{4}\right)$, $\theta_B \in \left(0, \pm\frac{\pi}{4}, \pm\frac{\pi}{2}, \pm\frac{3\pi}{4}\right)$ and T_s is the sub-carrier period. θ_A defines the timing of 180° phase reversals of the carrier and θ_B chooses the pair of opposite phase points which are hopped between during the chipping interval. θ_A and θ_B are set by the 16 possible states of the input sequences using a look-up table, shown in [Kaplan and Hegarty 2006]. Again, this can be achieved in hardware simply by adjusting the I and Q levels of the DAC for each of the 16 possible states of the four input signals and the transitions of the sub-carrier (see Appendix I). A spectrum analyser plot of an AltBOC(15,10) signal is shown in Figure 7-11.

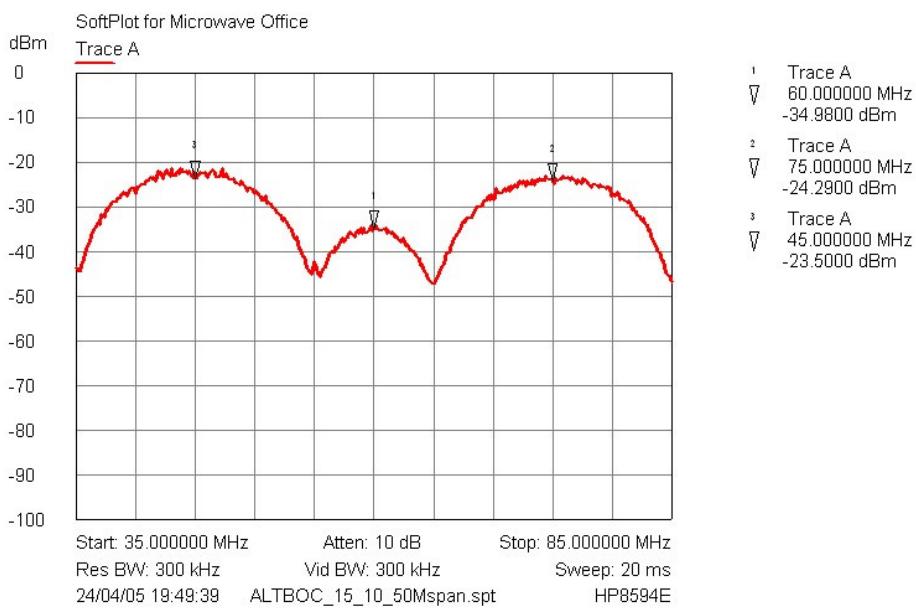


Figure 7-11, AltBOC(15,10) IF signal

7.2 Digital noise synthesis

In order to enable receiver performance testing in various noise conditions we synthesise additive noise digitally in the IF signal generator. Dr MS Hodgart provided the statistical principles required to precisely control the carrier to noise density C/N_0 of the source. A representation of the digital noise synthesis implemented in the IF signal generator is shown in Figure 7-12.

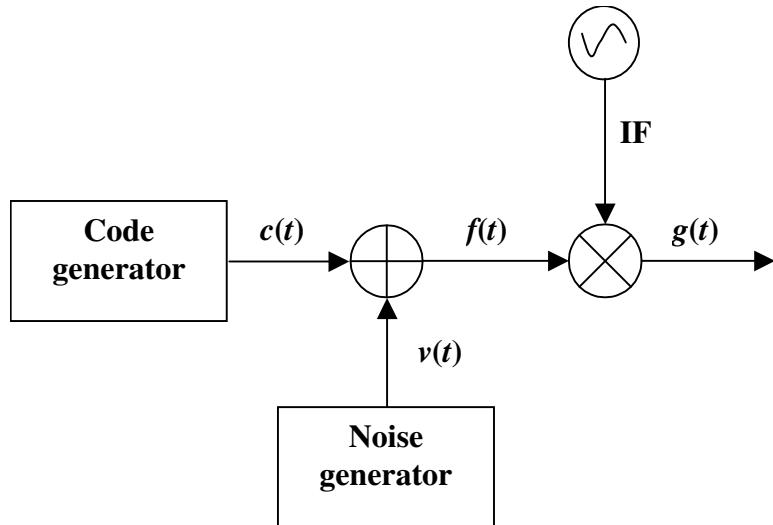


Figure 7-12, IF noise synthesis

The representations shown in Figure 7-12 are continuous in time. However, in the digital FPGA architecture the signal is necessarily discretized in steps, k . We add an integer noise sequence $v[k]$ with known quasi-Gaussian distribution before multiplication with the IF carrier. The quasi-Gaussian integer noise sequence is created by addition of random numbers generated using a multiplicative congruential random number generator developed first in [Lehmer 1951]. Lehmer's algorithm is generally considered the benchmark for random number generation satisfying virtually all tests of statistical randomness [Park and Miller 1988]. This elegantly simple algorithm can be implemented to generate random numbers $z[k]$ as follows.

$$z[k+1] = \text{mod}(r \times z[k], q) \quad 7-13$$

q is called the modulus and is a large prime integer, the multiplier r is an integer in the range $2 \leq r \leq q - 1$. The operation $\text{mod}(x, q)$ means the remainder after division of x by q . The designer must also set an initial value or seed $n[0]$ in the range $1 \leq n[0] \leq q - 1$. We choose $r = 7^5 = 16807$, $q = 2^{31} - 1$ and a seed $n[0] = 1$ as recommended values used in [Park and Miller 1988] and adopted by the well-known mathematical software Matlab. Figure 7-13 shows a histogram of 50,000 normalised random numbers generated by Equation 7-13.

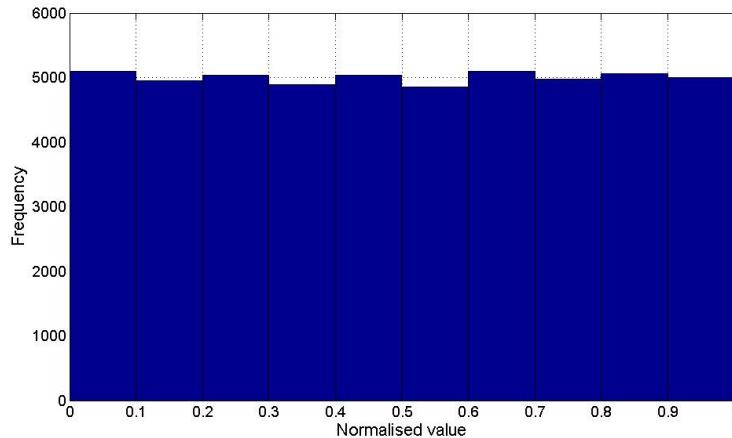


Figure 7-13, Histogram of 50,000 numbers from the multiplicative congruential random number generator

A quasi-Gaussian distribution is generated in the IF signal generator by a pipelined addition of eight random numbers as follows.

$$v[k] = \sum_{i=0}^7 n[k-i] \quad 7-14$$

Figure 7-14 shows a histogram of the quasi-Gaussian distribution derived from Modelsim simulation of the IF signal generator VHDL code. The distribution has a mean of $\mu = 128$ (zero for an 8-bit DAC) and a standard deviation of $\sigma = 24.292$.

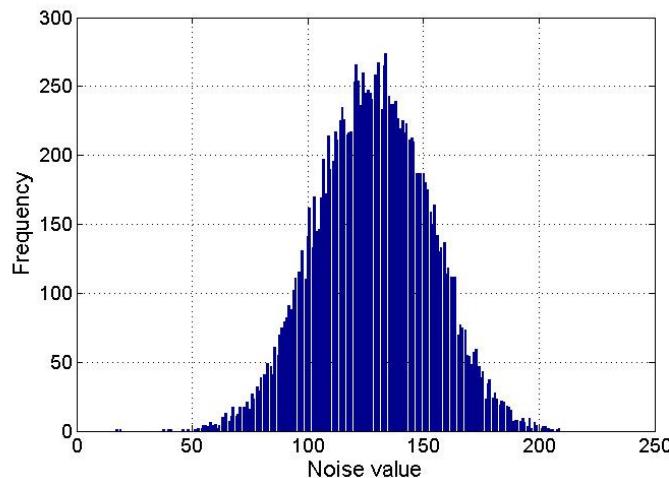


Figure 7-14, Histogram of quasi-Gaussian noise generator (15852 points)

We define a DAC sampling rate to code rate ratio, $K_{SC} = f_{DAC}/f_C$ and a noise decimation factor $K_N = f_{DAC}/f_N$, where f_N is the noise update rate. The PRN code sequence with added noise can then be written as follows.

$$f[k] = c[k/K_{SC}] + v[k/K_N] \quad 7-15$$

Where the notation [] denotes an ‘integer’ or ‘floor’ to a real number. The result of modulating with a bipolar (± 1) IF carrier running at half the DAC sampling rate can then be written as follows.

$$g[k] = f[k] \times (-1)^k \quad 7-16$$

Theory presented by Dr MS Hodgart (see Appendix F) derives an effective carrier to noise density for the digital noise synthesis as follows.

$$\begin{aligned} C/N_0 &= \frac{2 \times A^2 \times f_N}{\sigma_N^2} \\ &= \frac{2}{K_N} \times \frac{A^2 \times f_{DAC}}{\sigma_N^2} \end{aligned} \quad 7-17$$

where σ_N is the r.m.s. value of the synthesised noise A is the amplitude level given to the PRN code sequence, either $+A$ or $-A$.

Figure 7-15 shows a spectrum analyser plot of a BOC(1,1) signal produced by the IF signal generator with the digital noise generator switched off. The IF signal has a centre frequency of 20.46 MHz. Figure 7-16 shows a spectrum analyser plot of a BOC(1,1) signal produced by the IF signal generator with the digital noise switched on. We choose a noise update rate of 1.023 MHz, $A = 1$, $\sigma_N = 24.292$ and $f_{DAC} = 81.84$ MHz, which equates to a carrier to noise density of 38.4 dB-Hz.

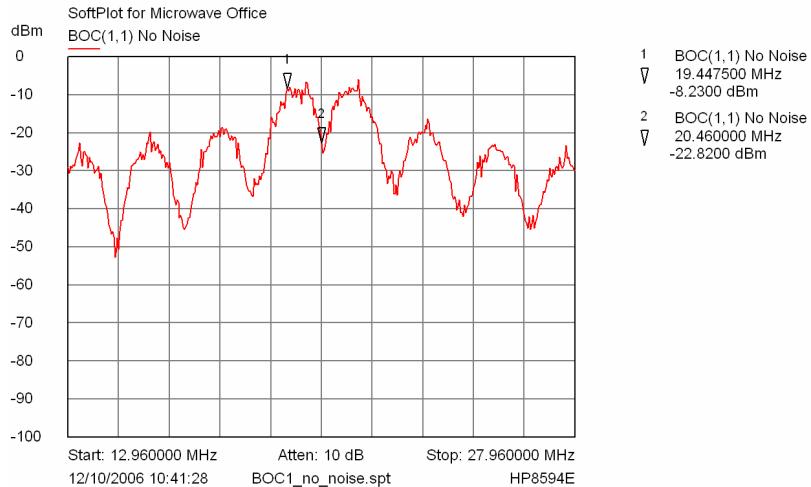
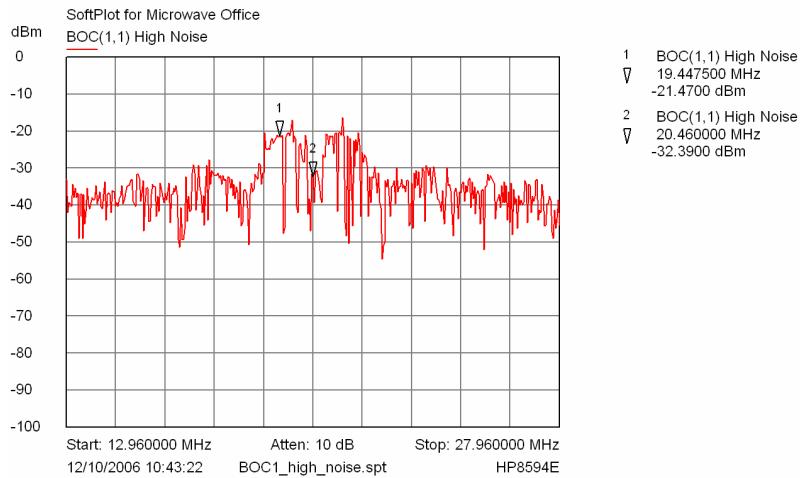


Figure 7-15, Spectrum analyser plot of BOC(1,1) from IF signal generator with no noise.



**Figure 7-16, Spectrum analyser plot of BOC(1,1) from IF signal generator with noise
($C/N_0 = 38.4\text{dB-Hz}$).**

Receiver performance testing using the IF signal generator across various carrier to noise levels is shown in Chapter 9.2.

This chapter has detailed the implementation of GNSS signal generators in hardware. The design of the SSTL MFUU Galileo signal generator was outlined and its extension to a prototype IF signal generator used by this research. The modulation techniques and representations of current and future GNSS signals are detailed with implementation examples. Also, the principles of digital noise synthesis for bench testing of GNSS receivers are given with application to the IF signal generator.

8 The SGR receivers and the PIF receiver

This chapter provides a detailed overview of SSTL’s existing receiver designs and identifies specific areas of improvement that this project has contributed towards. It is necessary to understand the detailed low-level hardware functions of existing GNSS space receivers, such as the SSTL receivers in order to address the impact of the future GNSS signals and enhancements on the receiver. The design of an experimental Prototype Intermediate Frequency (PIF) receiver is detailed. The PIF receiver provides a development platform for evaluating acquisition and tracking approaches to the new generation of GNSS signals. The choice of components for the receiver and the rationale behind them is discussed. Details are also given on the frequency plan and sampling scheme for the receiver. Finally, a full description of the inner workings of the receiver’s correlator and processor are given with an emphasis on the adaptations required for future GNSS signals. The PIF receiver provides a demonstration of the DE BOC tracking technique and details on the receiver processes required for implementation of this technique are given.

8.1 The SSTL receiver hardware

SSTL produces and supplies a wide range of Space GNSS Receivers (SGRs). These receivers are primarily used for their position, velocity and time (PVT) information, enabling orbit determination for the parent spacecraft. In recent years the receivers have been used to demonstrate novel applications of GNSS in space, such as GNSS attitude determination and ocean reflectometry.

Table 8-1 summarizes the SGR range of receivers and highlights the key features of individual models.

Table 8-1, SGR receiver models

Receiver	Channels	Antennas	Mass (g)	Power consumption (W)	Key features / applications
SGR-05	12	1	20	0.8	Miniaturised receiver suitable for nano-satellites
SGR-10	24	2	1050	5.3	Established space receiver with considerable heritage. Enhanced version used for GNSS ocean reflectometry
SGR-20	24	4	1150	6.3	Enabled for 3-axis attitude determination
SGR-GEO	24	1 or 2	2500	5.0	Suitable for GEO and GTO applications

The SGRs are based on a chipset from Zarlink semiconductors [Zarlink 1999] and comprise of an RF front-end, an ASIC correlator and an ARM processor. A block diagram of the key components of the SGR is shown in Figure 8-1. The RF signal is received through the use of a Right-Hand Circularly Polarised (RHCP) antenna and fed directly into a Low Noise Amplifier (LNA), which effectively sets the noise floor for the receiver. This is the most critical amplification stage, because at this point the signal is below the thermal noise floor and any noise is amplified along with the signal of interest. Therefore, it is important that the noise figure of the LNA is as small as possible (≤ 3 dB) while providing enough gain to raise the signal above the thermal noise level (20-30 dB). The LNA also provides filtering to protect against saturation from transmitters at other frequencies.

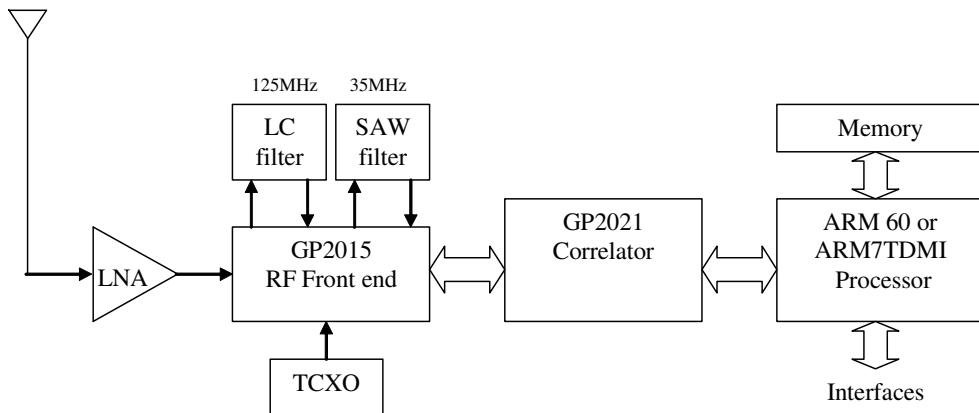


Figure 8-1, SGR receiver components

The GP2015 chip converts the GPS L1 signals (1575.42 MHz) to 4.309 MHz in three down-conversion stages, filtering at each stage resulting in a IF bandwidth (1 dB) of 1.9 MHz. The GP2015 then samples the signal at a rate of 5.714 MHz, which translates an image of the negative frequency to 1.405 MHz, as depicted in Figure 8-2. All mixing frequencies and the sampling frequency are derived from a 10 MHz Temperature Controlled Crystal Oscillator (TCXO).

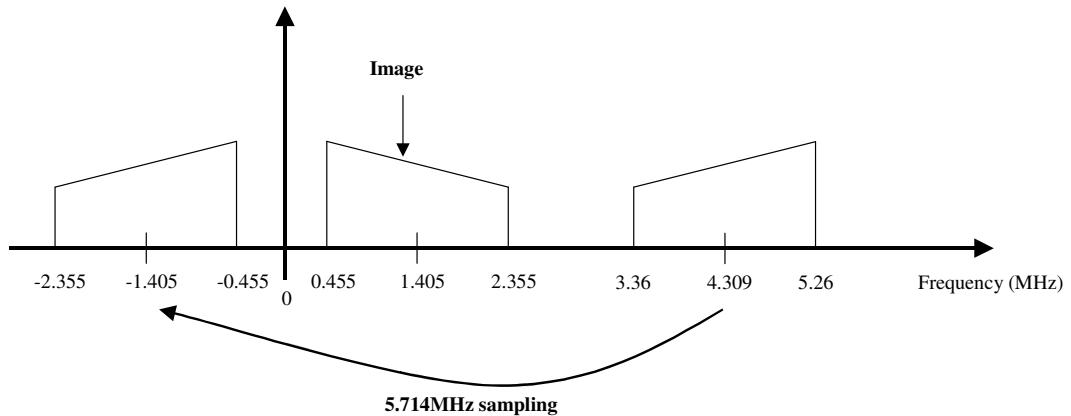


Figure 8-2, Frequency plan for GP2015

The signal is quantised to a 2-bit representation with the mapping shown in Table 8-2. The IF signal is used to control the Automatic Gain Control (AGC) loop, which sets the magnitude bit to be high 30% of the time and set the SIGN bit high approximately 50% of the time. The AGC loop is necessary to account for varying amplifier gains and any cable losses. The time constant of the AGC loop is controlled via an external capacitor to the GP2015. This time constant must be considerably less than the

settling time of the receiver's tracking loops in order track variations in power level without compromising the receiver operation.

Table 8-2, 2-bit mapping by the GP2015

Signal level	Bit 0 (SIGN)	Bit 1 (MAG)	Percent in state (%)
-3	0	1	15
-1	0	0	35
+1	1	0	35
+3	1	1	15

In the absence of Continuous Wave (CW) interference the distributions across the four digital levels given in Table 8-2 are held to within $\pm 1\%$ across a temperature range of -50°C to 110°C. However, in the presence of moderate CW interferers this is degraded to $\pm 10\%$ [Zarlink 1999]. Figure 8-3 shows a histogram of an example distribution of sampled bits from the GP2015.

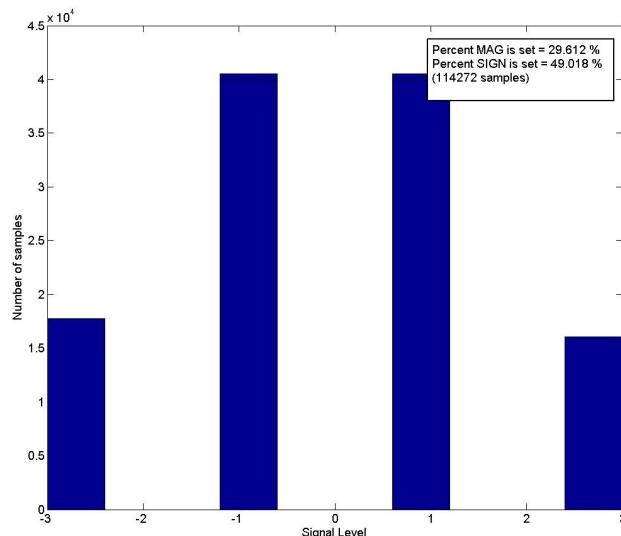


Figure 8-3, Histogram of sampled signals from the GP2015

The 2-bit quantised signal is fed to the GP2021 correlator, which is a dedicated 12-channel GPS L1 C/A code correlator ASIC, shown in Figure 8-4. SGRs with 24 channels effectively combine two GP2021 chips interfaced with a single processor. The GP2021 has a bus interface, an address decoder and a number of status registers to allow debugging of the correlator. The time-base generator produces two important interrupt signals, which are used to ensure correct receiver operation. The

first is a fast rate (<1 ms) interrupt for the accumulators (ACCUM_INT), this is necessary to ensure that the essential information required for tracking the incoming signal is read by the processor at least once every integration period. The second signal is the measurement interrupt (MEAS_INT), which allows the processor to read the raw measurement data. This interrupt is necessarily synchronized with the local oscillator to provide measurement data for the navigation solution. Both these interrupts are derived from and synchronized with the sampling frequency of 5.714 MHz.

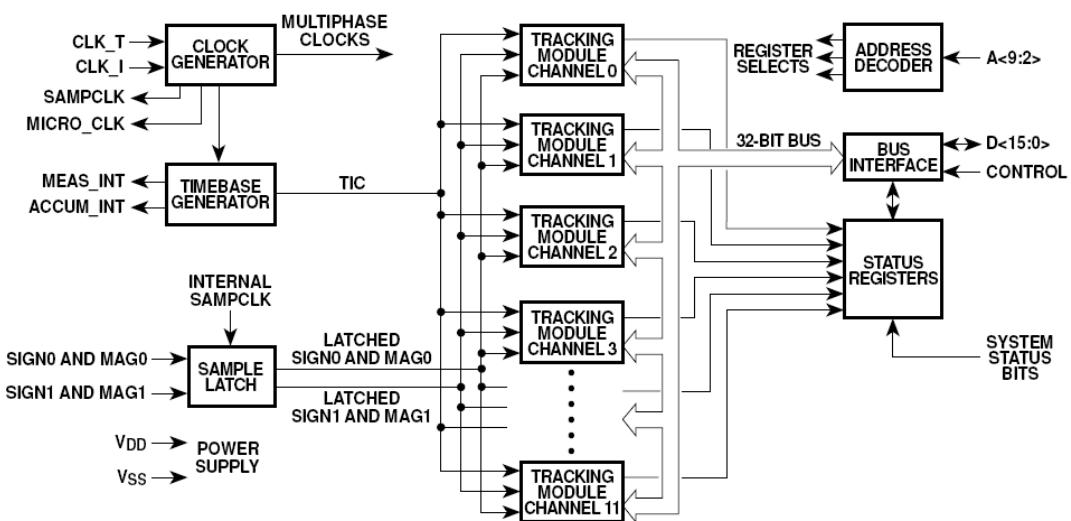


Figure 8-4, GP2021 block diagram [Zarlink 2001]

The incoming signal is latched and fed to the tracking modules, shown in Figure 8-5. Here, locally generated replicas of the carrier and code are multiplied onto the signal and the result is applied to the accumulator every sample period. At the end of the integration period the result is latched onto a register to be read by the microprocessor before the next dump. The carrier and code signals are driven by Digitally Controlled Oscillators (DCO), which can be updated instantaneously or at the start of each integration period. The tracking module has two modes, acquisition and tracking. As shown in Figure 8-5 these four results are equivalent to the correlation results derived for PSK in Equation 5-7 when the correlator is in tracking mode. In acquisition mode the tracking modules produce in-phase and quadrature correlation for a code sequence $\frac{1}{2}$ a chip earlier than the prompt code as in Equation 5-21.

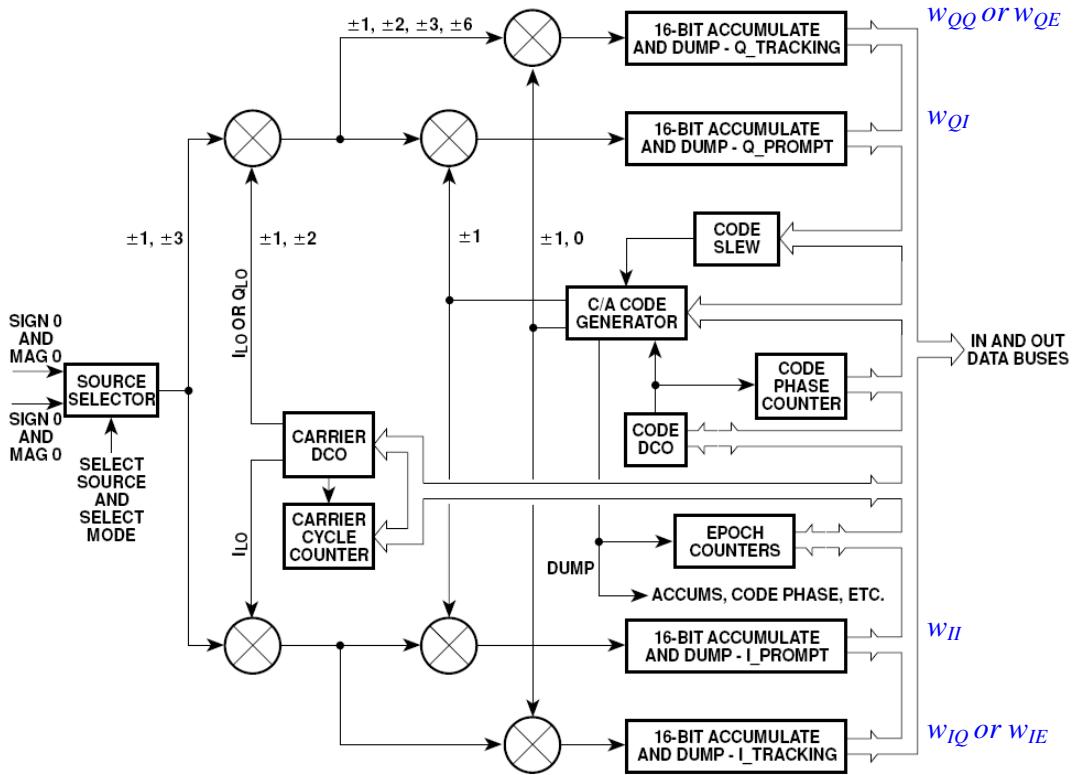


Figure 8-5, GP2021 tracking module diagram [Zarlink 2001]

The processor uses the interrupt signals produced by the GP2021 to ensure timely access to the correlation results and measurement data. Figure 8-6 depicts the interrupt driven task structure of the SGR processor. The initialisation involves setting up the software and starting the correlator channels running. After initialisation the software enables the software interrupts. The fast-rate tracking task reads the accumulator values, estimates the navigational data state and updates all three loops with new estimates of carrier and code phase. The lower-rate measurement task provides the detailed measurements required to form the navigation solution such as reading the carrier, and code DCO values and the necessary counters in the correlator. Under these essential tasks priority can be given to the various navigational tasks. The two low level tasks encompass the basic acquisition and tracking functions of the receiver and therefore are the tasks of interest for this research. Knowledge of the low-level processor tasks and correlator architecture is necessary in order to appreciate the receiver enhancements required by the future GNSS signals.

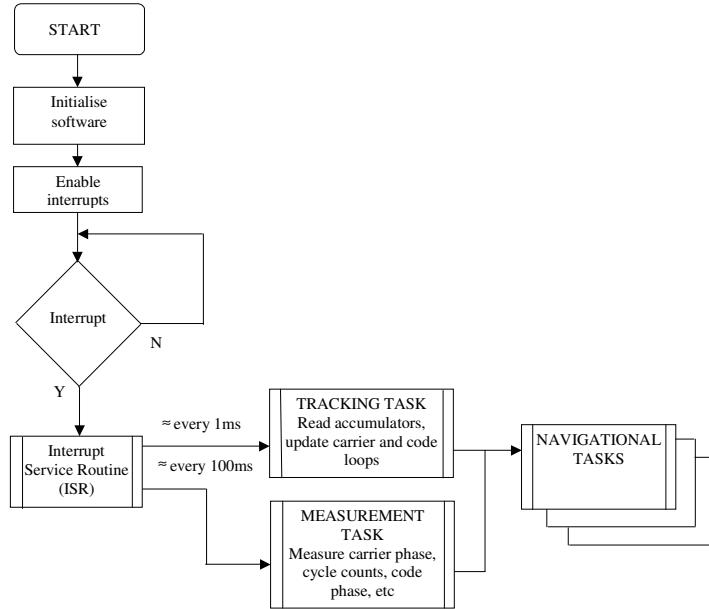


Figure 8-6, Interrupt service routine for SGR receivers

8.2 SGR acquisition and tracking loops

The implementation of PSK acquisition and tracking loops in the SGR gives us a basis on which to build and expand to realise the potential of the future GNSS signals. Therefore, in this section a detailed review of SGR's acquisition and tracking loops is given, from which we form the basis for the PIF receiver.

In order to judge whether a signal is present or absent the theoretical noise floor of the receiver must be calculated. While tracking is achieved this value can also be used to estimate the signal to noise ratio of the received signals. The theoretical noise floor of the receiver can be determined from statistical analysis of the correlation outputs with only thermal noise present at the receiver input. Table 8-3 shows the mean square accumulation values taken over one IF carrier cycle.

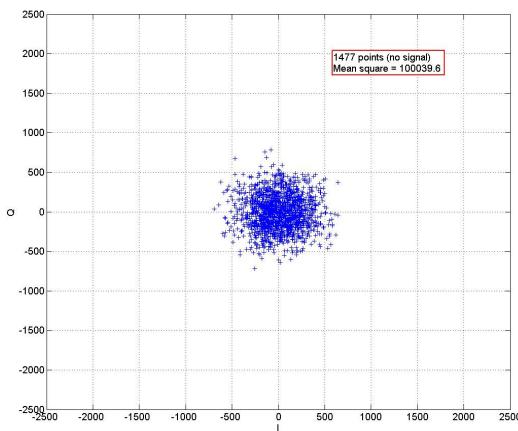
Table 8-3, Mean square accumulation values over one carrier cycle

Input signal from ADC	Result of sine carrier DCO mixing over one cycle									Mean square
+3	3	6	6	3	-3	-6	-6	-3	22.5	
+1	1	2	2	1	-1	-2	-2	-1	2.5	
-1	-1	-2	-2	-1	1	2	2	1	2.5	
-3	-3	-6	-6	-3	+3	+6	+6	+3	22.5	

Combining the mean square accumulation values from Table 8-3, with the statistical distribution of the input signal from Table 8-2, results in the following theoretical noise floor value for one accumulation period T .

$$NF_{SGR} = 2 \times (0.3 \times 22.5 + 0.7 \times 2.5) \times f_s \times T = 97,142 \quad 8-1$$

The factor of 2 accounts for the combination of two accumulation values (w_{II} and w_{QI}) that are used to determine the signal power, both of which contribute to the theoretical noise floor of the receiver. Figure 8-7 shows the noise floor of the SGR receiver with no signal present, the mean square of the I/Q points agrees strongly with the derived theoretical noise floor.

**Figure 8-7, SGR noise floor with no signal present**

The SGR uses a traditional time-domain search across two dimensions: code delay and carrier Doppler. The code search is performed by programming the code DCO to

run slightly faster than the predicted rate (0.8 chip per msec), allowing the received and replica codes to slide past each other with time. The presence or absence of a signal is determined by through the correlation power given by

$$w_{SSGR} = w_{II}^2 + w_{QI}^2 + w_{IE}^2 + w_{QE}^2 \quad 8-2$$

The SGR sums the correlation power of two identical PRN codes, one a $\frac{1}{2}$ chip earlier than the other. This allows a search rate of 0.8 chips per msec with a minimum correlation gain of only -0.7 dB from the peak value.

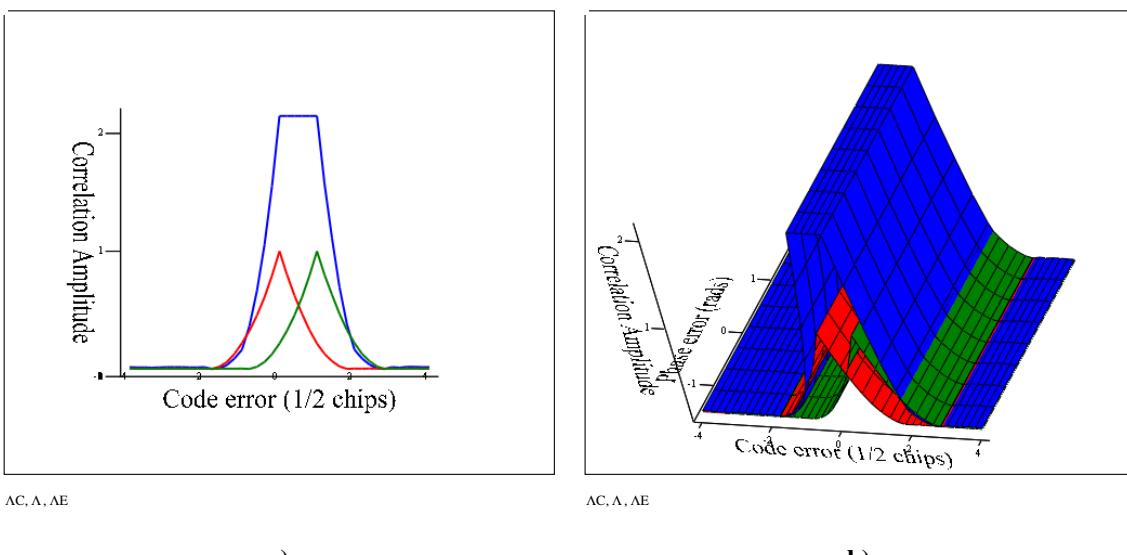


Figure 8-8, Plot combined search correlation w_{SSGR} (shown in blue)

Signal presence in the SGR is declared if the correlation power is greater than a threshold, which is nominally set to twice the receiver's theoretical noise floor. The carrier is searched in 500 Hz frequency bins. This corresponds to a minimum correlation gain of -4 dB compared to the peak.

The SGR tracking loops were originally based on the Mitel GPS Architect software, which was designed for the ARM60 processor. The Architect code uses a 2nd order FLL with the cross-product frequency discriminator described in Equation 5-14. In order to enable precise delta pseudorange, integrated Doppler measurements and applications such as attitude determination through GNSS a PLL is required. In 1999 the SGR was adapted to use a FLL/PLL combination to acquire and track GPS in

satellite orbits although it retains the ability to solely use the FLL for more robust applications.

The FLL/PLL combination uses a 1st order frequency discriminator to reduce the carrier frequency error to within the capture range of the PLL. The FLL employs two stages; acquiring the signal with a large loop bandwidth (31.25 Hz) and reducing the frequency error with a narrower loop bandwidth (1 Hz) FLL. The transition is made to the PLL when the estimated frequency error is less than 1 Hz. The SGR FLL uses a four quadrant discriminator which determines a frequency error term by differencing adjacent 1ms observations, assuming no data transitions have occurred. The change between adjacent I and adjacent Q samples can be written as

$$\begin{aligned}\Delta I &= I_k - I_{k-1} \\ \Delta Q &= Q_k - Q_{k-1}\end{aligned}\quad 8-3$$

The sign of the current correlations and their magnitudes provide the choice and sign of the error term as follows.

$$e_\omega = \begin{cases} \Delta Q & \text{for } |I_k| > |Q_k|, I_k > 0 \\ -\Delta Q & \text{for } |I_k| > |Q_k|, I_k \leq 0 \\ \Delta I & \text{for } |I_k| \leq |Q_k|, Q_k > 0 \\ -\Delta I & \text{for } |I_k| \leq |Q_k|, Q_k \leq 0 \end{cases} \quad 8-4$$

A block diagram of a first order FLL is shown in Figure 8-9.

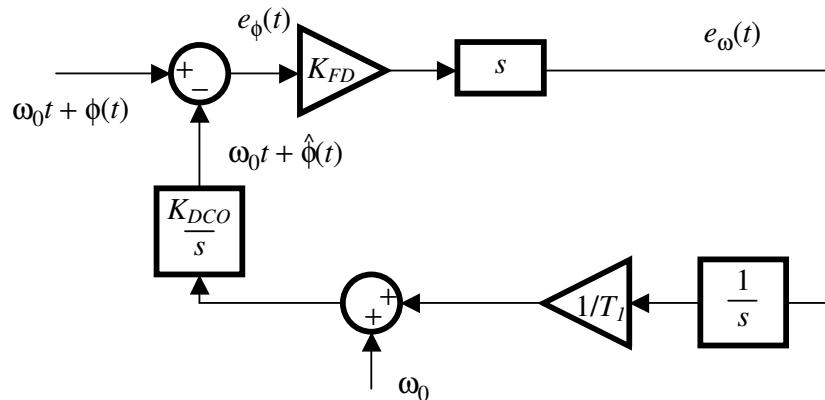


Figure 8-9, First order FLL

From Figure 8-9 the loop phase estimate can be identified as follows.

$$\hat{\Phi} = \frac{K_{FD} \times K_{DCO}}{s^2 T_1} \times E_\omega \quad 8-5$$

T_1 is the time constant of the first order loop, K_{FD} is the gain of the frequency discriminator and K_{DCO} is the carrier DCO gain. This can also be expressed in terms of phase error e_ϕ as follows.

$$\hat{\Phi} = \frac{s K_{FD} K_{DCO}}{s^2 T_1} \times (\Phi - \hat{\Phi}) = \frac{K_{FD} K_{DCO}}{s T_1} \times E_\phi \quad 8-6$$

In order to convert to the digital domain there is no unique mapping, but a commonly used approximation is [Jordan and Smith 1997]

$$s \approx \frac{1}{\Delta} (e^{s\Delta} - 1) = \frac{1}{\Delta} (z - 1) \quad 8-7$$

where Δ is the sampling or update interval of computation

$$\hat{\Phi} = \frac{K_{FD} K_{DCO} \Delta}{(z - 1) T_1} \times E_\phi \quad 8-8$$

or

$$(z - 1) \hat{\Phi} = \frac{K_{FD} K_{DCO} \Delta}{T_1} \times E_\phi \quad 8-9$$

$$(1 - z^{-1}) \hat{\Phi} = z^{-1} \frac{K_{FD} K_{DCO} \Delta}{T_1} \times E_\phi$$

which allows identification with the theory given in Chapter 5 for the FLL, which gives a digital loop update equation of the form

$$\begin{aligned} e_\phi &\leftarrow e_\phi + E_\omega \\ \hat{\phi} &\leftarrow \hat{\phi} + k_l \times e_\phi \end{aligned} \quad 8-10$$

where

$$k_l = \frac{K_{FD} K_{DCO} \Delta}{T_1} \quad 8-11$$

The natural loop frequency ω_n and loop bandwidth B_L can then be calculated as follows.

$$\omega_n = \frac{K_{FD} \times K_{DCO}}{T_1}, \quad B_L = \frac{\omega_n}{4} \quad 8-12$$

FLL loop bandwidths of 31.25 Hz and 1 Hz correspond to loop filter values (T_l) of 1/8 and 1/256 respectively. The receiver starts with the wide band filter and if carrier lock is declared the narrow band filter is used. The transition between FLL and PLL occurs when the frequency error, e_ω is estimated to be less than 1 Hz.

The SGR PLL is a 2nd order loop, a block diagram is shown in Figure 8-10.

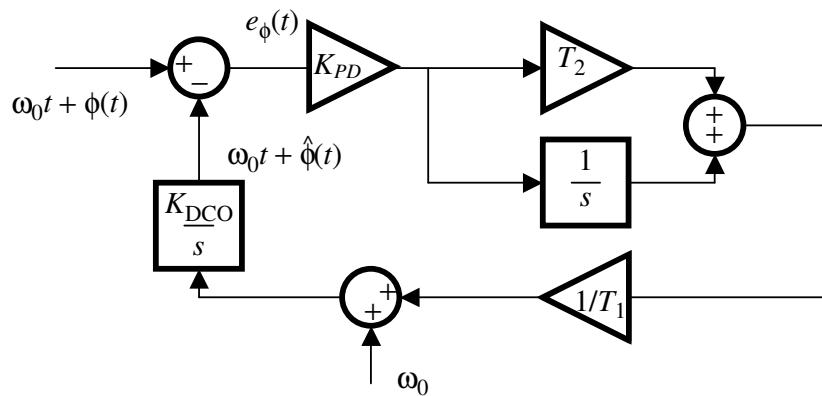


Figure 8-10, Second order PLL

The phase estimate of the second order PLL can then be written as follows.

$$\begin{aligned} \hat{\Phi} &= \frac{K_{PD} K_{DCO}}{s T_1} \times \left(T_2 + \frac{1}{s} \right) \times (\Phi - \hat{\Phi}) \\ &= \frac{K_{PD} K_{DCO}}{s T_1} \times \left(T_2 + \frac{1}{s} \right) \times E_\phi \end{aligned} \quad 8-13$$

T_1 and T_2 are time constants, K_{PD} is the gain of the frequency discriminator and K_{DCO} is the carrier DCO gain. Then converting to the digital domain using the approximation given in Equation 8-7 gives

$$\hat{\Phi} = \frac{K_\phi \Delta}{(z-1)T_1} \times \left(T_2 + \frac{\Delta}{z-1} \right) \times E_\phi \quad 8-14$$

or rearranging

$$(z-1)\hat{\Phi} = \frac{K_\phi \Delta^2}{T_1} f_\phi + \frac{K_\phi T_2 \Delta}{T_1} E_\phi \quad 8-15$$

$$(1-z^{-1})\hat{\Phi} = z^{-1} \frac{K_\phi \Delta^2}{T_1} f_\phi + z^{-1} \frac{K_\phi T_2 \Delta}{T_1} E_\phi$$

where

$$F_\phi = \frac{E_\phi}{(z-1)} \quad 8-16$$

which allows identification with the theory given in Chapter 5 for the FLL, which gives a digital loop update equation of the form

$$f_\phi \leftarrow f_\phi + e_\phi \quad 8-17$$

$$\hat{\phi} \leftarrow \hat{\phi} + k_1 \times f_\phi + k_2 \times e_\phi$$

where

$$k_1 = \frac{K_{FD} K_{DCO} \Delta^2}{T_1} \quad k_2 = \frac{K_{FD} K_{DCO} T_2 \Delta}{T_1} \quad 8-18$$

The filter coefficients T_1 and T_2 set the natural loop frequency ω_n , the damping factor ξ and loop bandwidth B_L as follows

$$\omega_n = \sqrt{\frac{K_D \times K_{DCO}}{T_1}}, \quad \xi = \frac{T_2 \times \omega_n}{2}, \quad B_L = \omega_n \frac{(1+4 \times \xi^2)}{(8 \times \xi)} \quad 8-19$$

The designer must consider a trade off at this point between narrowing the loop bandwidth to reduce the thermal noise jitter and widening the loop bandwidth in order to track accelerations. This depends strongly on the dynamic environment the receiver will operate within. Also, in practical systems there is the consideration of computational load, the SGR loop design chooses filter values to the nearest power of 2 to reduce microprocessor burden. The effect of this is to shift the loop parameters away from the desired values. Therefore, if the response parameters of the loop are

critical, floating-point calculations must be performed within high-speed tracking processes.

The maximum rate of change that can cause loss of lock is can be approximated by [Gardener 1979]

$$\Delta\dot{\phi}_{\max} = \omega_n^2 \quad 8-20$$

The SGR loops are designed for a maximum acceleration of 60 Hz/s, however the approximation to power of two calculations reduces the maximum to 52.1 Hz/s.

The DLL in the SGR uses the dot product discriminator, which has the following error function (repeat from Equation 5-17).

$$e_\tau = w_{II} \times w_{IQ} + w_{QI} \times w_{QQ} \quad 8-21$$

This discriminator is used in a first order loop as described in Equation 8-10. The SGR code DLL has a loop bandwidth of 0.25 Hz. It is only possible for the DLL to be first order and employ such narrow loop bandwidths because the DLL receives Doppler aiding from the carrier loop. The carrier tracks the frequency and/or phase of the incoming signal; this is a second order loop and tracks accelerations in the system. The estimated Doppler frequency of the carrier can then be applied to the DLL, with sufficient scaling to effectively remove the dynamics from the loop and allow first order operations.

The scaling K_ϕ is simply the ratio of the code frequency to the L-band carrier frequency (1.023 MHz / 1575.42 MHz for standard GPS). If the carrier update is $\hat{\phi}$ then the loop update equation with carrier aiding becomes

$$\hat{\tau} = \hat{\tau} + k_\phi \times f_\phi + k_\tau \times e_\tau \quad 8-22$$

where

$$k_\tau = \frac{K_{CD} K_{DCO} \Delta}{T_1} \quad 8-23$$

Where T_1 is the time constant of the first order loop, K_{CD} is the gain of the code discriminator and K_{DCO} is the code DCO gain.

The SGR receiver uses a number of indicators to monitor the quality of the code and carrier tracking. The quality of the code tracking is computed by taking running average of the correlation power. The SGR code lock indicator can be written as

$$C_{dLi} = C_{dLi} + \left(\frac{(w_H^2 + w_Q^2) - C_{dLi}}{256} \right) \quad 8-24$$

The signal to noise ratio can then be estimated by comparing this filtered value to the receiver's noise floor as follows.

$$SNR_{SGR} = 10 \times \log \left(\frac{C_{dLi}}{NF_{SGR}} \right) \quad (dB - kHz) \quad 8-25$$

This represents the signal to noise in a 1 kHz bandwidth ($T = 1$ ms), to convert to standard units of carrier to noise in a 1 Hz bandwidth simply use the following translation.

$$\frac{C}{N_0} = SNR_{SGR} + 10 \times \log \left(\frac{1}{T} \right) \quad (dB - Hz) \quad 8-26$$

While the receiver is tracking in FLL mode the quality of the carrier frequency tracking is computed by looking at adjacent I and Q samples (assuming no data transition). The SGR carrier lock indicator while running a FLL is given by

$$C_{rLiF} = C_{rLiF} + \left(\frac{(w_{II}' \times w_{QI}') + w_{QI} \times w_{II}') - C_{rLiF}}{4096} \right) \quad 8-27$$

where w_{II}' and w_{QI}' are the previous correlation results.

When the receiver is in PLL mode the quality of the carrier phase tracking is computed by subtracting the correlation power in the quadrature channel from the in-phase correlation power. The SGR carrier lock indicator while running a PLL is given by

$$C_{rLiP} = C_{rLiP} + \left(\frac{(w_{II}^2 - w_{QI}^2) - C_{rLiP}}{4096} \right) \quad 8-28$$

The current range of SGR receivers have been very successful and still offer an attractive product for most space applications. However, the receiver is restricted to the capabilities of the now aging Zarlink GPS chipset and requires a more flexible architecture to gain the advantages of future GNSS systems.

8.3 PIF receiver hardware and frequency plan

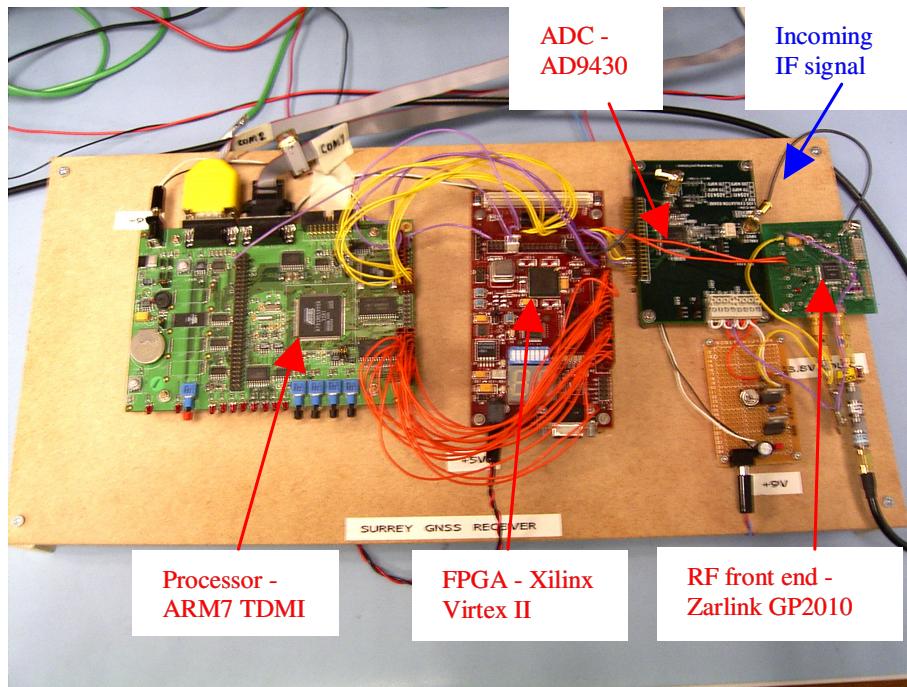
Evaluation of receiver acquisition and tracking algorithms for future GNSS signals is desirable at an Intermediate Frequency (IF) due to the current lack of RF front-end architectures suitable for these signals. The PIF receiver was created in order to evaluate the performance of different variations in receiver architectures for the new signals and novel acquisition and tracking techniques. In particular, the PIF receiver provides a demonstration of the DE BOC receiver and enabled the detailed hardware processes and performance of the DE technique to be defined, tested and analyzed.

This project provides a PIF receiver architecture, which will provide the flexibility for many new variants of SSTL space receivers, while maintaining the same baseband architectural components. Table 8-4 outlines the receiver versions suggested by this research as forming the future range of SSTL GNSS receivers. All these receivers are based on the baseband receiver architecture provided by the PIF receiver.

Table 8-4, Predicted future SSTL receiver versions

Receiver version	Signals processed	Filter bandwidth	Sampling frequency	Application
1	GPS L1	2 MHz	5.7 MHz	Single frequency, low precision, low bandwidth
2	GPS L1	2 MHz	5.7 MHz	Dual frequency, low precision, low bandwidth
	GPS L2			
3	GPS L1 + Galileo E1	4 MHz	50 MHz	Dual frequency, high precision, high bandwidth
	GPS L5 + Galileo E5a			
4	GPS L1 + Galileo E1	4 MHz	120 MHz	Triple frequency ambiguity resolution, ultra-high precision, ultra-high bandwidth,
	GPS L2			
	GPS L5 + Galileo E5a + Galileo E5b	55 MHz		

The PIF receiver is shown in Figure 8-11 connected to a Zarlink GP2010 RF front-end for GPS testing. The IF GNSS signal is fed into the receiver's 12-bit ADC (AD9430), which is a high-speed device from Analogue Devices capable of sampling frequencies up to 210 Msps. Normally the ADC and AGC are provided by the receivers RF front-end architecture. However, no RF front-ends suitable for the signal bandwidth detailed in Table 8-4 were available during this research. Therefore, it was necessary to implement a high-speed, multi-bit ADC with large dynamic range and perform digital AGC in the correlator section.

**Figure 8-11, Prototype IF GNSS receiver**

A Xilinx Virtex II Field Programmable Gate Array (FPGA) was used to incorporate all correlator functions within a single high-density chip. The FPGA is traditionally used as a development platform, allowing the designer to re-program and debug their prototype design prior to ASIC manufacture in large volumes (> 100,000 pieces). However, GNSS space receivers are rarely manufactured in large volumes and recent advances in FPGA design, increasing capacity, improving radiation tolerance and reducing power consumption, make the FPGA a practical platform for GNSS space receiver designs. For space applications with extreme radiation environments, the FPGA code was designed with the intention of implementation in an Actel RTAX series radiation tolerant chip, which is manufactured up to a two million gate capacity. FPGA's are programmed using a Hardware Description Language (HDL) allowing the following advantages in flexibility over the existing SSTL Space GPS Receiver (SGR) design.

- Absorbing changes to GNSS signal structure – An FPGA can be reconfigured to any future choice of PRN coding sequence, whether it is a stored memory code, LFSR based or a concatenated coding scheme [Pratt *et al* 2004].
- Flexible tracking techniques – The FPGA can be configured to allow adaptive tracking techniques for BOC, BCS and AltBOC modulation schemes.
- Architectures with massed correlator channels– The high density of modern FPGAs also allows more parallel search channels to be implemented than current chipsets, vastly reducing the Time To First Fix (TTFF). This is especially important for space users, where power restrictions result in intermittent usage. More tracking channels can also be useful for space applications such as GNSS attitude determination and ocean reflectometry.
- Fast Fourier Transform (FFT) search – Future GNSS implement longer PRN codes than current civil systems. Combined with the large Doppler range necessary for space users, an FFT search becomes essential for future receivers (see Chapter 10). Therefore, a number of options for an FPGA based FFT acquisition engine are being considered to reduce the computational load on the processor and reduce the receivers TTFF.

An ARM7 32-bit Reduced Instruction Set Computer (RISC) is used to perform the high-speed receiver processes and low-rate navigational processes. The

microprocessor of a GNSS receiver is required to perform rapid interrupt driven updates to sustain the receiver processes and maintain tracking loops for all receiver channels. The processor must also perform navigational processes such as data demodulation, frame synchronisation, pseudorange and Doppler formation, all essential in order to form a navigational solution. The navigational processes generally occur at a relatively sedate speed (1-10 Hz), due to the low data rate of GNSS signals, compared to the rapid update (1000 Hz) rate of the receiver tracking processes.

The PIF receiver is designed to receive high bandwidth GNSS signals, up to 20 MHz bandwidth. The sampling frequency (50 MHz) is chosen in order to enable the receiver to process signals from the SSTL IF GNSS signal generator and the SSTL MFUU signal generator. The MFUU is capable of producing Galileo signals at an IF of 61.38 MHz. The frequency plan for receiving MFUU signals is shown in Figure 8-12.

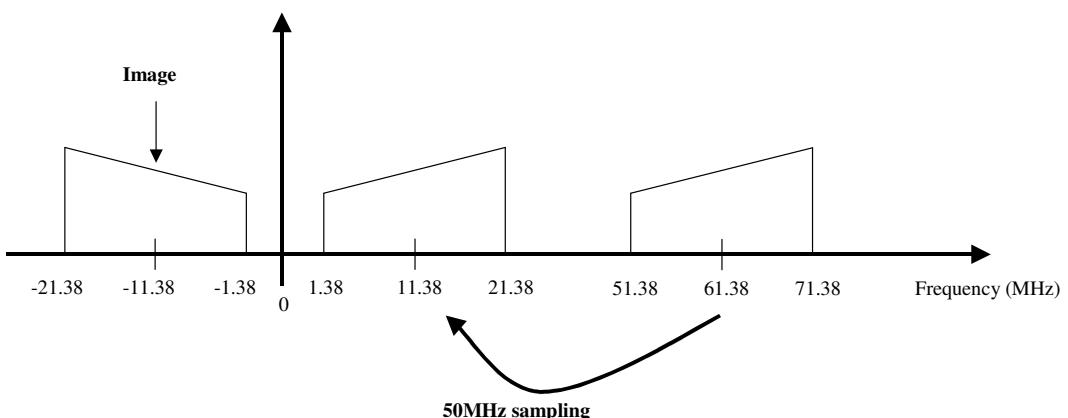


Figure 8-12, Frequency plan for receiving MFUU signals

Sampling the signal at a lower rate than the IF performs digitisation and frequency translation in a single step, this is called ‘sampling translation’. When under-sampling the IF carrier in this way the designer must be careful to avoid aliasing with other sampled products. To choose a suitable under-sampling frequency first the sample rate f_s , must satisfy the Nyquist criterion as follows.

$$f_s \geq 2 \times B$$

B is the two-sided signal bandwidth. Then to avoid aliasing while under-sampling, the sampling frequency must meet the following criterion [Lyons 2004].

$$\frac{(2 \times f_0) - B}{m} \geq f_s \geq \frac{(2 \times f_0) + B}{m + 1} \quad \text{8-30}$$

where m is an arbitrary positive integer and f_0 is the down-converted signal centre frequency . For under-sampling the prototype IF receiver the MFUU signal, with an IF of 61.38 MHz, $m = 2$ and bandwidth of 20 MHz Equation 8–30 becomes

$$51.38 \geq f_s \geq 47.5 \quad \text{8-31}$$

Therefore, $f_s = 50$ MHz seems a good choice.

The SSTL IF signal generator is capable of producing GNSS signals at an IF of 20.46 MHz. If the receiver is sampling at 50 MHz we are now over-sampling the signal and the highest frequency component faithfully represented without aliasing is 25 MHz from Equation 8–29. Therefore, the receiver can process signal from the IF signal generator with bandwidths ± 4.54 MHz around the carrier or 9.08 MHz two-sided bandwidth.

8.4 Correlator design for the PIF receiver

The FPGA correlator design is depicted in Figure 8-13. A 2-bit interface to a GPS RF front-end is maintained for testing with GPS simulators and real signals. The digital front-end reduces the quantisation level of the signal to either a single bit with no gain control or two bits with digital AGC dependant on the incoming signal level.

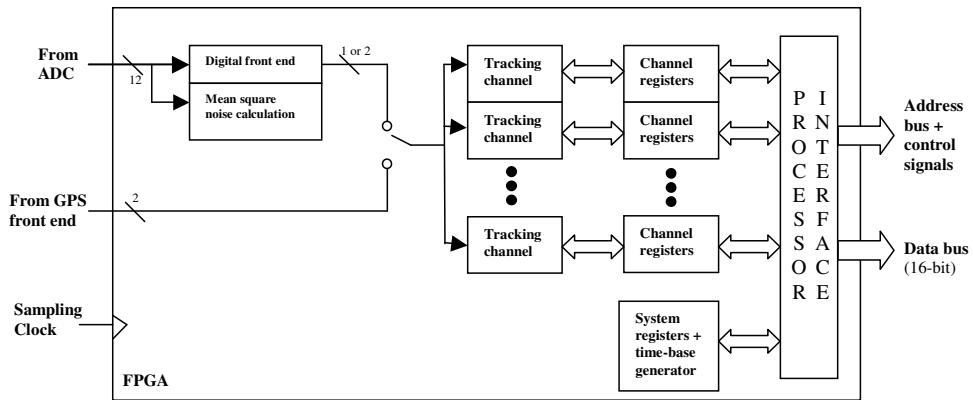


Figure 8-13,Top level FPGA correlator architecture

The digitised input signals are fed to each tracking channel. System registers are used to provide global timing signals and debug modes. Similar to the GP2021 correlator two timing signals are sent to processor, a fast rate interrupt for accumulation values and a lower rate interrupt from measurement data. Tracking channels have a number of associated channel registers, which store raw data from each correlation channel. A full description of the system and channel registers is given in Appendix G. The tracking channel architecture is shown in Figure 8-14. This is equivalent to the DE BOC correlator structure shown Figure 6-8.

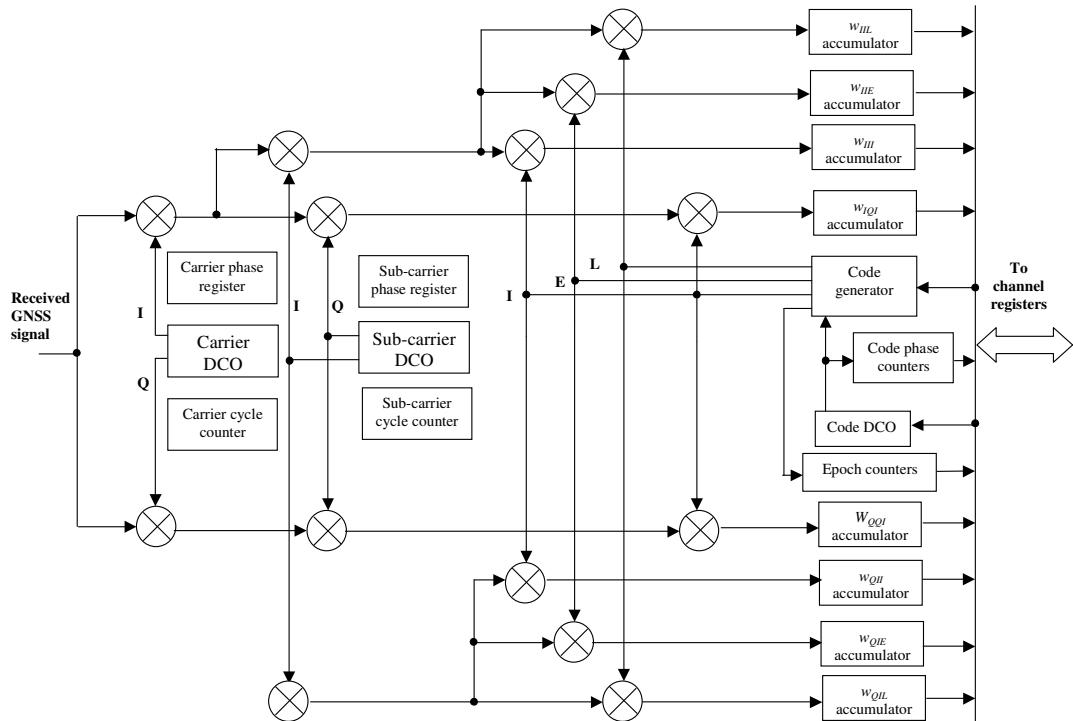


Figure 8-14, IF receiver tracking channel

The number of tracking channels available for the receiver is strongly dependant on the size and architectural components of the FPGA chosen. For example, some FPGAs have built in multiplier blocks while others will have to synthesise multipliers using logic. Therefore, the number of logic gates available to a specific chip only gives a very rough estimate of device utilisation. To provide proper comparison one must look to into the actual hardware requirements of each channel. Table 8-5 shows the hardware requirement for each tracking channel of the PIF receiver with comparison against an equivalent PSK tracking channel operating at the same sampling rate.

Table 8-5, IF receiver hardware requirements per tracking channel

Components	Size	Number required per channel	
		PSK	BOC + PSK
Multipliers	4x2	4	8
	2x2	0	4
	2x4	2	2
Digitally Controlled Oscillators (DCO)	31 bits (frequency resolution = 23.03 MHz)	2(Carrier and Code DCO's)	3 (Carrier, Subcarrier and Code DCO's)
Accumulators	19 bits	4	8
Counters	21 bits (carrier cycles in 100ms)	1	1
	20 bits (subcarrier cycles up to 10.23MHz)	0	1
	20 bits (code chips up to 10.23Mcps)	1	1
	11 bits (epoch counter 1ms epochs)	1	1
Registers	31 bits (phase register)	2(Carrier and Code DCO phase)	3 (Carrier, Subcarrier and Code DCO phase)

The tracking channels were synthesised for the Xilinx Virtex II FPGA, implementing a single tracking channel and then 2 tracking channels. Then the maximum number of channels can be accurately estimated for this family of FPGAs. Table 8-6 shows the FPGA utilisation for the Virtex II device. The figure of interest is the number of 4 input Look-Up-Tables (LUT), which is the resource most readily consumed by an increase in channels. From this we can estimate 19 PSK channels or 13 BOC in a 1 million gate device, 39 PSK or 27 BOC in a 2 million gate device.

Table 8-6, Xilinx Virtex II FPGA utilisation for PSK and BOC channels

Logic utilisation	PSK					
	1 channel			2 channels		
	Used	Available	Utilisation	Used	Available	Utilisation
Number of Slice Flip Flops	684	10,240	6%	1126	10,240	10%
Number of 4 input LUTs	870	10,240	8%	1384	10,240	13%
Number of bonded IOBs	88	172	51%	88	172	51%
Number of MULT18X18s	2	40	5%	4	40	10%
Number of GCLKs	2	16	12%	2	16	12%
Number of DCMs	1	8	12%	1	8	12%
Number of occupied Slices	653	5,120	12%	833	5,120	16%
Logic utilisation	BOC + PSK					
Number of Slice Flip Flops	1,041	10,240	10%	1,673	10,240	16%
Number of 4 input LUTs	1,266	10,240	12%	1,996	10,240	19%
Number of bonded IOBs	88	172	51%	88	172	51%
Number of MULT18X18s	2	40	5%	4	40	10%
Number of GCLKs	2	16	12%	2	16	12%
Number of DCMs	1	8	12%	1	8	12%
Number of occupied Slices	941	5,120	18%	1,487	5,120	29%

8.5 Processor design for the PIF receiver

At a low level the processor must calculate the updates and take essential measurements from the tracking loops. In addition, the navigational data must also be decoded in order to perform a navigational solution.

When acquiring and tracking PSK signals the processor commands the correlator in the similar manner as the SSTL SGR receiver. The signal search process is performed using a serial code slew, shifting the code in half chip increments. The frequency is searched in bins $\frac{1}{2} \times T$ Hz bins, where T is the integration period.

Comparing the correlation given in Equation 8–2 to a threshold value it assesses the presence or absence of a PSK signal. When a signal is declared present the carrier DCO value is initialised with the frequency of the current search bin and the code DCO is initialised with the code offset plus the current frequency offset (Doppler)

scaled down to the code frequency. The signals are then acquired using a FLL/PLL combination for carrier tracking and a DLL for the code tracking. The quality of tracking is assessed using the formula given in Equation 8–24 for code tracking, Equation 8–27 for frequency tracking and Equation 8–28 for phase tracking.

The PIF receiver acquisition and tracking sequence for PSK signals is shown in Figure 8-15.

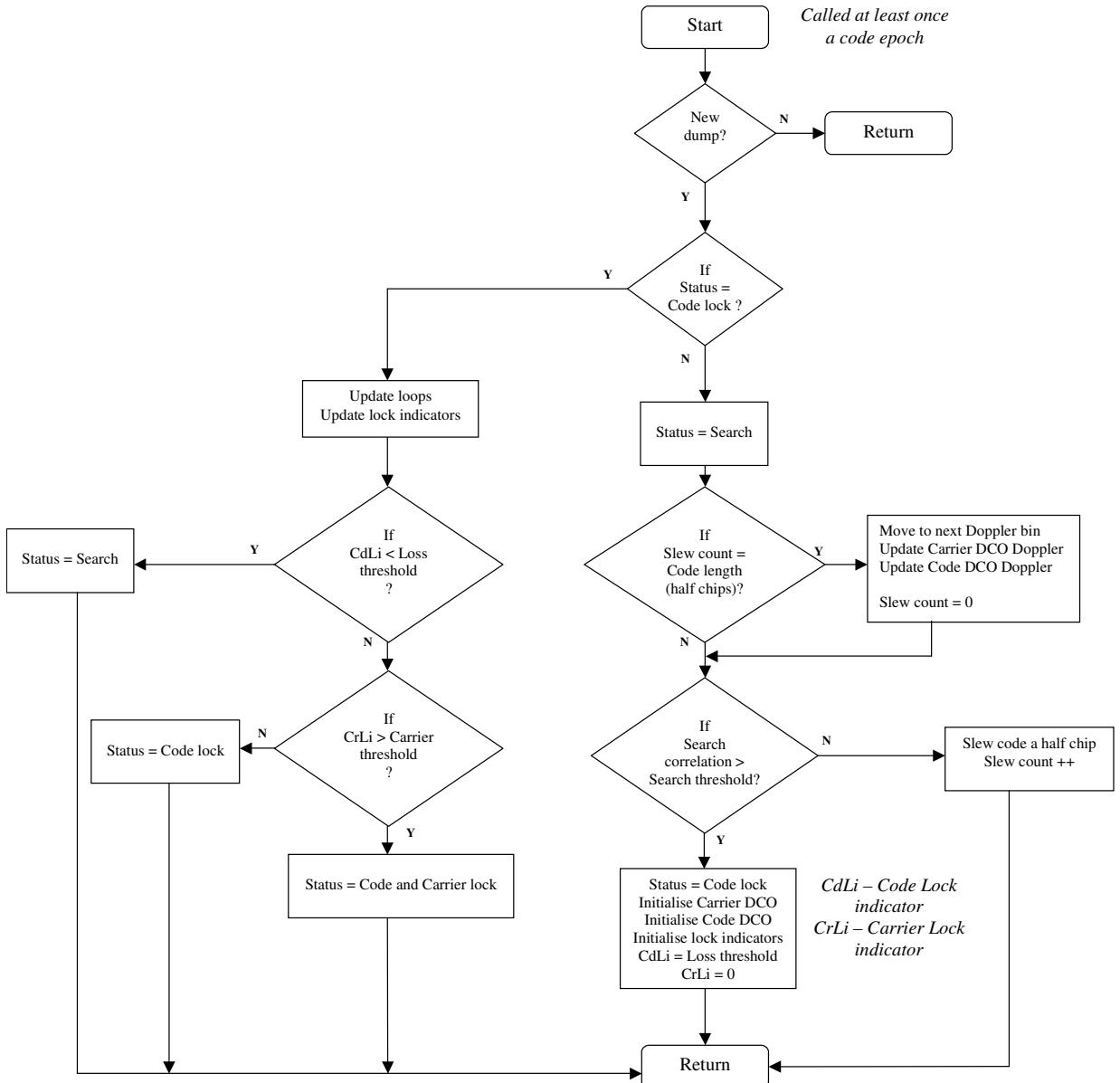


Figure 8-15, Interrupt driven acquisition and tracking for PSK signals

When searching for BOC signals the carrier and code bin width is unchanged from PSK. Despite this, as described in Section 5.3 we must create a single correlation peak by combining the in-phase BOC correlations with the quadrature BOC correlations as follows.

$$w_{SBOC} = \sqrt{w_{III}^2 + w_{QII}^2} + \sqrt{w_{IQI}^2 + w_{QQI}^2} \quad 8-32$$

The IF receiver acquisition and tracking sequence for BOC signals is shown in Figure 8-16. During the search process the BOC sub-carrier is kept locked to the code, both signals being derived from a common DCO. When a signal is detected, the carrier DCO is initialised with the value of the current search bin. The sub-carrier DCO is initialised with an appropriate Doppler scaled down to the sub-carrier frequency. The code DCO is initialised with the code offset plus estimated Doppler scaled down to the code frequency. A command is then sent to the correlator to unleash the sub-carrier. Subsequently the timing of the correlating sub-carrier is based purely on the sub-carrier DCO and is independent of the state of the code DCO. A Sub-carrier Locked Loop (SLL) must also now be operated to maintain lock on the signal. The quality of the sub-carrier phase tracking is computed by subtracting the correlation power in the quadrature BOC correlations (w_{IQI} and w_{QQI}) from the power of the in-phase correlations (w_{III} and w_{QII}). This is similar to the PLL lock indicator where the contribution of the quadrature correlation is monitored to observe any deviation from zero. The sub-carrier lock indicator used in the IF receiver is given by

$$S_{bLi} = S_{bLi} + \left(\frac{\left[(w_{III}^2 - w_{IQI}^2) + (w_{QII}^2 - w_{QQI}^2) \right] - S_{bLi}}{4096} \right) \quad 8-33$$

The quadrature carrier correlations w_{QII} and w_{QQI} are included if operating with incoherent FLL carrier tracking.

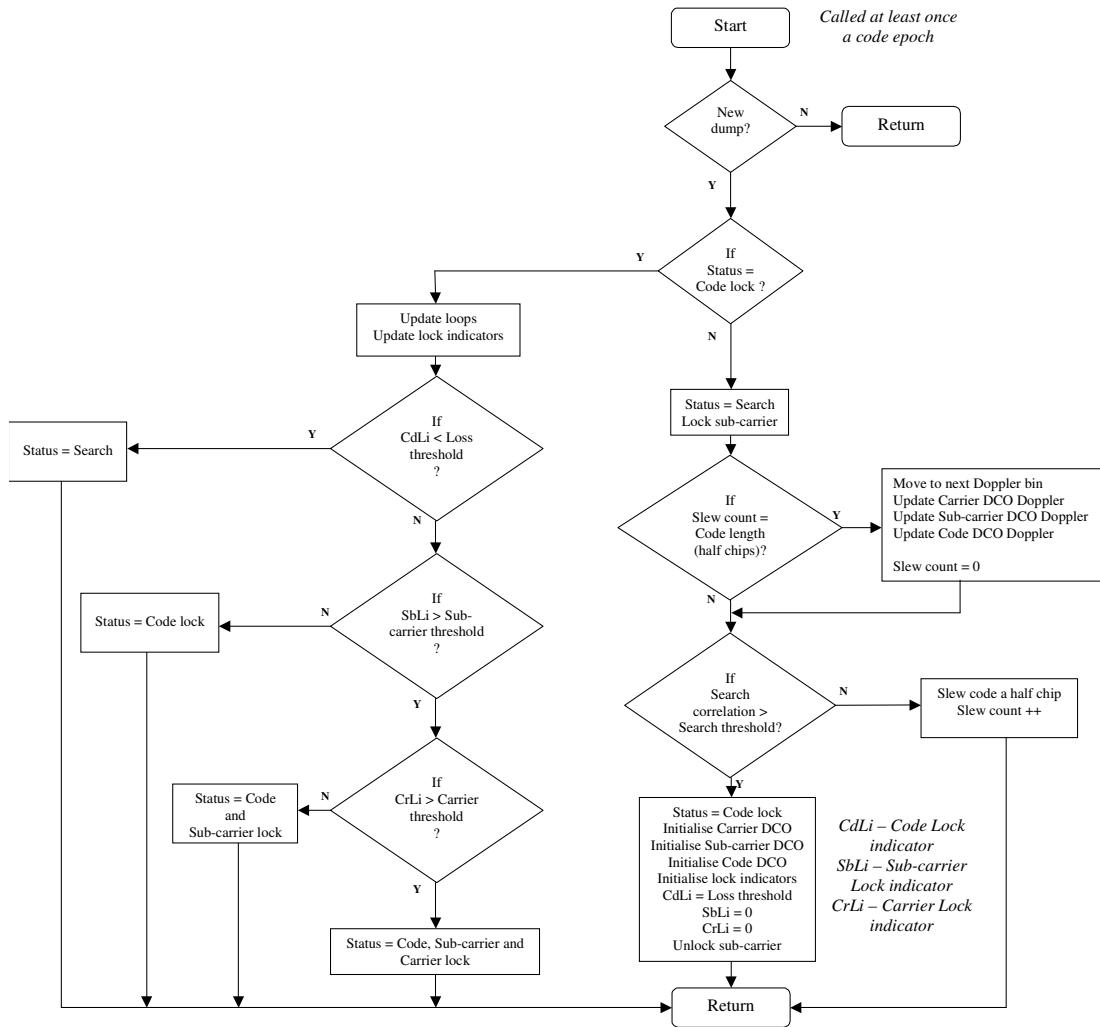


Figure 8-16, Interrupt driven acquisition and tracking sequence for BOC signals

The update equations for the carrier and code loops are based on the SGR loops, detailed in Section 8.2. As shown in Chapter 6 the SLL can be kept as a first order loop if receiving Doppler aiding from the carrier loop. The update equation for the SLL is then equivalent to the DLL update (Equation 8-22) with appropriate scaling of the Doppler estimate to the rate of the sub-carrier. Table 8-7 lists the loop parameters and loop update equations used in the IF receiver.

Table 8-7, Loop parameters and update equations

Loop	Update equation	Reference	Loop bandwidth - B_L , Damping factor - ξ
FLL	$e_\phi \leftarrow e_\phi + e_\omega$ $\hat{\phi} \leftarrow \hat{\phi} + k_1 \times e_\phi$	Equation 8-10	$B_L = 31.25$ Hz (wide) $B_L = 1$ Hz (narrow)
PLL	$f_\phi \leftarrow f_\phi + e_\phi$ $\hat{\phi} \leftarrow \hat{\phi} + k_1 \times f_\phi + k_2 \times e_\phi$	Equation 8-17	$B_L = 14.72$ Hz $\xi = 1.04$
SLL	$\hat{\tau}^* = \hat{\tau}^* + k_\phi \times f_\phi + k_\tau \times e_{\tau^*}$	Equation 8-22	$B_{SLL} = 1$ Hz
DLL	$\hat{\tau} = \hat{\tau} + k_\phi \times f_\phi + k_\tau \times e_\tau$	Equation 8-22	$B_{DLL} = 1$ Hz

This chapter has given a detailed description of the hardware and software of the SSTL SGR receivers and the PIF receiver. The PIF receiver, which was created during this research, provides a demonstration platform for the DE BOC tracking technique. The changes to hardware correlator design and software-tracking process required by future GNSS signal have been outlined in this chapter. In particular the adaptations required to implement the DE BOC tracking technique have been described. The FPGA-based correlator architecture provides future SSTL receivers a flexible core capable of receiving and processing the future GNSS signals. The extension of this concept to a single FPGA-based GNSS correlator and processor is shown in Chapter 10. Testing of the PIF receiver and the DE BOC tracking technique is shown in the following chapter.

9 Prototype receiver testing and results

This Chapter describes the testing strategy and the results derived from the PIF receiver. Firstly, the verification of the receiver design for existing GPS PSK signals is described. This was achieved using the SSTL Spirent STR4760 GPS simulator and live GPS signals from space. Secondly, a description of testing of PSK and BOC signals using the IF signal generator is given. The implementation of the DE BOC tracking technique is emphasised with in-depth details of the formation of DE measurements and performance testing of this technique. The results are compared with theoretical predictions with a detailed explanation of the receivers tracking loops necessary for this comparison.

9.1 AGC and GPS testing

Evaluating and verifying the receiver performance for PSK signals is simplified due to the current availability of GPS simulators. SSTL have three such simulators, manufactured by Spirent Communications (STR4760 (16 channels), STR4500(12 channels), STR4775(1 channel)), all of which are hardware simulators capable of producing representative RF GPS signals with accurate modelling of the receiver environment. A rooftop antenna was also used to verify receiver operation with live GPS signals. However, for receiver evaluation the simulator provides far more flexibility than live signals. The simulator can be pre-programmed with a scenario describing the movement of the receiver and GPS constellation. Changes in receiver attitude, accelerations and atmospheric variations can also be pre-programmed and the simulator has the capability to operate in a single channel mode where satellite PRN code, signal strength and Doppler offsets can be varied manually.

The Zarlink GP2010 RF front end has an IF output (4.309 MHz) suitable for feeding directly to the ADC of the IF receiver. Therefore, this front end was selected to enable testing with the SSTL simulators and real live signals. The lab setup is shown in Figure 9-1. A PC is used to download, run and monitor the output of the receiver through the serial UART interface.



Figure 9-1, Prototype receiver GPS PSK test setup

The ADC accepts signals up to 1.3 V peak-to-peak, centred at ground, with $50\ \Omega$ termination in low gain mode and signals of 0.7V peak-to-peak in high gain mode. The GP2010 provides a peak-to-peak voltage of between 0.09 V and 0.18 V into a $50\ \Omega$ termination. Therefore, the high-gain mode was selected. The signal is quantised to 12-bits and output using an offset binary data format (0 to 4095). In order to correctly emulate a GNSS receiver, the FPGA correlator in the PIF receiver must provide digital AGC (automatic gain control) to adjust for changes in the signal power level. Therefore, it is desirable to re-quantise the signal to 2-bits, representing the sign (SIGN) and magnitude (MAG) of the incoming signal. The SIGN bit is simply taken as the MSB of the data from the ADC.

The MAG is determined by averaging the bottom 11-bits of the ADC over a number of input samples, effectively setting the response time for the digital AGC. The response time of the AGC must be considerably less than the settling time of the receiver's tracking loops but large enough to remove noisy measurements. Generally, RF front architectures use AGC time constants from 1 ms to 10 ms [Zarlink 2005] [Nemerix 2005]. To enable the FPGA to run at high frequencies ($>50\text{MHz}$) the

number of samples is kept to a power of 2 and the update rate was set to 1.3 ms. The distribution of the digital AGC is shown in Figure 9-2.

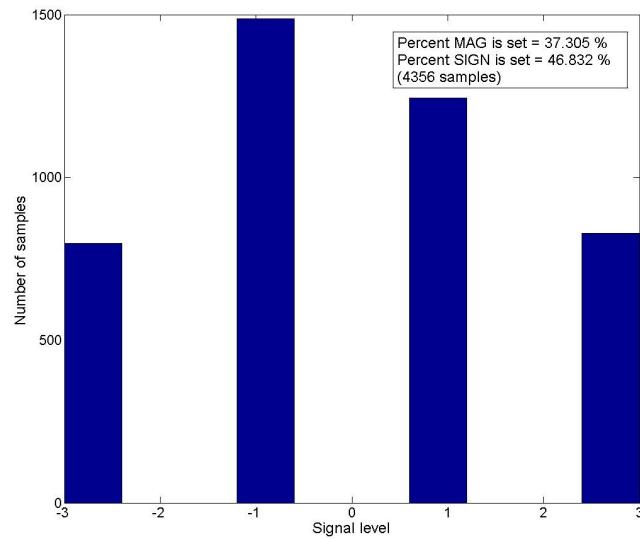


Figure 9-2, Distribution of digital AGC

Using the mean square accumulation values given in Table 8-3, with the statistical distribution given in Figure 9-2, the noise floor of the IF receiver can be calculated as follows.

$$NF_{IF} = 2 \times (0.37 \times 22.5 + (1 - 0.37) \times 2.5) \times f_s \times T = 990,000 \quad \text{9-1}$$

This noise floor value can be verified by measuring the mean square of the I (w_{II}) and Q (w_{QII}) correlations when correlating thermal noise at the receiver input. Figure 9-3 shows I and Q samples taken every second for a ten-minute data set, which through many trials was found to achieve good agreement with the theoretical noise floor value.

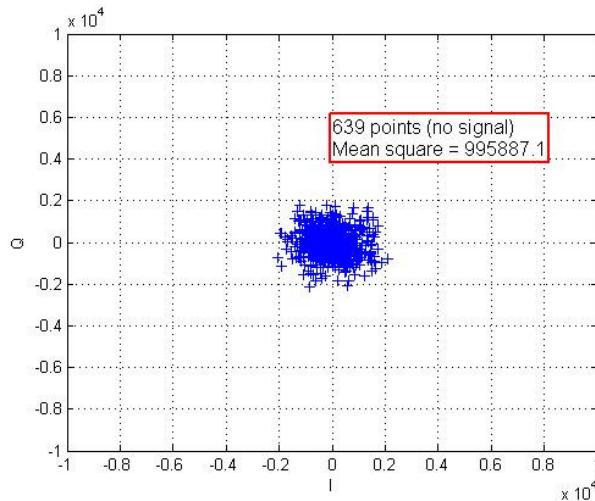


Figure 9-3, IF receiver noise floor with no signal present (50 MHz sampling)

The typical output of the IF receiver in PSK mode is shown in Figure 9-4. In this case 2 channels have been implemented and both are tracking the same SV at a signal to noise ratio of around 14.4 dB, which by Equation 8–26 ($T = 1 \text{ ms}$) corresponds to a carrier to noise of 44.4 dB-Hz. Pseudorange is given in metres and integrated carrier phase in cycles. The FLL and PLL counts allow us to monitor the acquisition status of the signals by counting how many epochs out of a thousand the tracking loop is using either FLL or PLL. Other outputs such as the raw correlation values and input signal samples may also be output.

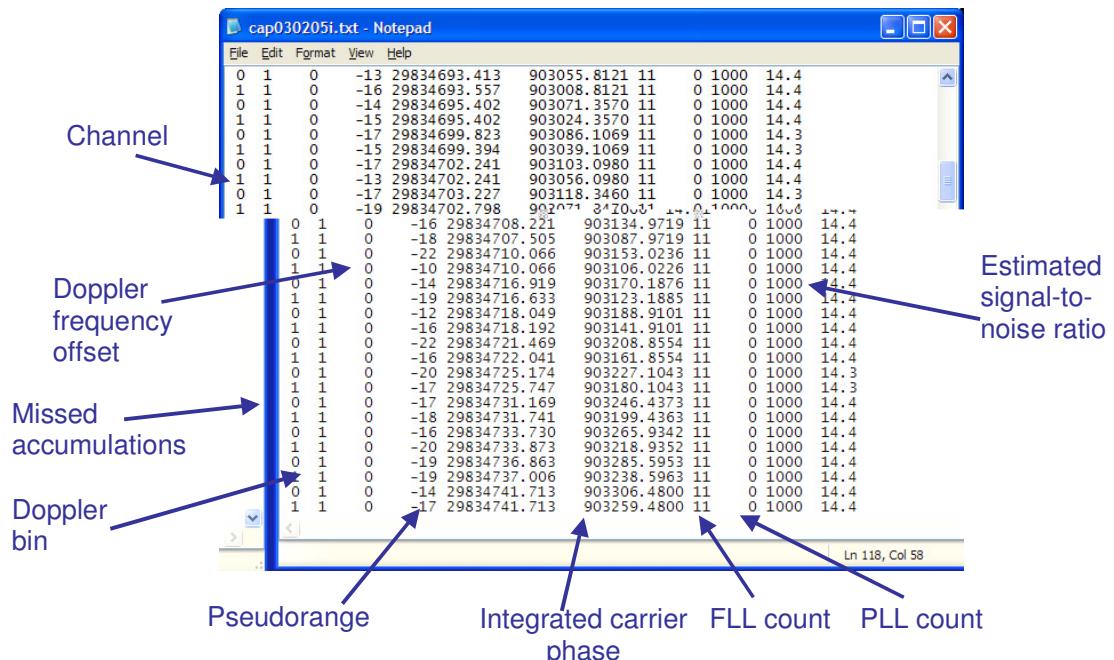


Figure 9-4, Typical PIF receiver output in GPS operation

The measurement period, a TIC, is $1/10^{\text{th}}$ of a second, although the data is normally output every second to reduce loading of the processor. The pseudorange ρ_i , is measured by calculating the time of flight of the GNSS signal as follows [Kaplan and Hegarty 2006].

$$\rho_i(n) = c \times (T_R(n) - T_{Ti}(n)) \quad (\text{m}) \quad \text{9-2}$$

$T_R(n)$ is the time based on the receiver's clock at epoch n , $T_{Ti}(n)$ is the time of transmission the signal based on the clock of the transmitting satellite i and c is the speed of an electromagnetic wave in a vacuum. In a cold start situation, $T_R(n)$ must be a guess, normally $T_{Tr}(n)$ plus a nominal propagation time. Assuming proper synchronisation with the incoming signal, $T_{Ti}(n)$ is determined from the 20ms and 1ms epoch counters (X_{E20} and X_{E1}), half chip counter (X_{HC}) and code DCO phase (τ_{DCO}) in milliseconds from the correlator sampled on a TIC. For GPS C/A code the transmit time (ms) is calculated as follows.

$$T_{Ti}(n) = (20 \times X_{E20}) + X_E + \frac{X_{HC}}{2046} + \tau_{DCO} \quad (\text{ms}) \quad \text{9-3}$$

A more generic approach, applicable to all GNSS signals can be written as

$$T_{Ti}(n) = (L_D \times X_D) + \frac{1}{L_E} \times \left(X_E + \frac{X_{HC}}{N_{HC}} \right) + \tau_{DCO} \quad (\text{ms}) \quad \text{9-4}$$

L_D is the length of one data bit in milliseconds, X_D is the data bit counter, L_E is the length of one code epoch in milliseconds and N_{HC} is the number of half chips in a code epoch.

The integrated carrier phase or integrated Doppler measurement is a measure of the number of carrier cycles between two measurement intervals. It is formed from the carrier cycle counter (X_{CC}) and the carrier DCO phase from the correlator sampled on a TIC. The cycle counter is reset every TIC and the fractional phase is determined by

comparing the current DCO phase ϕ'_{DCO} to the previous phase value ϕ_{DCO} . If λ_c is the carrier wavelength the integrated carrier phase measurement in metres can be written as follows.

$$ICP_i = (X_{CC} + \phi'_{DCO} - \phi_{DCO}) \times \lambda_c \quad (m) \quad 9-5$$

The integrated carrier phase is used to form a precise delta range measurement between measurement intervals and velocity measurements. The noise on the carrier phase measurements is generally at least two orders of magnitude less than that of the equivalent noise on the code phase measurements. The carrier measurements are independent of the code phase measurements, therefore, the integrated carrier phase can be used to smooth the pseudorange measurements from the code loop.

It was desirable to compare the IF receiver to an SGR receiver tracking the same signal source, a ‘zero baseline’ test. This provides a ‘sanity check’ for the new FPGA correlator architecture, proving the performance of the digital section equivalent to the Zarlink chipset. The simulator RF output was fed to an LNA whose output was split in two, one end fed to the IF receiver and one end to an SGR receiver with additional gain stages bypassed. The difference in RF gains must be kept to a minimum to perform a fair comparison. The cable lengths were identical and each receiver uses identical RF front-end architectures. Therefore, any variation in signal power can only come from a difference in the gain stages between the RF front ends. Figure 9-5 shows the carrier to noise estimated by the two receivers against the output of the simulator. There is an average 0.64 dB offset between the receivers due to differences in the RF amplifiers. Removing this offset the receivers agree with each other to 0.118 dB (rms) across the data set.

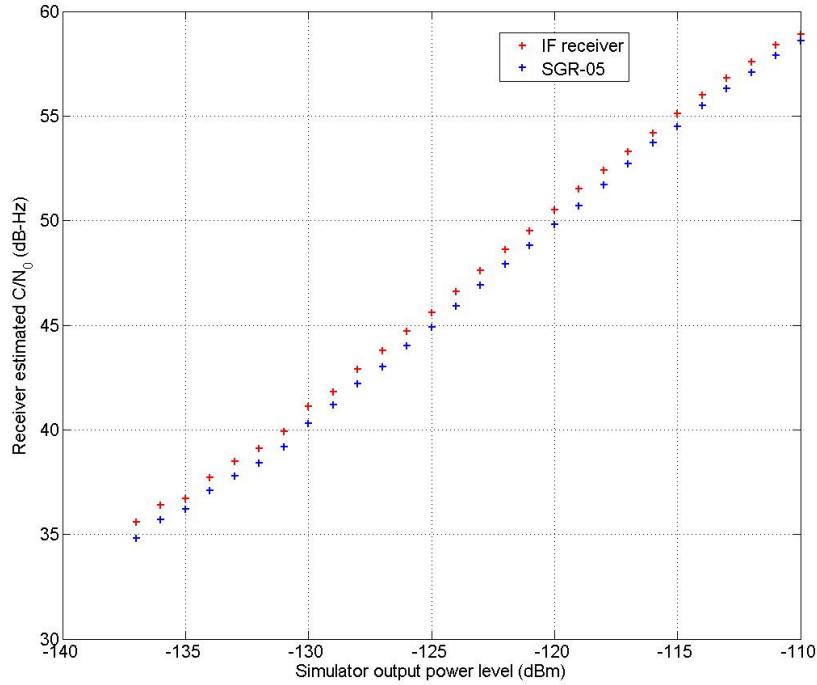


Figure 9-5, Zero baseline test between IF receiver and SGR-05

The pseudorange and integrated carrier phase is commonly used in order to measure the noise on the code tracking loop, the DLL [De Wilde *et al* 2004]. The integrated carrier phase can be used as a precise delta range measurement because noise on the carrier loop is on the order of millimetres, at least two orders of magnitude better than the code loop noise ($\approx 0.3 - 2$ m). Therefore, a good estimate of the noise of the code loop can be achieved by taking an average of the pseudorange minus the integrated carrier phase between measurement intervals. An arbitrary initial offset of carrier cycles must also be removed. It can be seen from Figure 9-6 that the noise present on the pseudorange minus the integrated carrier phase strongly agrees with theoretical predictions for PSK given by Equation 4–16. The variation between channels tracking the same incoming signal is shown to negligible (≈ 7 cm).

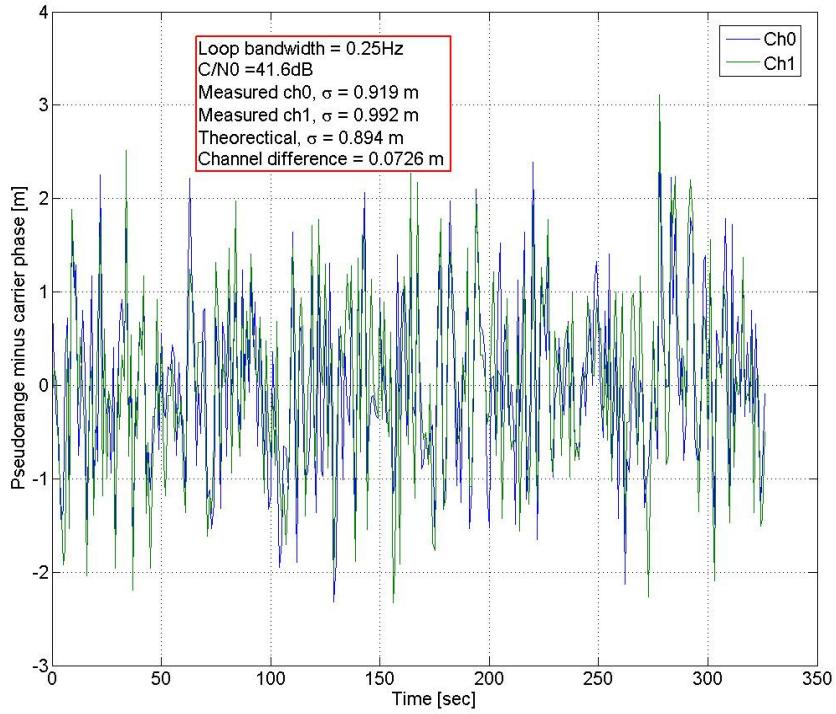


Figure 9-6, Pseudorange minus integrated carrier phase

Configuring the receiver to output raw correlation values allows the user to monitor the receiver's ability to decode the navigational data. This is achieved through an I/Q plot, from which the phase error can be derived. Figure 9-7 shows an I/Q plot taken from the PIF receiver at 45 dB-Hz and 34 dB-Hz carrier to noise. A carrier to noise density of 35 dB-Hz corresponds to an r.m.s. signal to noise per correlation of 5 dB for an integration period of 1 ms. Sub-frame parity errors in the decoded data occur at signal to noise levels less than 5 dB [Mitel 1996], this is illustrated in Figure 9-7 b) where noise induces a significant number samples to have incorrect sign at an equivalent signal to noise of 4 dB per correlation.

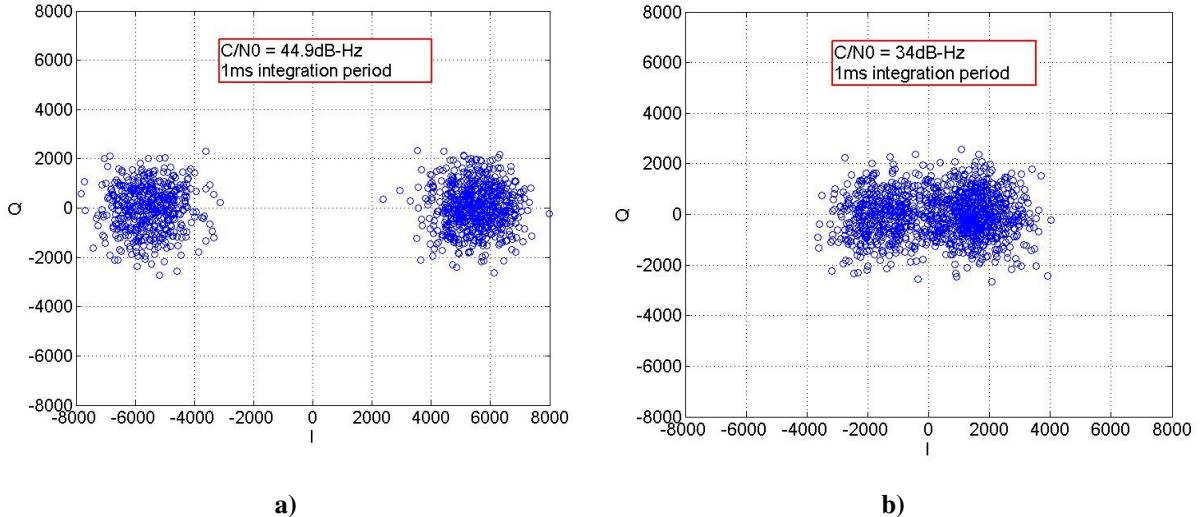


Figure 9-7. IQ plot from the PIF receiver: a) 45 dB-Hz b) 34 dB-Hz

To evaluate precisely the receiver code tracking performance against theoretically derived values we connect the receiver to the bench IF signal generator described in Chapter 7. This signal generator is capable of producing an IF GNSS signal with a precisely calibrated level of additive noise. Repeating from Equation 7–17 the carrier to noise density of the IF signal with digitally synthesized noise is given by

9-6

where A is the amplitude level given to the PRN code sequence, f_{DAC} is the DAC sampling rate, σ_N is the r.m.s. value of the synthesised noise and K_N is the noise decimation factor. We choose an IF of 20.46 MHz, a DAC sampling rate of $f_{DAC} = 81.84$ MHz and implement a noise Gaussian generator with standard deviation of $\sigma_N = 24.292$. The noise update rate was kept constant at 1.023 MHz ($K_N = 80$) and the PRN code sequence amplitude, A varied in steps of 0.5 from 1 to 16.5. The carrier to noise of the signal generator given by Equation 9–6 while generating a PSK-R(1) signal, is compared with the estimated carrier to noise from the IF receiver in Figure 9-8. The measured implementation loss is the sum of losses due to a single-bit IF up-conversion, digital to analogue conversion, RF cable loss and the conversion back from analogue to a 2-bit digital signal. After correcting for the

implementation loss the estimated carrier to noise can be seen to very accurately agree (0.24 dB r.m.s.) with the corresponding theoretical values.

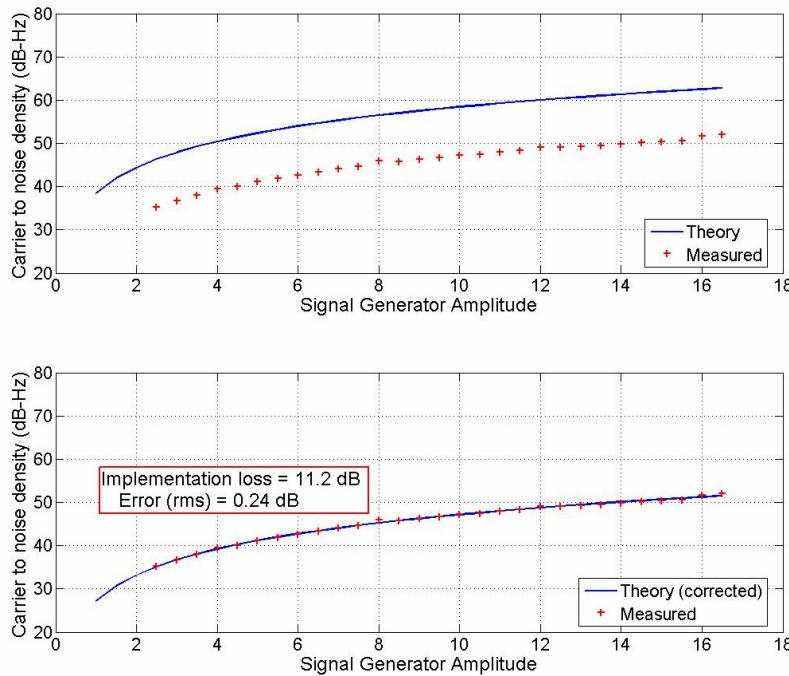


Figure 9-8, Comparison of PIF receiver estimated and theoretical carrier to noise densities for PSK-R(1)

In order to validate these results we measure the code tracking jitter at various C/N_0 levels and look for agreement with established theoretical values. The code tracking jitter can then be evaluated by examining the subtraction of pseudorange from the integrated carrier phase across a data-set of sufficient size (see Figure 9-6). Figure 9-9 shows a comparison of the code tracking measured from the receiver with the theory given for a coherent PSK DLL given in Equation 4-16. Each point on the figure represents a dataset of 8-10 minutes taking readings at 1 Hz. The receiver's code loop bandwidth is set to 1 Hz.

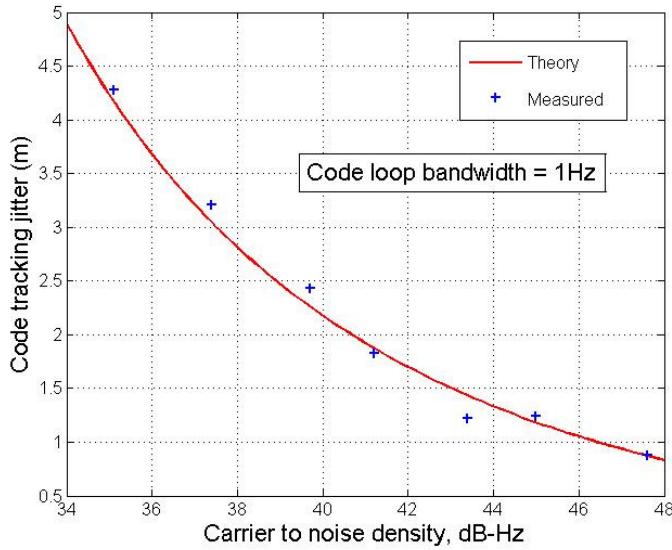


Figure 9-9, Comparison of PIF receiver estimated and theoretical code tracking jitter for PSK-R(1)

9.2 BOC measurements and testing

This section describes the demonstration of BOC signal acquisition and tracking using the PIF receiver. The measurements taken by the PIF receiver while processing BOC signals from the IF signal generator are detailed and results given.

A 2-channel receiver was configured with the first channel implementing the DE BOC tracking loops (see Chapter 6) and the second channel using the BJ algorithm (see Section 5.4). This allows cross checking between the channels to ensure correct tracking states. Acquisition is achieved by the SCC technique (see Section 5.3), which provides a single peak for robust signal acquisition.

Assuming proper synchronisation with the incoming signal using the DE BOC receiver, the transmit time of the signal, $T_{Ti}(n)$ can be determined. Similarly to PSK transmissions this is achieved by combining the values of the data counters and epoch counters, half chip counter and code DCO phase (τ_{DCO}), which can be written as follows.

$$T_{\tau_i}(n) = (L_D \times X_D) + \frac{1}{L_E} \times \left(X_E + \frac{X_{HC}}{N_{HC}} \right) + \tau_{DCO} \quad (ms) \quad 9-7$$

At the time of measurement this is entirely equivalent to the delay estimate from the DLL loop of the DE BOC receiver, denoted $\hat{\tau}$. The SLL delay estimate, which locks onto an ambiguous integer BOC sub-chip, can be formed using the sub-carrier DCO phase (τ_{DCO}^*) as follows.

$$T_{\tau^*_i}(n) = (L_D \times X_D) + \frac{1}{L_E} \times \left(X_E + \frac{X_{HC}}{N_{HC}} \right) + \tau_{DCO}^* \quad (ms) \quad 9-8$$

The more precise SLL estimate can then be corrected by the DLL estimate to deliver the best estimate of received signal transit time as follows.

$$T_{Ti}(n) = T_{\tau^*_i}(n) - \text{round}\left(\frac{T_{\tau^*_i}(n) - T_{\tau_i}(n)}{T_s}\right) \times T_s \quad (ms) \quad 9-9$$

T_s is a sub-chip. Alternatively the more precise SLL estimate can be used in combination with the values of the sub-carrier cycle counter, X_{SC} to provide an integrated sub-carrier phase (ISCP) measurement as follows.

$$ISCP_i = (X_{SC} + \tau'^*_{DCO} - \tau^*_{DCO}) \times \lambda_{SC} \quad (m) \quad 9-10$$

τ'^*_{DCO} is the current SLL delay estimate, τ^*_{DCO} is the previous SLL estimate and λ_{SC} is the sub-carrier wavelength.

As shown in Section 6.5 any distortions in the received BOC signal can compromise the reliability of receivers operating the BJ algorithm. In the DE BOC receiver an asymmetric correlation function causes a sub-carrier to code offset, which results in a non-integer sub-chip offset between the DLL and SLL delay estimate. A small offset between the DLL and SLL estimates has been observed on the PIF receiver when tracking signals from the IF signal generator. We believe this is due to distortion in

the signal generator causes an asymmetric BOC correlation function. Asymmetry has been observed from both the BOC(1,1) and BOC(15,2.5) [Falcone *et al* 2006] signals from Giove-A.

The DE BOC receiver can measure and therefore correct for this asymmetry. Figure 9-10 shows the measured difference between the DLL estimate and corrected SLL estimate (corrected by integer sub-chips).

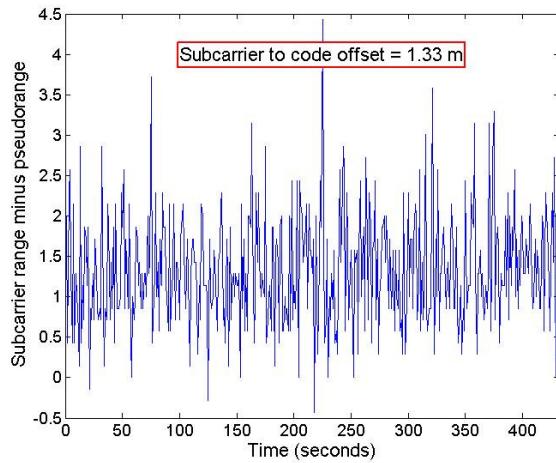


Figure 9-10, Measurement offset due to asymmetric BOC(1,1) signal

Once the DLL and SLL delay offset has been measured the receiver can be calibrated for each transmission. The transmit time corrected for asymmetry in the received signal can then be written as follows.

$$T_{Ti}(n) = T_{\tau^*i}(n) - \text{round}\left(\frac{T_{\tau^*i}(n) - T_{\tau i}(n) - \delta_{Si}}{T_s}\right) \times T_s \quad (ms) \quad 9-11$$

δ_{Si} is the asymmetry correction for the satellite i . A typical output of the PIF receiver while processing a BOC(1,1) signal is shown in Figure 9-11.

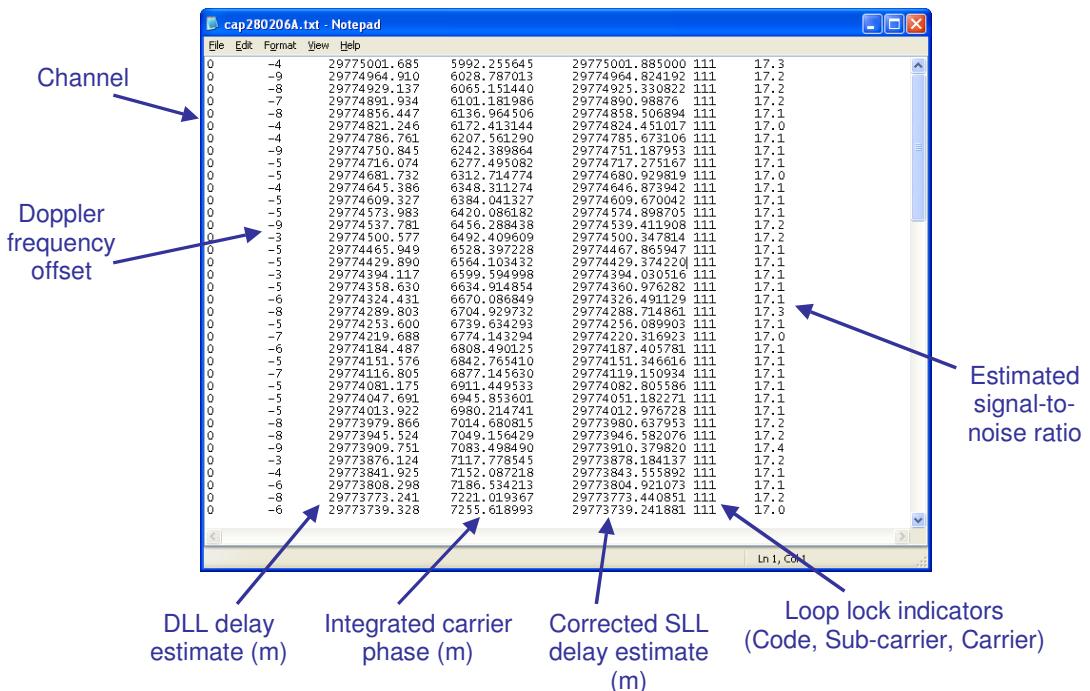


Figure 9-11, Typical PIF receiver display for BOC signals

The IF signal generator was configured to produce a BOC(1,1) modulated signal. For simplicity the same PRN codes were generated as the PSK case, a 1023 chip Gold code with a 1 ms repeat period (C/A code SV1). The PIF receiver was configured to search for the BOC(1,1) signal in half-chip code steps and 500 Hz frequency bins using the SCC BOC search technique. Both the loop bandwidth of SLL and DLL tracking loops of the DE BOC receiver channel were set to 1 Hz.

We repeat the test of Figure 9-8, comparing the receiver estimated carrier to noise density against theoretical predictions. The carrier to noise of the signal generator given by Equation 9-6 while generating a BOC(1,1) signal, is compared with the estimated carrier to noise from the IF receiver in Figure 9-12. We choose an IF of 20.46 MHz, a DAC sampling rate of $f_{DAC} = 81.84$ MHz and implement a noise Gaussian generator with standard deviation of $\sigma_N = 24.292$. The noise update rate was kept constant at 1.023MHz ($K_N = 80$) and the PRN code sequence amplitude, A varied in steps of 0.5 from 1 to 16.5. The measured implementation loss is the sum of RF cable loss and losses due to the conversion between the analogue and digital domain. After correcting for the implementation loss the estimated carrier to noise

can be seen to precisely agree (0.21 dB r.m.s.) with the corresponding theoretical values.

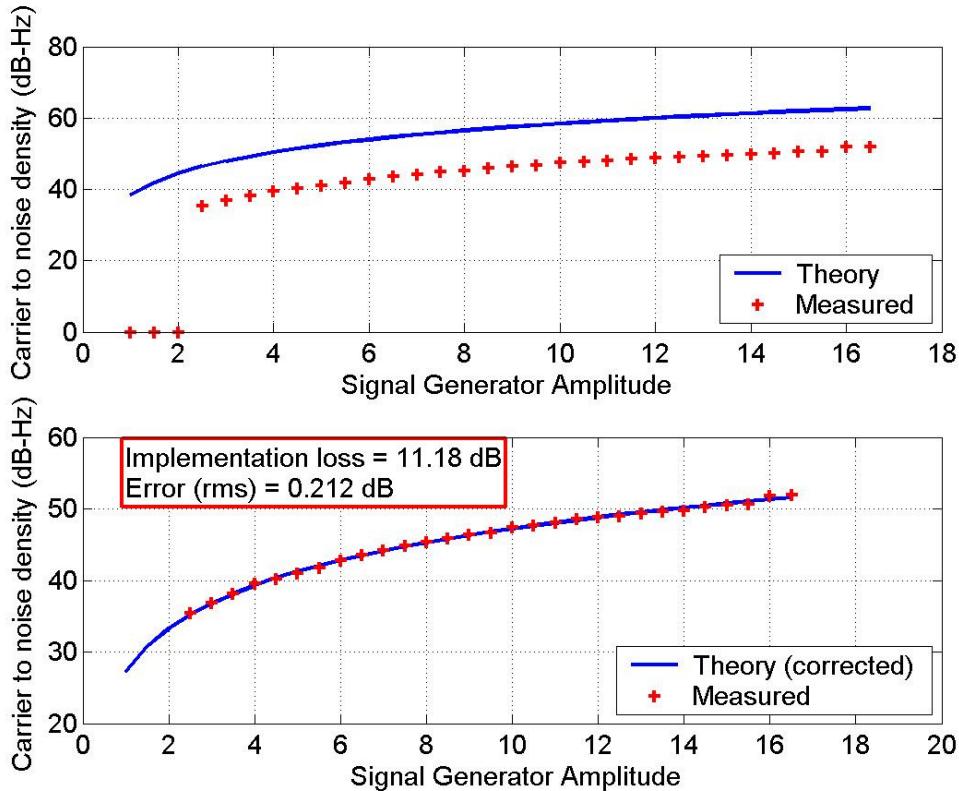


Figure 9-12, Comparison of PIF receiver estimated and theoretical carrier to noise densities for BOC(1,1)

The timing jitter of the DLL and SLL loops can be measured by subtracting the integrated carrier phase measurement from the delay estimate from each loop. An arbitrary bias of carrier cycles must also be removed. An example of the timing jitter of the DLL and SLL loops is shown in Figure 9-13.

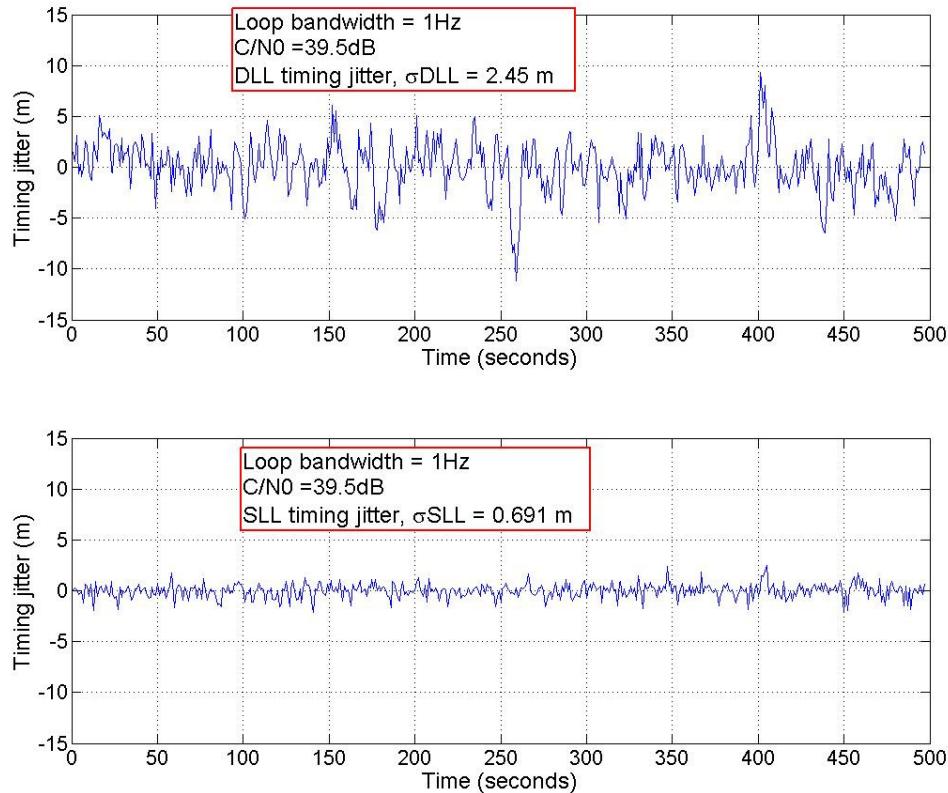


Figure 9-13, Example timing jitter of DLL and SLL loops

The DLL and SLL timing jitter were measured over a range of carrier to noise densities. Figure 9-14 shows a comparison of the receiver measured DLL and SLL timing jitter with the theory given for a coherent BOC receiver given by Equation 4–20. Each point on the figure represents a dataset of 8–10 minutes taking readings at 1 Hz. The receiver’s DLL and SLL correlator spacing were equal to a chip and a sub-chip respectively and both loop had loop bandwidths set to 1 Hz.

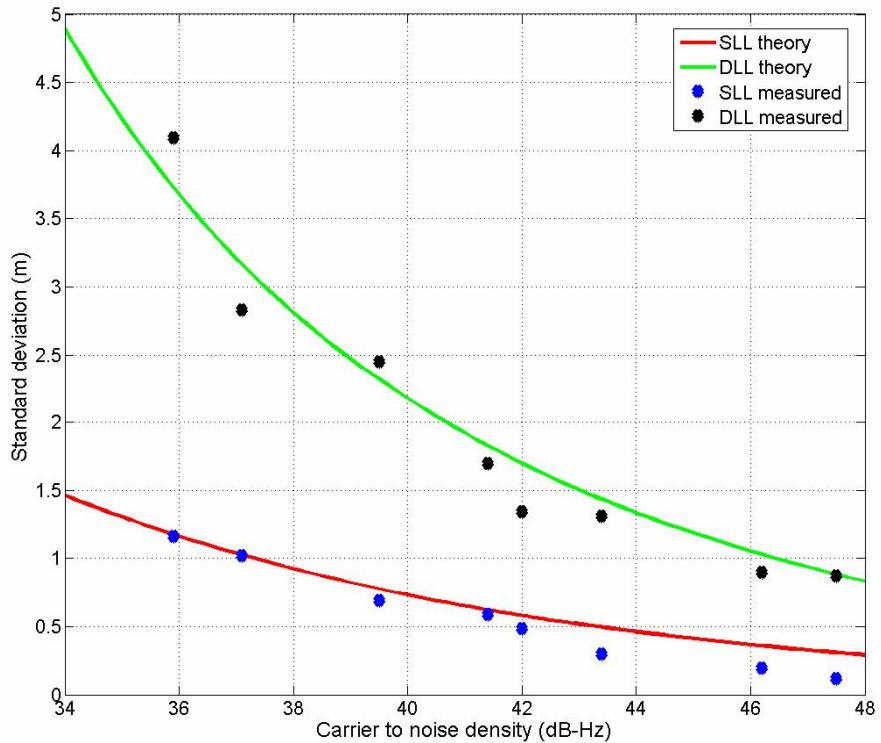


Figure 9-14, Comparison of PIF receiver estimated and theoretical code tracking jitter for

BOC(1,1) $\Delta_{DLL} = T_C$, $\Delta_{SLL} = T_S$, $B_{DLL} = B_{SLL} = 1 \text{ Hz}$.

10 Single chip GPS and Giove-A receiver

In this chapter we present a demonstration of terrestrial reception and processing of PSK signals from the GPS satellites and the BOC(1,1) signal from the Giove-A satellite. This was achieved through a prototype FPGA-based GNSS receiver, which was developed as an extension of the PIF receiver. The architecture of this receiver is described which combines the GNSS correlator and processor functions into a single system-on-chip solution suitable for space applications. This design is intended to replace the aging chipset in current SSTL SGR receivers. This demonstration provides an illustration of the practical challenges faced in receiving Galileo signals and implementing the BOC acquisition and tracking techniques developed during this research.

10.1 Single chip receiver overview

The heart of any hardware GNSS receiver is its correlator and processor architecture. Currently most GNSS receivers use Application Specific Integrated Circuit (ASIC) chipsets to perform the operations required by the correlator and processor. The mass market of terrestrial GNSS receiver has fueled development into reducing the size and power consumption of these chipsets, making a single chip baseband solution desirable. SSTL's SGR receiver uses the Zarlink chipset, which provides a single chip 12-channel receiver or two-chip 24-channel receiver. Similar chipsets such as the SIRFstarIIA [SiRF 2005] provide a system-on-a-chip (SOC) 12-channel solution. Both these chipsets use a separate RF down-conversion stage, which can generally be compressed into a small low-power package. Therefore, the SOC generally refers to the baseband section, providing a correlator and processor with in single ASIC, although a few modern ASICs have succeeded in combining the RF and baseband sections.

Traditionally FPGAs have been used for development and prototype work because of their ability to be reprogrammed. However, modern FPGA architectures, such as the Virtex 5 from Xilinx [Xilinx 2005], focus on reducing power consumption. Also,

many FPGA families prove radiation tolerant designs suitable for the harsh environments of space applications. SSTL have for many years operated both radiation tolerant and commercial one-time programmable Actel FPGAs in space. Re-programmable Actel ProASIC FPGAs have also been flown by SSTL and they have plans to use the Xilinx Virtex 4 family on future missions. Advances in FPGA technology now provide high-density low-power architectures capable of consolidating the correlator and processor architectures in a single chip. Therefore, in order to break the dependence of SSTL receivers on ASICs and provide a design suitable for the new generation of GNSS signal a single-chip FPGA solution is desirable.

FPGA families of particular interest are those developed to be compatible with soft-core processor designs. Actel have developed an ProASIC FPGA with the option of a 32-bit ARM7 TDMI soft-core processor. SSTL currently use the ARM7 in their SGR-05 receiver range and therefore this option was desirable in order to port the receiver code to the FPGA. However, this design was not available during this research and therefore other soft-core processors were considered.

The LEON project was introduced in October 1997, at European Space Research and Technology Centre (ESTEC). This internal project aimed to develop a high-performance 32-bit soft-core processor for future European Space Missions. These missions required a high-performance low-cost processor and with unrestricted long-term availability of both components and software tool-chains. The result was the LEON soft-core processor, which is free to use under a General-Purpose Licence (GPL). The third version of this core is called the LEON3 [Gaisler 2006]. Although this version of the core is still under a GPL its support is managed by Gaisler Research, who provide a complete range of supporting tools including compilers, simulators and debug applications. The architectural components of the LEON3 soft-core are shown in Figure 10-1. An attractive feature of the LEON3 is the ability to efficiently configure the core components as desired, reducing the FPGA resource consumption. The LEON3 includes a high-speed 32-bit data bus conforming to the Advanced Microprocessor Bus Architecture (AMBA) specification, which is ideal for connection to high performance units such as a GNSS correlator. An optional

floating-point unit is available which is attractive for numerically intense applications such as FFT acquisition, Kalman filtering, attitude and orbit determination.

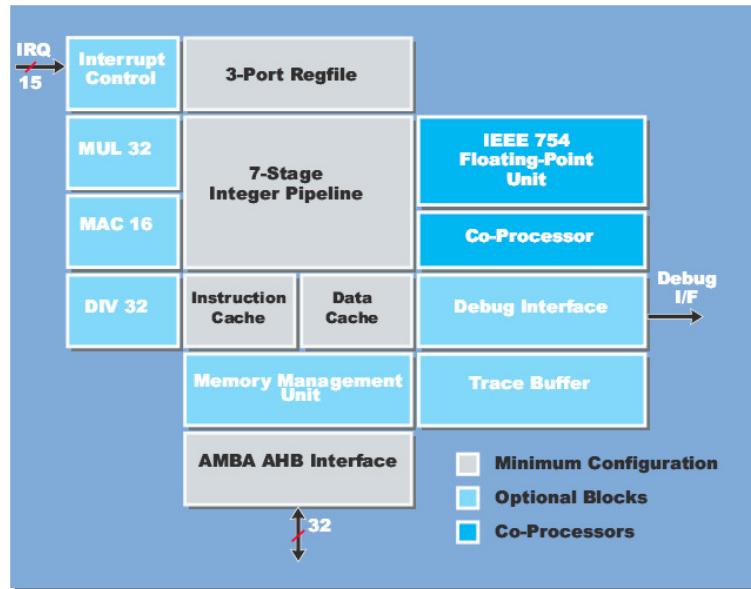


Figure 10-1, LEON3 architectural components [Gaisler 2006]

Supported by SSTL and SSC an undergraduate student project was carried out by Antonio Lopes to integrate a basic GPS correlator code with the LEON3 processor in a Xilinx Spartan 3 FPGA.

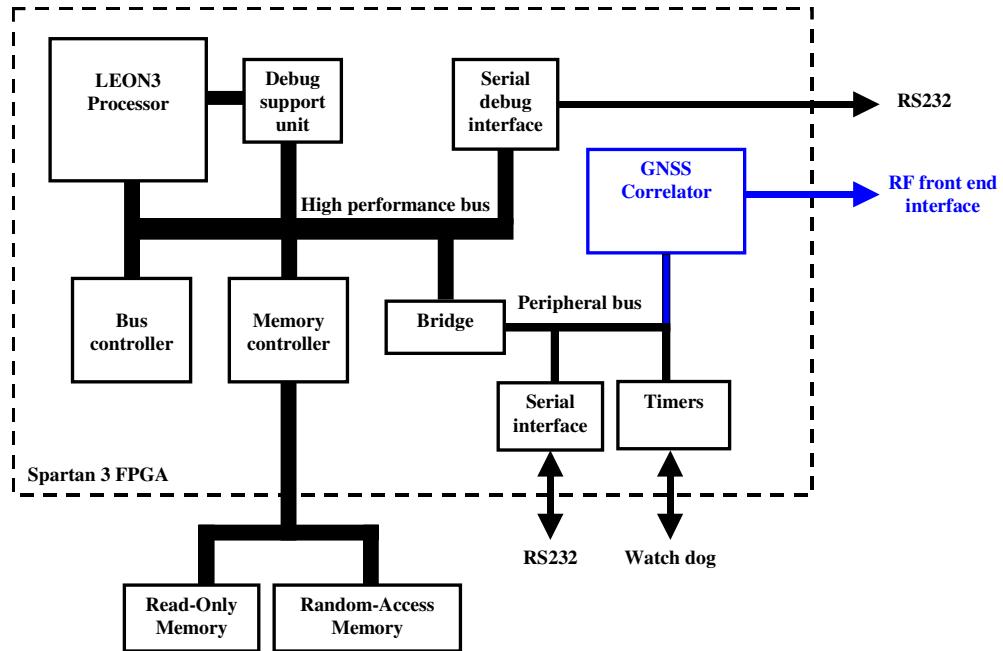


Figure 10-2, LEON3 processor with GNSS correlator

The GPS correlator combined with the LEON3 design was synthesized for a Xilinx Spartan 3 FPGA and implemented on the NuHorizons SP3-1500 development board. Figure 10-3 shows the single-chip receiver connected during testing with the GPS simulator.

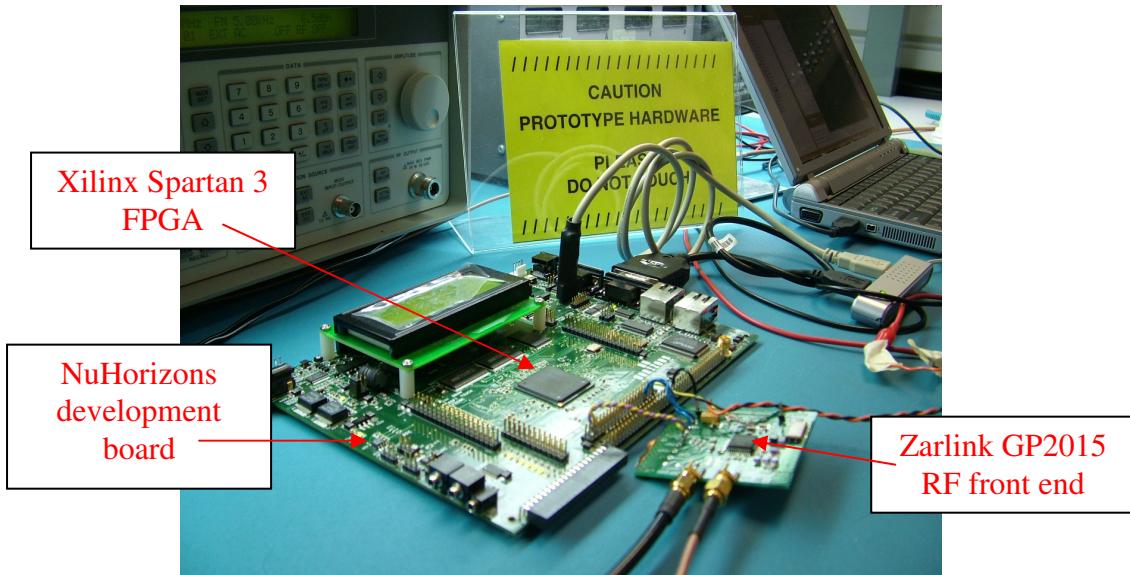


Figure 10-3, GPS testing of the single-chip receiver

Software was written to perform the basic GPS search, acquisition and tracking functions mirroring those implemented in the SGR receivers.

10.2 RF front-ends for the single chip receiver

Verification of the single-chip receiver with GPS signals was achieved using the Zarlink GP2010 RF front-end, currently used in the SGR receivers. The GP2015 mixes down the incoming L1 band carrier (1575.42 MHz) to a 2-bit sampled IF of 1.405 MHz (see Figure 10-4). The GP2010 is suitable for the GPS C/A signal, which has a PSK-R(1) modulation. However, the low sampling rate and tight IF filter (2MHz bandwidth), is insufficient to process the main lobes of the Galileo L1 B+C signal which has a BOC(1,1) modulation.

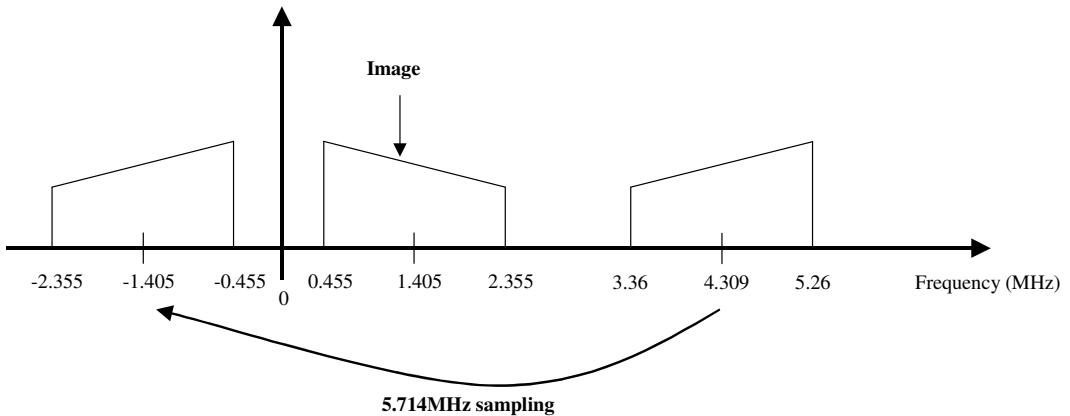


Figure 10-4, Frequency plan for GP2015

A major advantage of an FPGA-based GNSS receiver is its flexibility, which enables the designer change the RF front-end architecture with no change to the receiver's correlator hardware. Changing the RF front-end requires adapting the sampling rate and IF carrier frequency of the GNSS correlator. Increasing the sampling frequency of the correlator requires increasing the size of each channel's accumulators and may increase the size of the DCO phase registers. Therefore, increasing the sampling frequency reduces the number of channels achievable in a specific FPGA.

In order to process the Galileo BOC(1,1) signal with the single-chip receiver we use Nemerix NJ1006A RF front-end [Nemerix 2005]. This modern front-end ASIC mixes L1 band signal down to a 2-bit sampled IF of 4.188 MHz with a 3.5 MHz 3 dB filter bandwidth and a sampling frequency of 16.367 MHz (see Figure 10-5). Despite almost tripling the sampling rate of the GP2010 front-end the power consumption of the modern NJ1006A is actually one tenth of the GP2010, illustrating the advances in low-power RF front-end architectures.

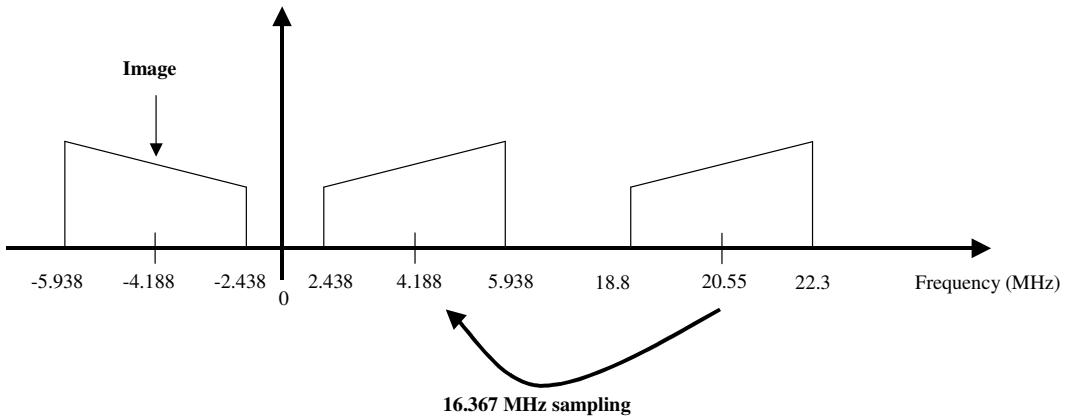


Figure 10-5, Frequency plan for Nemerix NJ1006A RF front end

10.3 Receiving the Galileo BOC(1,1) E1 signal

Demonstration and evaluation of the acquisition and tracking of the GPS C/A code signals was achieved using the SSTL 16-channel GPS simulator rooftop antenna. The Galileo signal E1 contains three components A, B and C, which are combined using Interplex modulation with a modulation index $m = 0.6155$. Substituting $m = 0.6155$ into Equation 7–8 the Galileo E1 signal with normalized power can be written as follows.

$$S_{E1}(t) = \frac{1}{3} [\sqrt{2}(b_{E1B}(t)d(t) - b_{E1C}(t))] \cos(\omega_{L1}t) + [2(b_{E1A}(t)d(t)) + b_{E1A}(t)b_{E1B}(t)b_{E1C}(t)] \sin(\omega_{L1}t) \quad 10-1$$

The open service (B + C) signals are to be transmitted with either a BOC(1,1) or MBOC(6,1,1/11) modulation. It is important to note that the data component, B and the pilot component, C are transmitted on the same carrier component. The modulation I/Q plot shown in Figure 10-6 provides an insight into the effect of the interplex modulation. The inter-modulation term is used to control the level of the quadrature contribution in order to maintain a constant amplitude. However, from the receiver point of view it is unlikely that the receiver has the capability or has access to the E1 A component, which is a PRS signal. Looking from a receiver perspective, without the A component there is no quadrature contribution as shown in Figure 10-7.

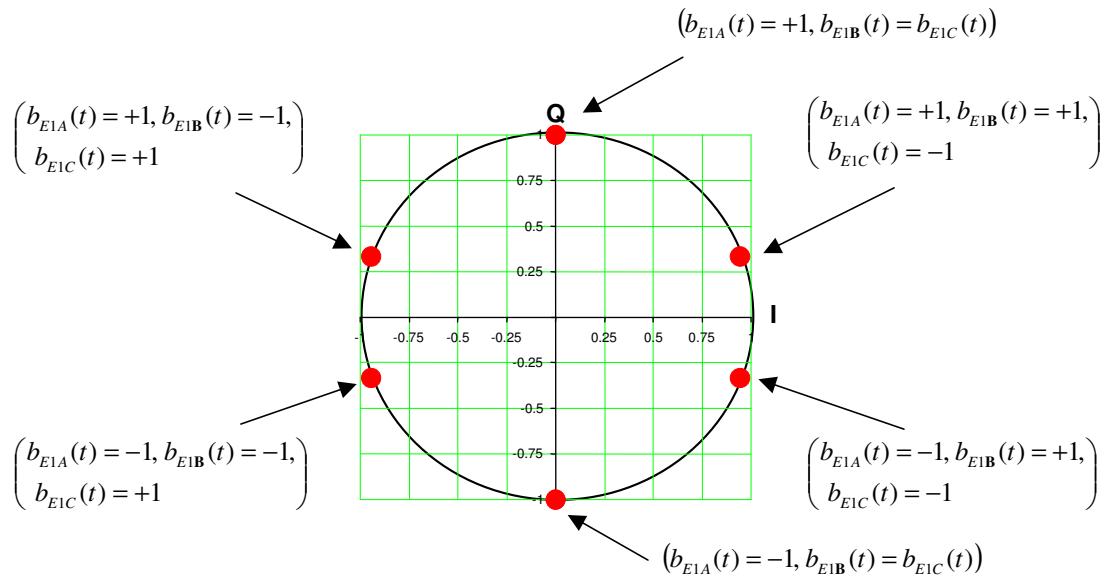


Figure 10-6, I/Q plot of Galileo E1 signal with code states (ignoring data modulation, $m = 0.6155$)

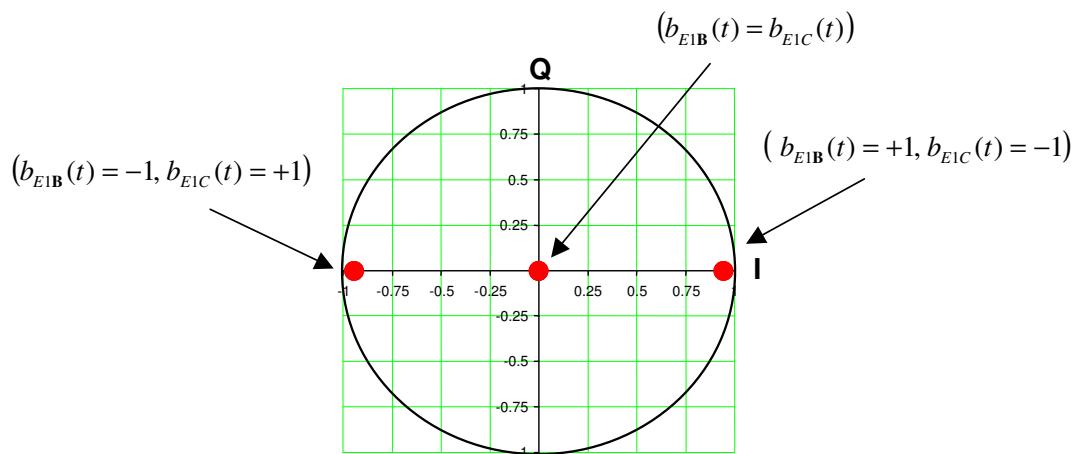


Figure 10-7, I/Q plot of Galileo E1 signal from the receiver perspective

(ignoring the A component and data modulation, $m = 0.6155$)

For the Galileo E1 signals 55. $\dot{5}$ percent of the transmitted power is given to the A component and inter-modulated product. The remaining 44. $\dot{4}$ percent is split equally between the B and C components. Code combinations correlating the addition or subtraction of the B and C components can be used to recover all of the 44. $\dot{4}$ percent of transmitter power given to these components. This is of particular importance for high-sensitivity receivers or those operating in weak signal environments. Addition or subtraction of codes can be performed prior to the accumulation in the correlator in order as in [Mattos 2005]. Equally the codes may be individually correlated and

summed after the accumulation process. Both techniques require knowledge of the polarity of the secondary code of the C components in order to recover all of transmitted power and decode the navigational data bit. In this research we have avoided using code combinations because applications for patent protection have been filed for these techniques. Avoiding code combinations also enabled comparison between the single-chip receiver and the Septentrio Galileo experimental test receiver (GETR) [De Wilde *et al* 2004].

The single chip receiver was configured to receive the Galileo E1 B data modulated signal component. The B component has a chipping rate of 1.023 MHz and a code length of 4092 chips, which results in a 4ms repeat period or code epoch. The code epoch is also equal to the symbol period of the navigational data, which is therefore modulated at a rate of 250 sps. The current Galileo E1 specification defines codes, which must be stored in receiver memory. These memory codes designed to provide balanced codes with low cross-correlation values. However, the codes transmitted by Giove-A are based on Gold codes, which are generated by shift register polynomials (see Figure 3-4). These codes were designed to be representative of Galileo signals but were not intended for public and have not been officially released. However, researchers and engineers first in the USA at Stanford University and in [Psiaki *et al* 2006] have managed to decode the transmitted PRN code sequences generally through the use of high-gain antennas.. Since then, researchers in France have also managed to decode the Giove-A PRN code. Table 10-1 shows the publicly known generator polynomial for the Galileo E1 signal transmitted by Giove-A.

Table 10-1, Galileo E1 PRN codes on Giove-A

Signal	Code length ms (chips)	Generator polynomial (hexadecimal)		Start value (hexadecimal)	Secondary code length	Secondary code bit pattern (hexadecimal)
		1	2			
E1 B	4 (4092)	26B1	31E1	1B83	1	-
E1 C	8 (8184)	201B	26B1	1983	25	7015B2

For simplicity we maintain the simple serial search. When integrating across a 1ms code period (GPS C/A) the approximate search time is 20.46sec (± 5 kHz search) assuming half-chip steps in delay and 500 Hz frequency bins. Integrating across a 4 ms code period (Galileo E1 B) results in an equivalent search time of 1309 seconds or 21.8 minutes. Clearly this is an unacceptable length of time to search for the signal. A solution is to short-cycle the code and correlate a 1 ms section of the code for acquisition. When sub-dividing into four 1ms chunks, four code shifts are searched every code epoch (4 ms). Therefore, the search time is only increased by the number of chips to be searched, a factor of 4 compared to 1ms integration. Short-cycling the code results in an approximate search time of 81.84 seconds or 1.364 minutes, which is acceptable for most applications. If further reductions in search time are required the receiver must devote additional correlation channels to the search or implement an FFT search algorithm.

Table 10-2, Search times

Signal	Code period (s)	Integration period (s) (A)	Number of half-chip code shifts required (B)	Number of frequency bins (± 5 kHz search) (C)	Search time (s) (AxBxC)
GPS C/A	0.001	0.001	2046	10	20.46
Galileo E1 B	0.004	0.004	8184	40	1309
Galileo E1 B	0.004	0.001	8184	10	81.84

Estimation of the quality of the Giove-A signal has been carried out under ESA contract using the Septentrio GETR receiver. This receiver estimates the separate carrier to noise densities for the Galileo E1 B and C components. The results of monitoring the receiver-estimated carrier to noise against the elevation of the Giove-A satellite were presented in [Falcone *et al* 2006].

On the 26th of June 2006, the SSTL rooftop antenna was used to receive the Giove A E1 B signal with the single-chip receiver. Figure 10-8 shows the elevation and azimuth of the satellite pass on June 26th derived from STK simulation.

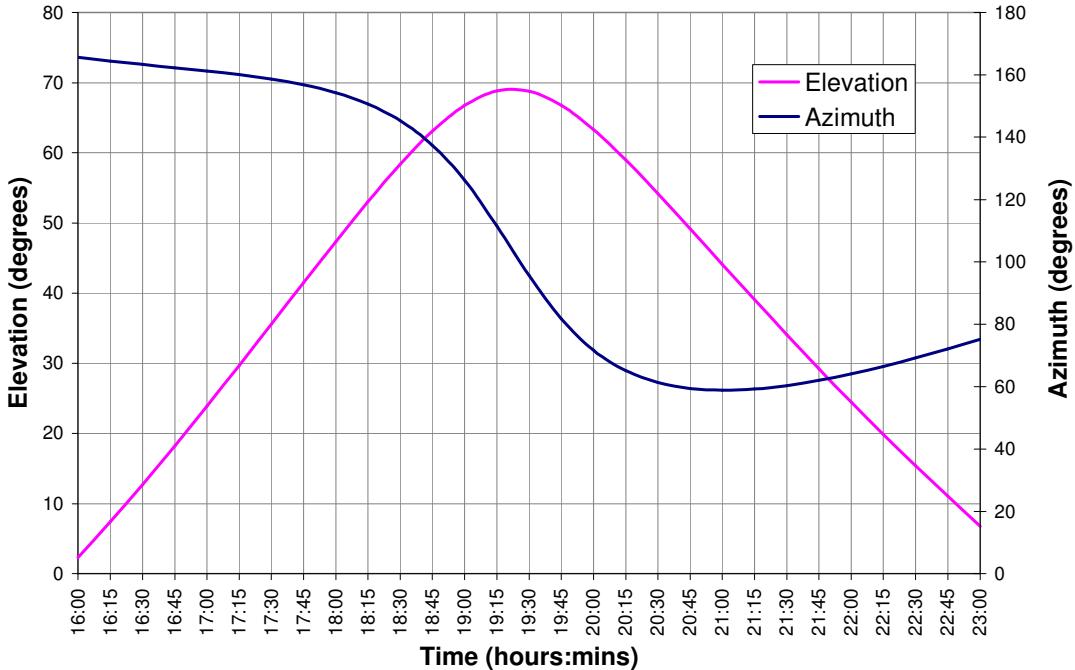


Figure 10-8, Elevation and azimuth of the Giove-A pass on the 26th of June 2006

The signal was successfully acquired at 19:57, the receiver estimated carrier to noise density as 45 dB-Hz. This figure agrees well with the results from the Septentrio GETR receiver. The receiver was configured to track the phase of the incoming carrier, the IQ plot taken from Giove-A tracking is shown in Figure 10-9.

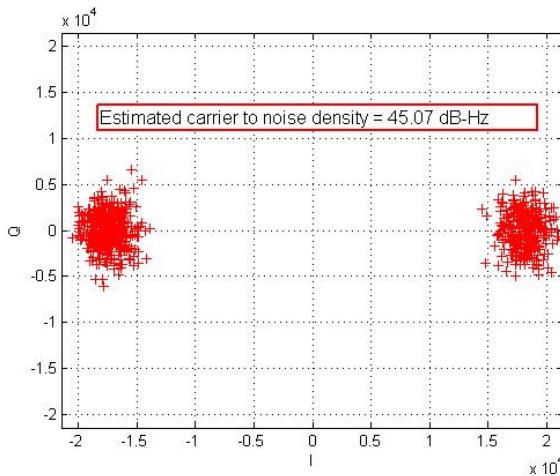


Figure 10-9, I/Q plot taken from Giove-A while in PLL mode

The receiver successfully acquired and tracked the Giove-A BOC(1,1) signal with both DE BOC receiver technique and the BJ algorithm. Both tracking schemes were able to maintain lock on the central peak of the BOC(1,1) correlation.

The single chip receiver provides SSTL with a compact flexible correlator and processor architecture for future missions. The receiver has been demonstrated with of both GPS PSK signals and the Giove-A BOC(1,1) signals. As part of their ongoing investment in this research SSTL are currently adapting the single chip receiver design to track the Giove-A BOC(15,2.5) signal. This demonstration is intended to prove the advantages of the DE BOC receiver for signal with significant distortion (asymmetry).

11 Discussion, conclusions and future work

This chapter provides a synopsis of the contributions made by this research and suggestions on areas of future work in this area. Firstly the contributions are described, which due to the strong practical emphasis of this research contain industrial contributions as well as academic. Following this the suggestions for future work are given, which are also contrived for both industry and academia.

11.1 Academic contributions

The core academic contributions of this research are based around the reception of BOC modulated signals.

In Chapter 4 the advantages and disadvantages of BOC modulated signals are detailed and analyzed. A simply derived yet accurate model for the theoretical timing jitter of BOC systems is given. This allowed derivations for the cosine BOC timing jitter, which have not yet been produced in the literature. A fair comparative analysis of the timing jitter and multipath error performance between BOC and PSK modulations is given. This analysis differs significantly from those given in the literature comparing each signal from the perspective of occupied bandwidth of the signal, rather than a predetermined signal specification. Although there are many political pressures and influences involved in GNSS signal definition, it is important to realize that considering the occupied bandwidth of the signal BOC modulation does not provide significant performance benefits compared with PSK. BOC modulation provides only a small benefit in timing jitter (3 dB maximum), potentially worse multipath performance and can introduce acquisition and tracking problems for the receiver. The fundamental advantage of BOC modulation is to enable spectral separation between signals within an allocated spectral bandwidth. BOC modulation therefore allows efficient use of spectral bandwidth while minimizing interference.

Chapter 5 details the theory of search, acquisition and tracking of PSK and BOC modulated signals. Although the theory for PSK systems is well established, a full comparative analysis of BOC search and tracking techniques has not yet been

produced. This chapter draws on the techniques proposed in the literature for BOC search and tracking and provides a comparative analysis considering both performance measures and the receiver hardware impact. The *sub-carrier cancellation* technique [Heiries *et al* 2004] is found to be the leading BOC search technique, considering search performance, hardware impact and compatibility with BOC tracking techniques. The *bump-jumping* (BJ) algorithm [Fine and Wilson 1999] is found to deliver the maximum timing precision achievable from the BOC modulation and is the most efficient in terms of hardware resources. The *single side band* tracking technique [Martin *et al* 2003] and *smooth multiple gate discriminator* [Bello and Fante 2005] provide the most robust acquisition and tracking performance but are less efficient with hardware resource and have severely degraded timing precision.

The issue of integrity of the BJ algorithm in presence of signal distortion and multipath inference has been analyzed. The results show that both distortion and multipath inference can compromise the performance and reliability of receivers using the BJ algorithm. This approach to solving the BOC ambiguity problem is therefore not suitable for high-integrity applications.

From Chapter 5 we identify two distinct types of BOC tracking scheme. The first type preserves the full timing precision but has false-lock conditions resulting in potentially degraded acquisition performance and unreliable operation. The second type provides robust reliable acquisition and tracking but has a significant reduction in timing sensitivity. In Chapter 6 the *double estimation* (DE) BOC tracking technique is detailed. This tracking technique is an entirely novel contribution to this field of GNSS and as such forms much of the academic contributions of this research. The DE tracking technique is shown to provide the full timing precision of the BOC modulated GNSS signal, while maintaining robust acquisition and tracking. The DE technique is more efficient with hardware resource than the BJ algorithm and in simulation shows a small improvement in multipath performance.

The DE technique has no false-lock conditions within its discriminator function. Therefore, the integrity of a DE BOC receiver is less sensitive to inferring multipath signals and distortions in the correlation function. In addition, slips in receiver

tracking can be automatically corrected, without the need for the *a posteriori* false-lock detection synonymous with the BJ algorithm. This research has identified the effect of asymmetry in the received BOC spectrum and detailed the impact on receiver tracking techniques. The DE technique is shown to be more robust to distortions in the received spectrum when compared to the BJ algorithm.

The DE technique shows many advantages over the existing BOC tracking technique particularly for high-accuracy and high-integrity applications. We hope this will result in the DE technique will become widely accepted and used in future GPS and Galileo receiver designs.

11.2 Practical contributions

This research has made a number of practical contributions and provided demonstrations of signal generators and receivers for the next generation of GNSS signals.

In Chapter 7 the architecture of the signal generator on-board the Giove-A satellite is detailed. This architecture is capable of producing every GNSS signal currently specified for the future systems. The modulation of method of producing the in-phase and quadrature carrier modulation in the DAC reduces the fundamental sampling frequency of the FPGA baseband modulation by a factor of two.

Chapter 8 and 9 describe the contributions of this research to the SSTL receiver design in the form of the *prototype intermediate frequency* PIF receiver and the *single chip* receiver respectively. Both these receiver designs are based on re-programmable FPGAs. The move to FPGA based receiver architecture provides a number of advantages for future GNSS receivers. The most obvious advantages of FPGA based receivers are removing the risk of obsolescence of chipsets, providing flexibility to receiver designs and the option of radiation tolerant architectures. The option of radiation tolerance is of particular importance to space receivers, which commonly operate in extreme environments.

The prototype receiver designs developed during this research provided practical demonstration of the DE BOC tracking technique. Through these demonstrations the techniques required to implement the DE technique in hardware were developed. The demonstrations also act to further our confidence in the theory developed during the research and models developed in order to simulate receiver operation.

11.3 Future Work

This research has resulted in the development of a theoretical novelty, namely the *double-estimating* (DE) BOC receiver. During this research this technique has been demonstrated with rigorous tests in both simulation and with practical receiver designs. The DE BOC tracking technique has been shown to be preferred choice of tracking scheme for BOC modulated GNSS signals with a natural extension to the Galileo AltBOC signal given. One area of further research on the DE BOC receiver is the extension of the DE technique to MBOC signals. This extension is currently being developed by Dr Hodgart with the expectation of filing a second patent application in the near future.

The multipath performance of the DE BOC tracking technique has been assessed in this thesis for standard correlator and narrow correlation techniques. It seems clear that the DE technique can be generalized to other forms of current multipath mitigation techniques, such as double-delta correlators and the early-late slope technique, the performance of such schemes with DE tracking is however yet to be determined.

The strong practical emphasis of this research has resulted in development of both GNSS transmitter and receiver architectures. SSTL are currently further developing the single-chip receiver in order to demonstrate the DE BOC tracking technique on the BOC(15, 2.5) signal from Giove-A. The aim of this work will be to fully characterize the effect of distortion of the transmitter and the receiver front-end filters on the tracking of high-rate BOC signals and hence the advantages of the DE tracking technique.

As detailed in Chapter 8 the FPGA-based correlator and processor architecture are currently under consideration for future SSTL receiver designs. Many space applications require GNSS receiver hardware that is application specific, radiation tolerant and flexible. Therefore, FPGA-based receivers provide the ideal solution for space GNSS receivers.

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A Tiered codes for GPS modernisation and Galileo

Conceived initially for the new GPS L5 signal, tiered codes are to be broadcast by both GPS modernised and Galileo signals. A tiered system overlays the fast changing PRN sequence, which is denoted the primary code, with a secondary code whose bit period is equal to one primary code epoch. The secondary code length is then chosen such that the secondary code period is equal to one symbol period of the navigational data stream (Figure A-1). The aim is to rapidly eliminate the ambiguity that initially exists in locating the PRN code epoch relative to the longer length data transitions.

GNSS receivers can detect 180° phase shifts of the incoming carrier due to a secondary code or navigational data bit flip. The secondary code is known and therefore, its bit pattern can be searched for. Once detected, this sequence can be used to accurately predict the navigational data transitions and true PLL discriminators used in the tracking loops.

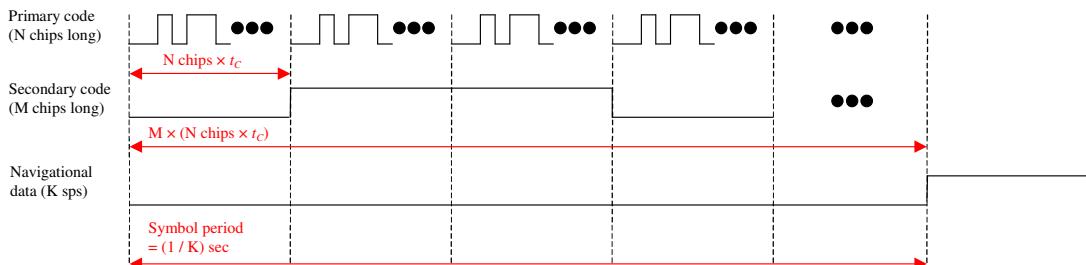


Figure A-1, Tiered code hierarchical structure

The secondary codes are typically less than 100 bits long, in order to maintain an acceptable data rate and therefore can have significant cross correlation magnitudes. To minimise this they are chosen from families of codes that have good synchronisation properties, meaning, the absolute value of their cross-correlation is small. For short secondary codes, up to 13 bits long, the unique Barker or Willard codes can be used. However, for long sequences, up to 100 bits long, Newman / Hofman sequences are used.

In general terms, a tiered code can be written

$$a_T(t) = \sum_n a_p(t - nt_p) \sum_m a_s(t - mt_s) \quad \text{A-1}$$

where $a_p(t)$ is the primary code repeating every $t_p = N \times t_c$ sec, and $a_s(t)$ is the secondary code repeating every $t_s = M \times t_p$ sec, as follows.

$$a_p(t) = \sum_{j=1}^{j=N} a_p p_p(t - jt_c) \quad \text{A-2}$$

$$a_s(t) = \sum_{k=1}^{k=M} a_s p_s(t - kt_p) \quad \text{A-3}$$

$a_p \in (-1,+1)$ is the primary code PRN sequence counting over $1 \leq j \leq N$,
 $a_s \in (-1,+1)$ is the secondary sequence counting over $1 \leq k \leq M$, $p_p(t)$ and
 $p_s(t)$ are ideal rectangular pulses of width t_c and t_p , respectively.

B Mathcad simulations of PSK and BOC

A number of software packages are currently available for theoretical modelling and evaluation of GNSS algorithms. The Mathworks Matlab package is generally favoured for analysis and plotting of sampled data, and was used to generate plots of the data generated by the receiver. However, during this research the Mathsoft Mathcad package was favoured for modelling and comparative analysis of the various GNSS receiver algorithms. This powerful tool provides a see-at-a-glance environment to the designer where all the operations of a representative GNSS receiver can be displayed on a single console screen.

B.1 Received signal representations

Consistent with the theory given in Chapter 5, received PSK signals down-converted to a suitable IF frequency were modelled as follows.

$$u_{PSK}(t) = A \times \cos(\omega_0 t + \phi) \times a(t - \tau) \times d + v(t) \quad \text{B-1}$$

A is the amplitude of the signal, ω_0 is the centre frequency of the IF signal, $a(t)$ is the PRN code sequence and d is the navigational data. τ is the time delay of the code, ϕ is a general phase shift and $v(t)$ is additive white Gaussian noise. In Appendix C, Dr Hodgart provides the necessary theory to set $v(t)$ in order to vary the carrier to noise density of the incoming signal and loop parameters of the simulation.

A single multipath PSK interferer was modelled using a addition of the received direct and multipath signal, which can be written as follows.

$$\begin{aligned} u_{PSK}(t) = & A \times \cos(\omega_C t + \phi) \times a(t - \tau) \times d \\ & + \alpha \times [A \times \cos(\omega_C t + \phi) \times a(t - \tau - \delta) \times d] \end{aligned} \quad \text{B-2}$$

α is the coefficient of reflection, which in all analysis presented here is assumed to be $\alpha = 0.5$. δ is time delay of the multipath signal with respect to the direct signal.

Similarly a single received BOC signal was modelled as follows.

$$u_{BOC}(t) = A \times \cos(\omega_0 t + \phi) \times s(t - \tau) \times a(t - \tau) \times d + v(t) \quad \text{B-3}$$

$s(t)$ is the BOC sub-carrier waveform. The multipath BOC model is then

$$\begin{aligned} u_{BOC}(t) &= A \times \cos(\omega_c t + \phi) \times s(t - \tau) \times a(t - \tau) \times d \\ &+ \alpha \times [A \times \cos(\omega_c t + \phi) \times s(t - \tau - \delta) \times a(t - \tau - \delta) \times d] \end{aligned} \quad \text{B-4}$$

Simulation of multiple interfering signals was also modelled, again simply using the linear addition of signals.

B.2 Example simulation

In order to demonstrate the format of the simulations and the flow in Mathcad we use the PSK model. The extensions to BOC and the various tracking schemes given in Chapters 5 and 6 are then elementary as they follow the same simulation flow. In the following PSK example a 15 chip PRN code spreading sequence is used to reduce the simulation time. Full-length code simulations were carried out for all techniques presented in this thesis. However, using a shorter codes allows rapid initial evaluation of receiver algorithms provided noise levels and loop bandwidths are adjusted accordingly.

The sampling rate of the simulations was generally set to be much greater than required in order to remove any sampling dependant effects. However, care was always taken to insure the sampling frequency is not a multiple of the code rate, which is clearly detrimental to receiver operation.

Time in the simulation in engineering units of quarter chips. Notice the familiar notation of the integration results, w_{II} , w_{IQ} , w_{QI} (same as chapter 5). The carrier PLL is second order and the code DLL is first order.

PSK SIMULATION

$$\begin{aligned}
 N := 4 & \quad T := 15 & \delta \equiv 0.07161 & \quad \Delta := \frac{1}{4} \\
 k := 20 & \quad T_S := \frac{1}{N \cdot 1.023 \cdot 10^6}
 \end{aligned}$$

$\text{prn} := \begin{cases} r_3 \leftarrow 1 \\ \text{for } i \in 0..14 \\ \quad x \leftarrow r_0 \oplus r_1 \\ \quad \text{for } j \in 1..3 \\ \quad \quad r_{j-1} \leftarrow r_j \\ \quad r_3 \leftarrow x \\ \quad a_i \leftarrow x \\ \quad a \leftarrow 2 \cdot a - 1 \end{cases}$

$\text{code}_I(t) := \begin{cases} \tau \leftarrow t \\ \text{while } \tau \geq T \cdot N \\ \quad \tau \leftarrow \tau - T \cdot N \\ \text{while } \tau < 0 \\ \quad \tau \leftarrow \tau + T \cdot N \\ \quad j \leftarrow \text{floor}\left(\frac{\tau}{N}\right) \\ \quad \text{prn}_j \end{cases}$

$\text{code}_Q(t) := \text{code}_I\left(t + \frac{\Delta \cdot N}{2}\right) - \text{code}_I\left(t - \frac{\Delta \cdot N}{2}\right)$

$$\begin{aligned}
 CN0 &:= 6 + k \cdot 0.1 \\
 C_{N0} &:= 10^{CN0} & \phi_C &:= 0 \\
 \sigma_N &:= \frac{1}{\sqrt{2 \cdot \delta \cdot T_S \cdot C_{N0}}} & \sigma_N &= 0.535
 \end{aligned}$$

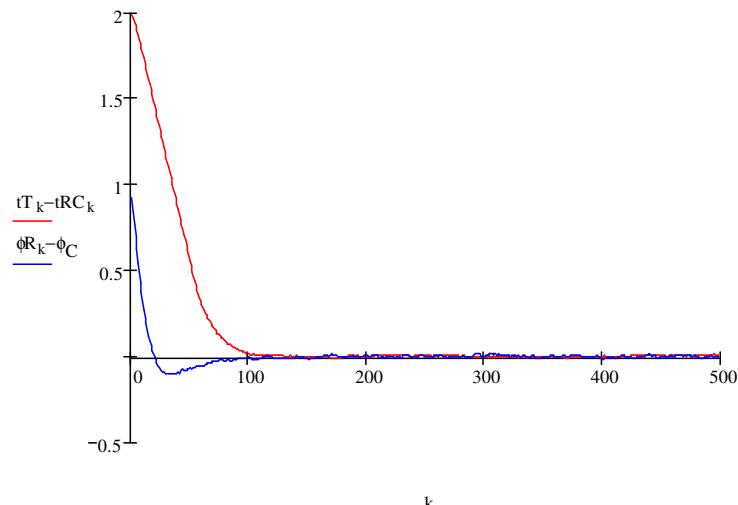
$$\Lambda(t_T, t_{RC}, \phi_R) := \begin{cases} w_{II} \leftarrow 0 \\ w_{IQ} \leftarrow 0 \\ w_{QI} \leftarrow 0 \\ \text{while } t_{RC} \leq 15 \cdot N \\ \quad u_I \leftarrow \cos(\phi_C - \phi_R) \cdot (\text{code}_I(t_T)) + \text{rnorm}(1, 0, \sigma_N) \\ \quad u_Q \leftarrow \sin(\phi_C - \phi_R) \cdot (\text{code}_I(t_T)) + \text{rnorm}(1, 0, \sigma_N) \\ \quad v_I \leftarrow \text{code}_I(t_{RC}) \\ \quad v_Q \leftarrow \text{code}_Q(t_{RC}) \\ \quad w_{II} \leftarrow w_{II} + u_I \cdot v_I \\ \quad w_{IQ} \leftarrow w_{IQ} + u_I \cdot v_Q \\ \quad w_{QI} \leftarrow w_{QI} + u_Q \cdot v_I \\ \quad t_T \leftarrow t_T + \delta \\ \quad t_{RC} \leftarrow t_{RC} + \delta \\ \quad w_{II} \leftarrow w_{II} \frac{\delta}{N \cdot T} \\ \quad w_{IQ} \leftarrow w_{IQ} \frac{\delta}{N \cdot T} \\ \quad w_{QI} \leftarrow w_{QI} \frac{\delta}{N \cdot T} \\ \quad t_T \leftarrow t_T - N \cdot T \\ \quad t_{RC} \leftarrow t_{RC} - N \cdot T \\ \quad (w_{II} \ w_{IQ} \ w_{QI} \ t_T \ t_{RC} \ \phi_R)^T \end{cases}$$

$$k_0 C \equiv 0.114 \quad k_0 \phi \equiv 0.2 \quad k_1 \phi \equiv 0.005$$

$$\Phi(S_{wIQ}, S_{wQI}, t_T, t_{RC}, \phi_R) := \begin{cases} X \leftarrow \Lambda(t_T, t_{RC}, \phi_R) \\ d \leftarrow \text{sign}(X_0) \\ w_{IQ} \leftarrow X_1 \cdot d \\ w_{QI} \leftarrow X_2 \cdot d \\ S_{wIQ} \leftarrow S_{wIQ} + w_{IQ} \\ S_{wQI} \leftarrow S_{wQI} + w_{QI} \\ t_T \leftarrow X_3 \\ t_{RC} \leftarrow X_4 + k_0 C \cdot w_{IQ} \\ \phi_R \leftarrow X_5 + k_0 \phi \cdot w_{QI} + k_1 \phi \cdot S_{wQI} \\ (S_{wIQ} \ S_{wQI} \ t_T \ t_{RC} \ \phi_R)^T \end{cases}$$

$$\begin{aligned} k &:= 1..1500 & S_{wIQ_0} &:= 0 & t_{T_0} &:= 2 & t_{RC_0} &:= 0 \\ && S_{wQI_0} &:= 0 && && \phi_{R0} &:= 1 \end{aligned}$$

$$\begin{pmatrix} S_{wIQ_k} \\ S_{wQI_k} \\ t_{T_k} \\ t_{RC_k} \\ \phi_{R_k} \end{pmatrix} := \Phi(S_{wIQ_{k-1}}, S_{wQI_{k-1}}, t_{T_{k-1}}, t_{RC_{k-1}}, \phi_{R_{k-1}})$$



C Analogue and digital DLL formulas

This appendix was kindly supplied by Dr Hodgart and provides the formulas used to simulate additive noise to GNSS signals.

C.1 Introduction

Necessary formulas for the triple loop PLL + SLL + DLL are presented derived by inference from real time pulse detection

Suggested nomenclature

PLL phase lock loop for carrier (may be replaced by FLL)

SLL subcarrier lock loop

DLL delay lock loop – for tracking the code

The loop creates two time estimates - one from the DLL effectively ignoring the subcarrier modulation,

We simplify first by just looking at the low pass waveforms –carrier phase analysis is ignored.

Instead of a code sequence $a(t)$ we have a BOC sequence

$$b(t - \tau) = a(t - \tau) \times s(t - \tau) \quad \text{C-1}$$

where $s(t)$ is a squared up sine wave (or an actual sinewave in LOC)

Because of necessity to describe noise at various points we have had to change symbols to describe input.

Our actual signal input is the in-phase channel only here

$$y_I(t) = Ab(t - \tau) + v_I(t) \quad \text{C-2}$$

which the SLL and the DLL then test with *independent* delay estimates

$$\mathbf{z}_I(\hat{\tau}^*, \hat{\tau}) = \frac{1}{T_G} \int_0^{T_G} y_I(t) \times \begin{pmatrix} s(t - \hat{\tau}^*) \\ \tilde{s}(t - \hat{\tau}^*) \end{pmatrix} \times \begin{pmatrix} a(t - \hat{\tau}) \\ \tilde{a}(t - \hat{\tau}) \end{pmatrix}^\top dt \quad \text{C-3}$$

where

$$\tilde{a}(t) = a\left(t + \frac{T_D}{2}\right) - a\left(t - \frac{T_D}{2}\right) \quad \text{C-4}$$

The correlation

$$\frac{1}{T_G} \int_0^{T_G} a(t-\tau) a(t-\hat{\tau}) dt = \Lambda(\tau - \hat{\tau}) \quad \text{C-5}$$

where Λ has usual width $\pm T_C$ and unit height Also form

the correlation

$$\frac{1}{T_G} \int_0^{T_G} a(t-\tau) \tilde{a}(t-\hat{\tau}) dt = \Lambda_V(\tau - \hat{\tau}) \quad \text{C-6}$$

and gives a discriminator characteristic

With conventional gate width $T_D = T_C$ then discriminator slope = $2/T_C$

Looking at actual outputs

$$z_{IIQ} = \frac{A}{T_G} \int_0^{T_G} a(t-\tau) \tilde{a}(t-\hat{\tau}) dt + \frac{1}{T_G} \int_0^{T_G} u(t) \tilde{a}(t-\hat{\tau}) dt = A \Lambda_V(\tau - \hat{\tau}) + w_{IIQ} \quad \text{C-7}$$

where Λ_V has slope $2/T_C$ after setting gate width $T_D = T_C$

$$\begin{aligned} z_I(\hat{\tau}^*, \hat{\tau}) &= \frac{1}{T_G} \int_0^{T_G} a(t-\tau) \times s(t-\tau) \times \begin{pmatrix} s(t-\hat{\tau}^*) \\ \tilde{s}(t-\hat{\tau}^*) \end{pmatrix} \times \begin{pmatrix} a(t-\hat{\tau}) \\ \tilde{a}(t-\hat{\tau}) \end{pmatrix}' dt \\ &+ \frac{1}{T_G} \int_0^{T_G} u(t) \times \begin{pmatrix} s(t-\hat{\tau}^*) \\ \tilde{s}(t-\hat{\tau}^*) \end{pmatrix} \times \begin{pmatrix} a(t-\hat{\tau}) \\ \tilde{a}(t-\hat{\tau}) \end{pmatrix}' dt \end{aligned} \quad \text{C-8}$$

Knowing that the loops are able to proceed independently we can in theory set

$\hat{\tau}^* = \tau$ and consider variation of above as only between $\hat{\tau}$ and τ

$$z_{III}(\hat{\tau}^* = \tau, \hat{\tau}) = \frac{A}{T_G} \int_0^{T_G} a(t-\tau) \times a(t-\hat{\tau}) dt + \frac{1}{T_G} \int_0^{T_G} u(t) \times a(t-\hat{\tau}) dt \quad \text{C-9}$$

or

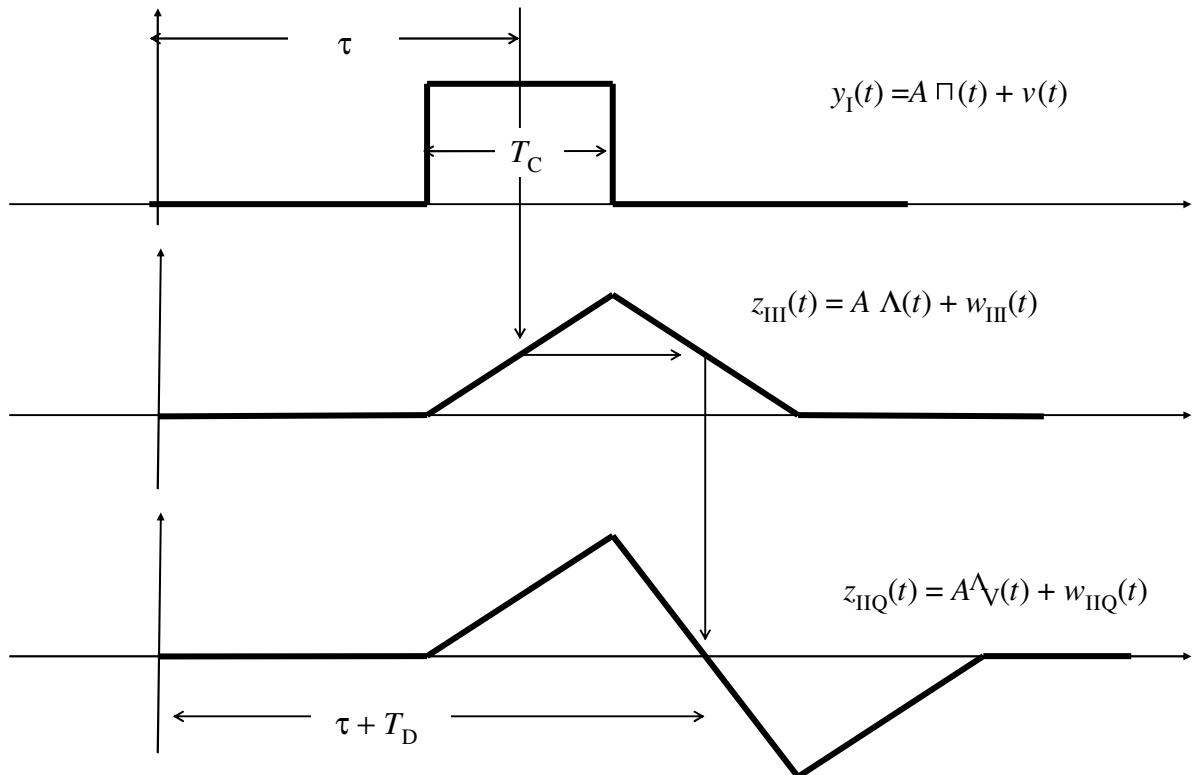
$$z_{III}(\hat{\tau}^* = \tau, \hat{\tau}) = A \Lambda(t) + w_{III} \quad \text{C-10}$$

$$z_{IIQ}(\hat{\tau}^* = \tau, \hat{\tau}) = \frac{A}{T_G} \int_0^{T_G} a(t-\tau) \times \tilde{a}(t-\hat{\tau}) dt + \frac{1}{T_G} \int_0^{T_G} u(t) \times \tilde{a}(t-\hat{\tau}) dt \quad \text{C-11}$$

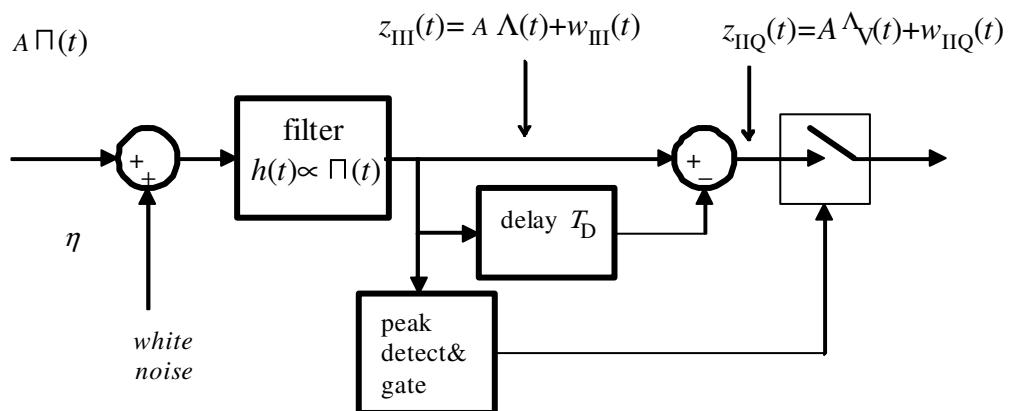
Or

$$z_{\text{IIQ}}(\hat{\tau}^* = \tau, \hat{\tau}) = A \Lambda_V(t) + w_{\text{IIQ}} \quad \text{C-12}$$

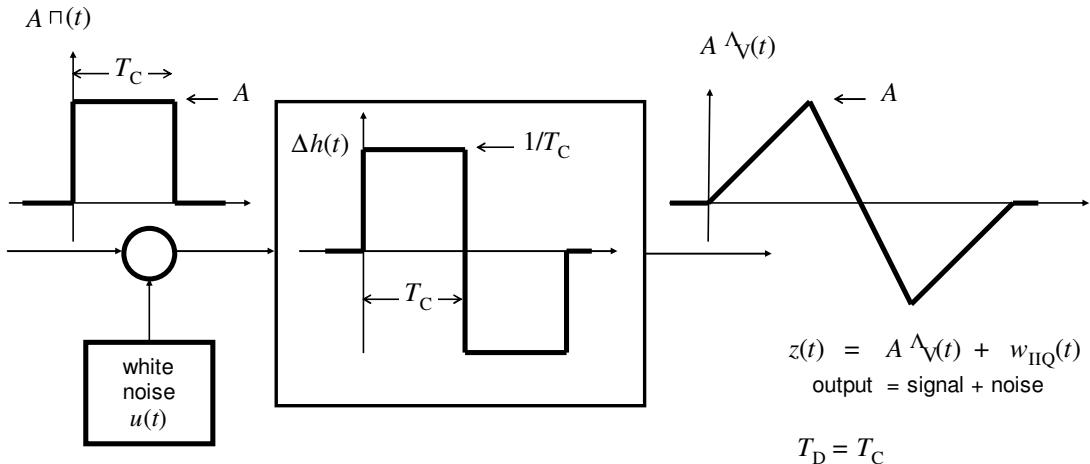
which allows the evaluation of error exactly as if this was PSK transmission.



The system representation may be shown as



C.2 Linear system equivalent



We specifically identify a rectangular pulse of amplitude A and width T_C in presence of white noise of one-sided density η . We also set $T_D = T_C$

This filter representation of the processing system allows an immediate evaluation of timing error. A noise sample $w = w_{IIQ}$ converts to a timing error ϵ by the elementary relation of reflection though the slope dz/dt on the zero crossing in z .

$$\epsilon = \frac{w}{\frac{dz}{dt}} \quad \text{C-13}$$

and the mean square timing jitter

$$\Sigma^2 = \langle \epsilon^2 \rangle = \frac{\langle w^2 \rangle}{\left(\frac{dz}{dt} \right)^2} \quad \text{C-14}$$

The basic system theory which is needed is simply to know that the mean square noise out of the filter

$$\begin{aligned} \langle w^2 \rangle &= \frac{\eta}{2} \times \int \Delta h(t)^2 dt \\ &= \frac{\eta}{2} \times \int (h(t) - h(t - T_C))^2 dt \\ &= \frac{\eta}{2} \times 2 \times \left(\frac{1}{T_C} \right)^2 T_C \end{aligned} \quad \text{C-15}$$

Then

$$\langle w^2 \rangle = \frac{\eta}{T_C} \quad \text{C-16}$$

and since $dz/dt = 2A/T_C$ we get

$$\Sigma^2 = \frac{T_C \eta}{4A^2} \quad \text{C-17}$$

The custom exists in the literature of normalising the timing jitter to a chip length.
 (This practice can lead into difficulties when it comes to comparing PSK with BOC).
 However to ensure consistency with this approach let us now define and now express
 a timing jitter normalised to the chip length

$$\sigma^2 = \frac{\Sigma^2}{T_C^2} = \frac{1}{4T_C} \times \frac{1}{A^2/\eta} \quad \text{C-18}$$

A reduced delay time $T_D < T_C$ may be able to achieve a reduced timing jitter . Then

$$\sigma^2 = \frac{\Sigma^2}{T_C^2} = \frac{1}{4T_C} \times \frac{\Delta}{A^2/\eta} \quad \text{C-19}$$

where by usual convention the normalised delay

$$\Delta = \frac{T_D}{T_C} \quad \text{C-20}$$

which may be less than unity (but not greater).

C.3 Signal averaging

Let there be signal averaging over K pulses . Then the timing error reduces to

$$\sigma^2 = \frac{1}{4KT_C} \times \frac{\Delta}{A^2/\eta} \quad \text{C-21}$$

Now the product KT_C = the total transmission time – the total period over which the notional pulse transmitter is equivalent to an averaging or processing time = T

$$\sigma^2 = \frac{1}{4T} \times \frac{\Delta}{A^2/\eta} \quad \text{C-22}$$

C.4 Digital loop analysis

A practical system employs sampling at an interval we shall call here δ .

In simulation and reality let there be samples $y_l[l]$ at sample intervals δ . Code correlation time T_G

Number of samples per code

$$n_G = \frac{T}{\delta} \quad \text{C-23}$$

Sample number n_G is not an integer

Add noise samples $v[l] = v_I[l] =$ with an rms value $\sigma_v^2 = \frac{\eta}{2\delta}$

We synthesise therefore

$$y_I[l] = Ab(t_l - \tau) + v_I[l] \quad \text{C-24}$$

We need also to identify a code integration time T_G (G for GOLD) this being span of minimum time in which to run a correlation .

We shall ignore carrier recovery – which we can.

Ignoring presence and interaction of SLL is allowed in the limiting case with small deviations

$$z_{III} = \frac{1}{n_G} \sum_{l=1}^{n_G} y_I[l] a(t_l - \hat{\tau}) \quad \text{C-25}$$

which approximates the correlation

$$z_{III} = \frac{1}{T_G} \int_0^{T_G} y_I(t) a(t - \hat{\tau}) dt \quad \text{C-26}$$

As shown above

$$z_{III} = A \Lambda(\tau - \hat{\tau}) + v \quad \text{C-27}$$

$$z_{IIQ} = \frac{1}{n_G} \sum_{l=1}^{n_G} x_l \tilde{a}(t_l - \hat{\tau}) \quad \text{C-28}$$

which approximates the correlation

$$z_{IIQ} = \frac{1}{T_G} \int_0^{T_G} x(t) \tilde{a}(t - \hat{\tau}) dt \quad \text{C-29}$$

C.5 Loop operation

Simplify noise notation $w_k = w_{\text{I}Q}[k]$

On completion of one correlation (in time T_G) the loop estimate of time delay is updated

$$\hat{\tau}_{k+1} = \hat{\tau}_k + (A \Lambda_V (\tau_k - \hat{\tau}_k) + w_k) \times k_{0C} \quad \text{C-30}$$

or in linear region

$$\hat{\tau}_{k+1} = \hat{\tau}_k + \left(\frac{2A}{T_C} \times (\tau_k - \hat{\tau}_k) + w_k \right) k_{0C} \quad \text{C-31}$$

Let actual time delay $\tau_k = 0$ then we are looking at an error

$$\epsilon_{k+1} = (1 - \rho_C) \epsilon_k + k_{0C} w_k \quad \text{C-32}$$

after defining

$$\rho_C = \frac{2A}{T_C} \times k_{0C} \quad \text{C-33}$$

this is a classic 1st order IIR filter

The mean square absolute timing error

$$\Sigma_{\text{DLL}}^2 = \langle \epsilon^2 \rangle = \frac{\rho_C}{2 - \rho_C} \times \left(\frac{T_C}{2A} \right)^2 \times \langle w^2 \rangle \quad \text{C-34}$$

or after normalising and identifying

$$\sigma_{\text{DLL}}^2 = \langle \epsilon^2 \rangle = \frac{\rho_C}{2 - \rho_C} \times \left(\frac{1}{2A} \right)^2 \times \frac{\eta}{T_G} \quad \text{C-35}$$

comparison of the various formulas then identifies an overall averaging time

$$\frac{2 - \rho_C}{\rho_C} T_G = \frac{2 - 2Ak_{0C}/T_C}{2Ak_{0C}/T_C} T_G = \left(\frac{T_C}{Ak_{0C}} - 1 \right) T_G \quad \text{C-36}$$

Substituting in (C-35) after inverting and with $\Delta = 1$ then

$$\frac{1}{\sigma_{\text{DLL}}^2} = 4 \times \frac{A^2}{\eta} \times T_G \times \left(\frac{T_C}{Ak_{0C}} - 1 \right) \quad \text{C-37}$$

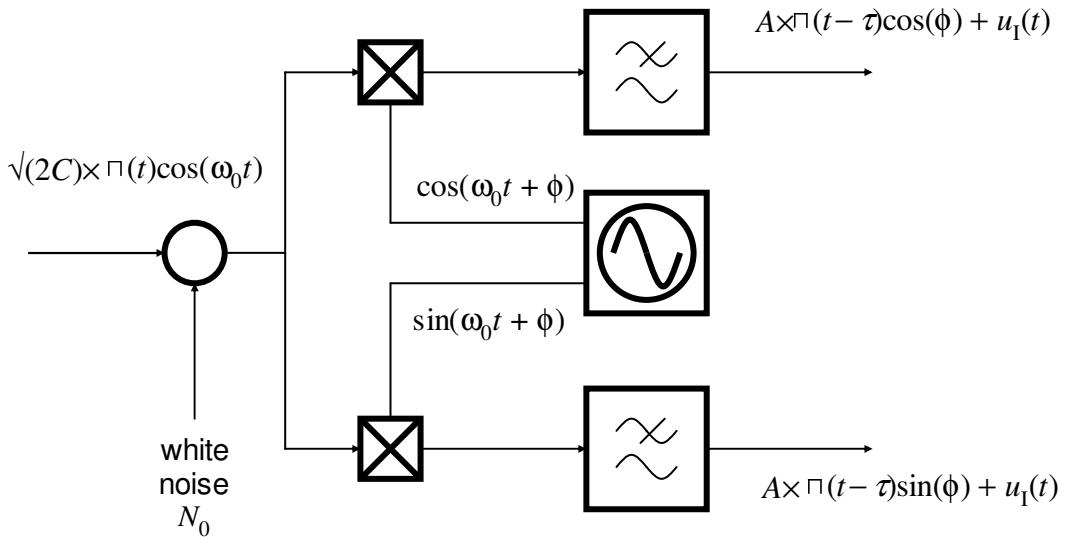
Then standard theory finds for the *input* noise

$$\sigma_v^2 = \frac{\eta}{2\delta} \quad \text{C-38}$$

Therefore given in loop simulation A , σ_v , δ , T_C , T_G , k_{0C} then

$$\frac{1}{\sigma_{\text{DLL}}^2} = 2 \times \frac{A^2}{\sigma_v^2} \times \frac{T_G}{\delta} \times \left(\frac{T_C}{Ak_{0C}} - 1 \right) \quad \text{C-39}$$

C.6 Conversion from RF system



In down conversion from an r.f channel there are by convention in phase and quadrature channels . We may generalise to

$$x_I(t) = A \cdot s(t - \tau) \cos(\phi) + u_I(t) \quad \text{C-40}$$

$$x_Q(t) = A \cdot s(t - \tau) \sin(\phi) + u_Q(t)$$

C.7 Informal comparison with coherent DLL systems

In a coherent system we can assume $\phi = 0$

Our result is directly convertible into RF equivalent of input carrier power $C \propto A^2$ and noise density $N_0 \propto \eta$

$$\sigma_{\text{DLL}}^2 = \frac{1}{4T} \times \frac{\Delta}{C/N_0} \quad \text{C-41}$$

We can match the above to well-established analyses.

It is in the nature of CDMA using the Gold code to be able to achieve the same effect as sending one pulse by a continuous code. So in L1 the effect of the transmission of 1023 chips organised in a code over 1 msec is to achieve $K = 1023$ in just $T = 1$ msec. This is the great advantage of using a code. T can therefore be interpreted as the total elapsed time over which that the signal is available
But a practical DLL system the averaging time is extended by employing a loop of (one-sided) bandwidth B_L which has an averaging time $T = 1/2B_L$. Therefore

$$\sigma_{\text{DLL}}^2 = \frac{B_L \Delta}{2 C/N_0} \quad \text{C-42}$$

In our PSK systems presently set conservatively $\Delta = 1$ - however there is more to it than that.

In principle one *can* reduce D to achieve greater accuracy – but always assuming that the bandwidth W in the system is capable of supporting the necessary sharpness of pulses (both transmitter and receiver).

On a code demand basis – the same T_C comparing PSK and BOC we can accept that the BOC system does demand an increased bandwidth and system bandwidth allocation.

A fair comparison against PSK then allows that PSK system to improve its accuracy by reducing D

C.8 Comparison with digital loop

Then standard theory finds for the *input* noise

$$\sigma_v^2 = \frac{\eta}{2\delta} \quad \text{C-43}$$

Therefore to match a given C/N_0 in the analogue r.f world choose A and σ_v such that

$$\frac{A}{\sigma_v} = \sqrt{2 \times \delta \times \left(\frac{C}{N_0} \right)} \quad \text{C-44}$$

C.9 Time estimate error from the SLL

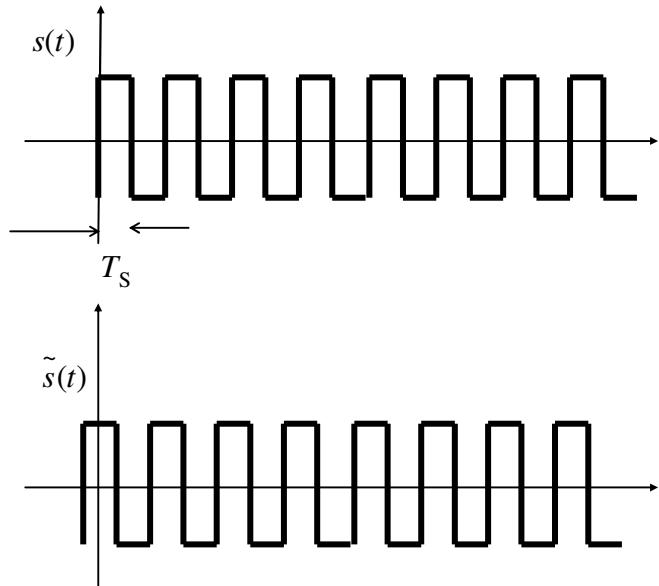
Equally we can in theory set $\hat{\tau} = \tau$ and consider variation of above as only between $\hat{\tau}^*$ and τ within the SLL

$$z_{\text{IQI}}(\hat{\tau}^*, \hat{\tau} = \tau) = \frac{A}{T_G} \int_0^{T_G} s(t - \tau) \times \tilde{s}(t - \hat{\tau}) dt + \frac{1}{T_G} \int_0^{T_G} v_I(t) \times \tilde{s}(t - \hat{\tau}) dt \quad \text{C-45}$$

or

$$\begin{aligned} y_{\text{IQI}}(\hat{\tau}, \hat{\tau}^* = \tau) &= A \times M(t) + \frac{1}{T_G} \int_0^{T_G} v_I(t) \times \tilde{s}(t - \hat{\tau}) dt \\ y_{\text{IQI}}(\hat{\tau}, \hat{\tau}^* = \tau) &= A \times M(t) + w_{\text{IQI}} \end{aligned} \quad \text{C-46}$$

which allows evaluation of error exactly as if this was a simple correlation from DLL. This is easily evaluated directly from the correlation equations where $s(t)$ is the squarewave function as shown with the noiseless output below



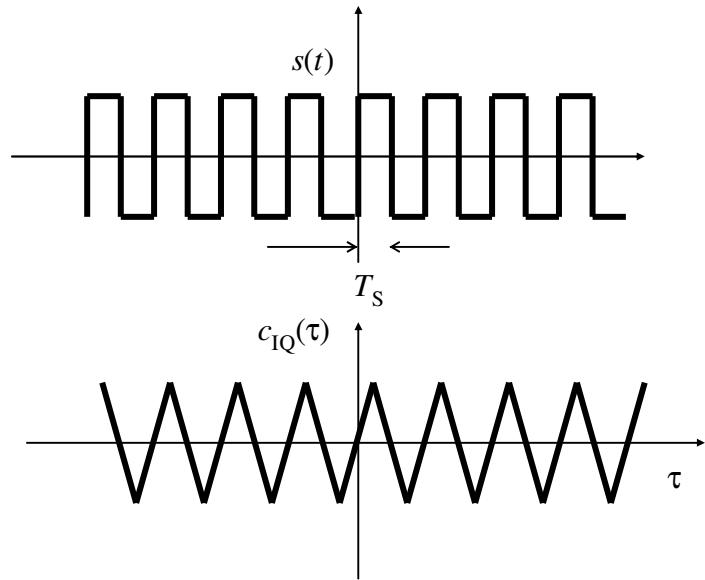


Figure C-1, Slope of output correlation

$$\frac{dc}{d\tau} = \frac{2A}{T_S} \quad \text{C-47}$$

and noise output

$$\langle w_{IQI}^2 \rangle = \frac{\eta}{2T} \quad \text{C-48}$$

Therefore mean square timing jitter -normalised to sub-chip T_S

$$\sigma_{SLL}^2 = \frac{\Sigma^2}{T_S^2} = \frac{1}{8T \left(A^2 / \eta \right)} \quad \text{C-49}$$

or in rf equivalent within a loop bandwidth B_L

$$\sigma_{SLL}^2 = \frac{B_L}{4C/N_0} \quad \text{C-50}$$

C.10 Loop operation

On completion of one correlation (in time T_G) the loop estimate of time delay is updated.

Simplify noise notation $w_k = w_{IQI}[k]$

$$\hat{\tau}_{k+1}^* = \hat{\tau}_k^* + (\mathcal{M}(\tau_k - \hat{\tau}_k^*) + w_k) \times k_{0S} \quad \text{C-51}$$

or in linear region

$$\hat{\tau}_{k+1}^* = \hat{\tau}_k^* + \left(\frac{2A}{T_S} \times (\tau_k - \hat{\tau}_k^*) + w_k \right) k_{0S} \quad \text{C-52}$$

Let actual time delay $\tau_k = 0$ then we are looking at an error

$$\varepsilon_{k+1} = (1 - \rho) \varepsilon_k + k_{0S} w_k \quad \text{C-53}$$

after defining

$$\rho_S = \frac{2A}{T_S} \times k_{0S} \quad \text{C-54}$$

this is again a classic 1st order IIR filter

The mean square absolute timing error

$$\Sigma_{SLL}^2 = \langle \varepsilon^2 \rangle = \frac{\rho_S}{2 - \rho_S} \times \left(\frac{T_S}{2A} \right)^2 \times \langle w_{IQI}^2 \rangle \quad \text{C-55}$$

or after normalising and identifying

$$\sigma_{SLL}^2 = \langle \varepsilon^2 \rangle = \frac{\rho_S}{2 - \rho_S} \times \left(\frac{1}{2A} \right)^2 \times \frac{\eta}{2T_G} \quad \text{C-56}$$

comparison of the various formulas then identifies an overall averaging time

$$\frac{2 - \rho_S}{\rho_S} T_G = \frac{2 - 2Ak_{0S}}{2Ak_{0S}} T_S = \left(\frac{T_S}{Ak_{0S}} - 1 \right) T_G \quad \text{C-57}$$

Substituting in (C-56) after inverting

$$\frac{1}{\sigma_{SLL}^2} = 8 \times \frac{A^2}{\eta} \times T_G \times \left(\frac{T_S}{Ak_{0S}} - 1 \right) \quad \text{C-58}$$

Then standard theory finds for *input* noise

$$\sigma_v^2 = \frac{\eta}{2\delta} \quad \text{C-59}$$

Therefore given in loop simulation A , σ_v , δ , T_C , T_G , k_{0S} then

$$\frac{1}{\sigma_{SLL}^2} = 4 \times \frac{A^2}{\sigma_v^2} \times \frac{T_G}{\delta} \times \left(\frac{T_S}{Ak_{0S}} - 1 \right) \quad \text{C-60}$$

C.11 Symbol list for Appendix C

$\tilde{s}(t)$	orthogonal subcarrier
A	amplitude
$a(t)$	Gold code sequence $a = +1$ or -1
$\tilde{a}(t)$	quasi orthogonal function obtained from subtracting so-called late gate from early gate
$b(t)$	BOC or LOC modulation product of $a(t)$ and sub-carrier
C	carrier power
d	a data value $\in (-1,+1)$
e	various kinds of signal processing error
k_{oc}	DLL loop gain
k_{os}	SLL loop gain
m	sub-carrier frequency (Hz)
$r(t)$	LO reference
$s(t)$	sub-carrier sequence $s = +1$ or -1
$Ssin(\Omega t)$	'squared up' sub-carrier $s(t)$
T_C	chip time
T_G	correlation time
T_s	sub chip time
$x(t)$	incoming signal on carrier
$y(t)$	signal expressed as equivalent I and Q
z	a correlation output obtained on completion of correlation time
Λ	idealised symbol to represent triangular output correlation shape
Λ_V	invented symbol representing the quasi-differentiation of Λ
Ω	sub-carrier frequency in rads/sec
α_{lk}	noise like cross correlation of competing Gold codes with orthogonal reference
α_{lk}'	noise like cross correlation of competing Gold codes with reference
δ	sampling interval
ϵ	timing error on a slope discrimination
σ_v	Standard deviation of additive white Gaussian noise to the received signal
ϕ	a phase shift on that carrier By implication $\phi = \phi(t)$ is time varying – but we do not show this dependence for clarity. The rate of change $d\phi/dt = \omega$ is a Doppler shift.
ϕ'	earlier or later phase shift in adjacent block
$\hat{\phi}$	test or trial phase shift
$\hat{\phi}'$	earlier or later phase shift estimate in adjacent block
τ	the delay time to be best estimated which is the navigational basic information
$\hat{\tau}$	test or trial delay
$\hat{\tau}^*$	trial or test time delay on sub-carrier
ω	Doppler shift on carrier
$\hat{\omega}$	test or trial delay Doppler shift
ω_0	the nominal carrier frequency (actually down converted)

D Setting loop parameters in practice

It is essential that GNSS receiver designers take into account the amplitude dependence of the different discriminators used in GNSS tracking loops. For this reason a list of all common discriminator for PLLs, FLLs, SLLs and DLLs is given in Chapter 5 and 6 of this thesis. Looking at the SSTL SGR DLL loop can show a good example of the importance of these considerations. Table 5-3 shows the different DLL loop discriminators for PSK signals.

Table D-1, DLL discriminators for PSK signals

Discriminator	Error signal	Dependency
Coherent		
Dot product	$e_\tau = w_{IQ} \times w_{II}$ $\approx A^2 \times \cos^2(\phi - \hat{\phi}) \times V^\Delta (\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A^2
Decision-directed	$e_\tau = w_{IQ} \times \text{sgn}(w_{II})$ $\approx A \times \cos(\phi - \hat{\phi}) \times V^\Delta (\hat{\tau} - \tau)$	Slope proportional to A
Incoherent		
Dot product	$e_\tau = w_{IQ} \times w_{II} + w_{QI} \times w_{QQ}$ $\approx A^2 \times V^\Delta (\hat{\tau} - \tau) \times \Lambda(\hat{\tau} - \tau)$	Slope proportional to A^2
Decision-directed	$e_\tau = w_{IQ} \times \text{sgn}(w_{II}) + w_{QQ} \times \text{sgn}(w_{QI})$ $\approx A \times (\left \cos(\phi - \hat{\phi})\right + \left \sin(\phi - \hat{\phi})\right) \times V^\Delta (\hat{\tau} - \tau)$	Slope proportional to A
Power	$e_\tau = w_{IE}^2 + w_{QE}^2 - w_{IL}^2 - w_{QL}^2$ $\approx A^2 \times V^{\Delta^2} (\hat{\tau} - \tau)$	Slope proportional to A^2

The SGR DLL loop uses a dot-product discriminator, which imposes a very small amount of loading on the receiver's microprocessor but has an A^2 dependence. The loop is first order with Doppler aiding from the carrier-tracking loop, which can be written as (repeat from Chapter 8)

$$\hat{\tau} = \hat{\tau} + k_\phi \times f_\phi + k_\tau \times e_\tau \quad \mathbf{D-1}$$

where

$$k_\tau = \frac{K_{CD} K_{DCO} \Delta}{T_1} \quad \mathbf{D-2}$$

T_1 is the time constant of the first order loop, K_{CD} is the gain of the code discriminator and K_{DCO} is the code DCO gain. The natural loop frequency ω_n and loop bandwidth B_L can then be calculated as follows.

$$\omega_n = \frac{K_{FD} \times K_{DCO}}{T_1}, \quad B_L = \frac{\omega_n}{4} \quad \text{D-3}$$

The value of K_{DCO} is a constant mapping between the estimated delay error and the required DCO frequency increment. However, setting K_{CD} is more complicated design issue. The normalised dot-product discriminator is shown in Figure 5-11, it delivers a nearly true error between $\pm 1/4$ chip of code error. However, this is a normalised plot. In practice this error characteristic has an A^2 dependence and therefore expands and contracts with the power of the incoming signal.

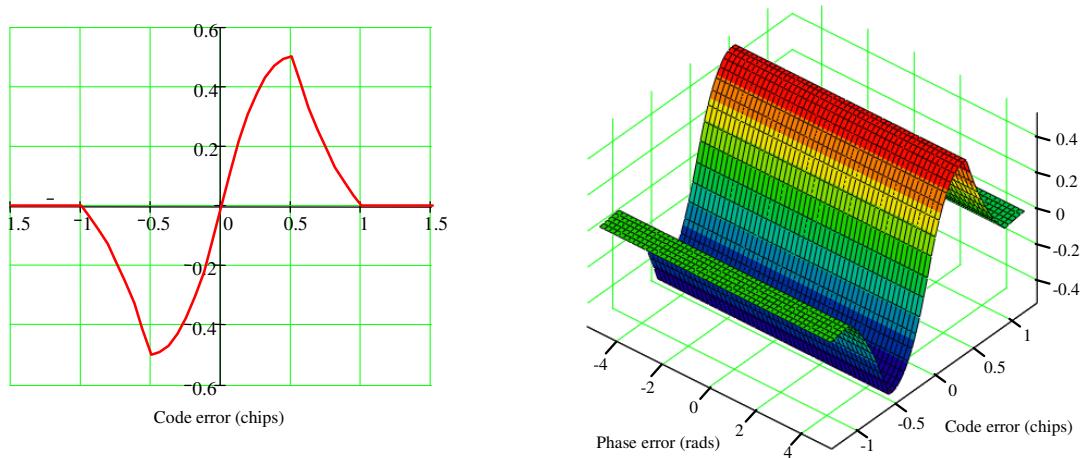


Figure D-1, Dot product discriminator characteristic

It is desirable to avoid normalisation in the receiver tracking loops in order to reduce microprocessor burden. A common practice is to design the loops for optimal performance at the weakest C/N_0 values the receiver is likely to experience and define a range of operation through simulation.

For example an early version of the SGR DLL was designed to give a loop bandwidth of 1Hz at a $C/N_0 = 40$ dB-Hz or a signal to noise per correlation (1ms) of 10dB.

Therefore, K_{CD} is a constant set to achieve a true error at $C/N_0 = 40$ dB-Hz.

However, the discriminator error diverges from the true error above and below this preset value. This has the effect of increasing the effective loop bandwidth for stronger input signal values and decreasing the loop bandwidth for weaker input signal strengths. The effect of input signal strength on loop bandwidth and DLL timing jitter is shown in Figure D-2.

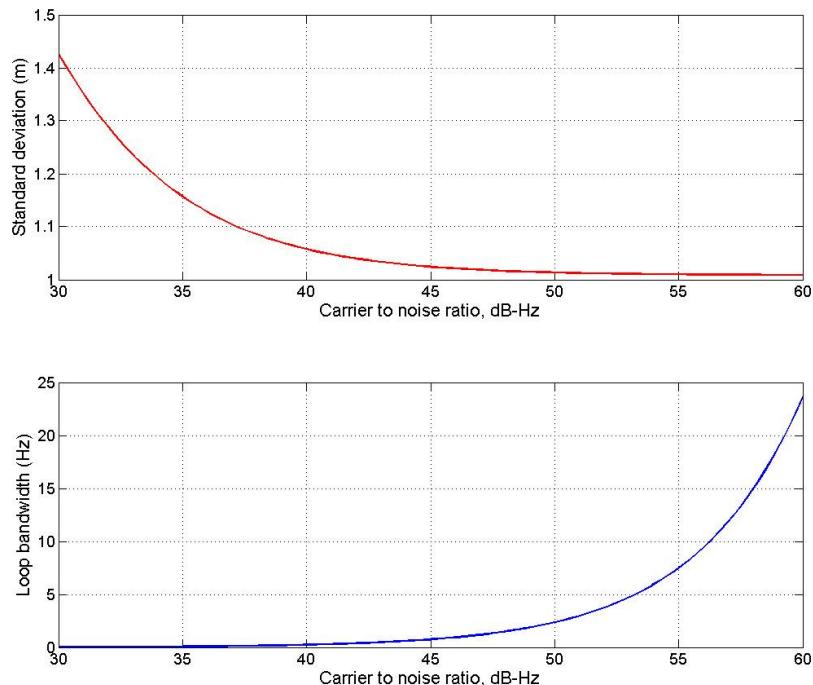


Figure D-2, SGR DLL loop bandwidth and timing jitter against input C/N_0

The changes to loop bandwidth with input C/N_0 define limits to the range of reliable receiver operation. Figure D-3 shows the results of subjecting the SGR DLL to increasing strong input signal levels. The timing jitter remain around 1m (predicted by Figure D-2), however at around $C/N_0 = 54$ dB-Hz the loop begins to oscillate giving large timing errors (>50 m).

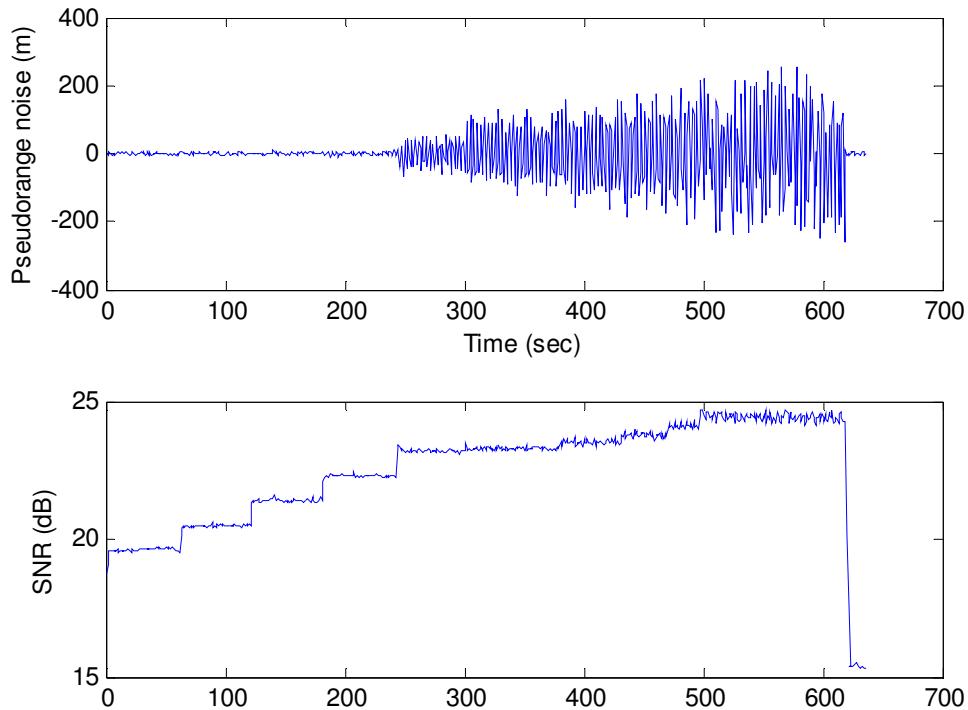


Figure D-3, SGR DLL pseudorange noise and receiver estimated SNR(dB-kHz)

The above example shows the importance of DLL amplitude dependence, although this issue is of equal importance to PLL, FLL and SLL designs. When using a discriminator with any kind of amplitude dependence, extreme care must be taken by the designer to insure the receiver will not be operating outside its reliable range. Clearly using normalised discriminators, which remove the amplitude dependence, is essential for high reliability application. However, if the receiver hardware will not support this, loop designs with consideration of the receiver's future environment of operation are required.

E Choosing a bump jumping threshold

GNSS BOC receivers operating the *bump-jumping* (BJ) algorithm must identify a BJ threshold. This threshold should be set high enough so that when the receiver is tracking the central BOC correlation peak occasional noise induced increments of the very early, VE or very late VL counters will never exceed this value. This would trigger a *false alarm* and actually cause the receiver to action a jump away from the valid tracking state.

In order to determine this threshold we first followed the approach of [Fine and Wilson 1999], assuming uncorrelated VE, P and VL correlations with random Gaussian noise on each on each correlation. In order to identify our results with this paper we consider in-phase correlations with a signal to noise per correlation of $S/N_I = 10 \text{ dB}$ and a $\text{BOC}(2\times f_C, f_C)$ signal (see Figure E-1).

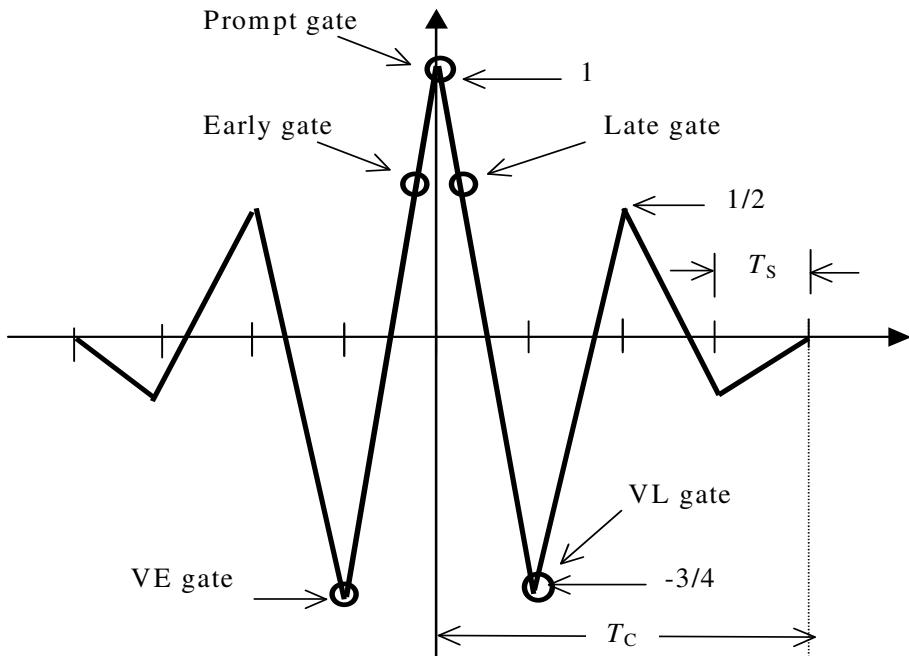


Figure E-1, $\text{BOC}(2\times f_C, f_C)$ false-lock example with BJ gates

The Mathcad simulation program for uncorrelated noise samples is shown in Figure E-2. The worse case of many trials identifies a threshold of 8 (see Figure E-3) which corresponds to the analysis and threshold choice in [Fine and Wilson 1999].

$$x_0 := -0.75 \quad y_0 := 1 \quad z_0 := -0.75 \quad N := 1000 \quad ve_0 := 0 \quad vl_0 := 0 \quad \sigma := \frac{1}{\sqrt{10}}$$

$$x := rnorm(N, x_0, \sigma) \quad y := rnorm(N, y_0, \sigma) \quad z := rnorm(N, z_0, \sigma)$$

$$k := 1..N - 1$$

$$f(ve, x, y, z) := \begin{cases} ve \leftarrow ve + 1 & \text{if } (|x| > |y|) \wedge (|x| > |z|) \\ ve \leftarrow ve - 1 & \text{if } (|y| > |x|) \wedge (|y| > |z|) \\ ve \leftarrow 0 & \text{if } ve < 0 \\ ve \end{cases}$$

$$g(vl, x, y, z) := \begin{cases} vl \leftarrow vl + 1 & \text{if } (|z| > |y|) \wedge (|z| > |x|) \\ vl \leftarrow vl - 1 & \text{if } (|y| > |x|) \wedge (|y| > |z|) \\ vl \leftarrow 0 & \text{if } vl < 0 \\ vl \end{cases}$$

$$ve_k := f(ve_{k-1}, x_{k-1}, y_{k-1}, z_{k-1})$$

$$vl_k := g(vl_{k-1}, x_{k-1}, y_{k-1}, z_{k-1})$$

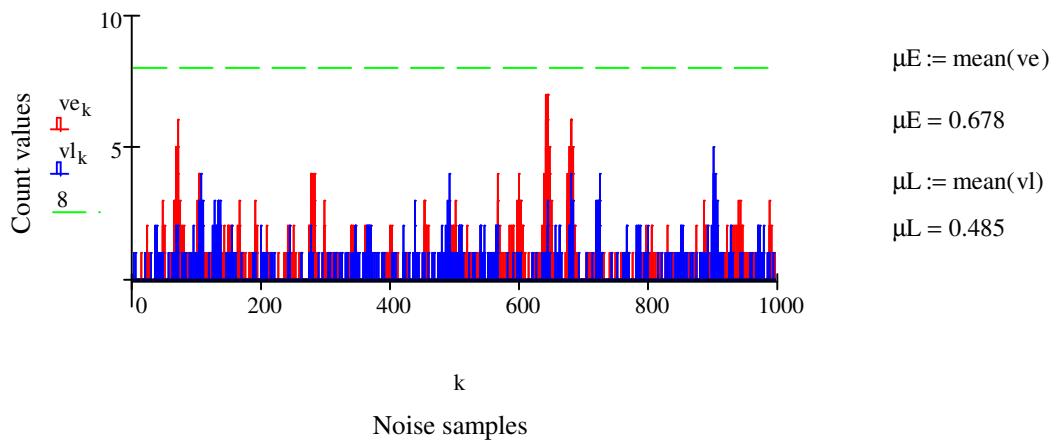


Figure E-2, Simulation of BJ threshold with uncorrelated noise samples

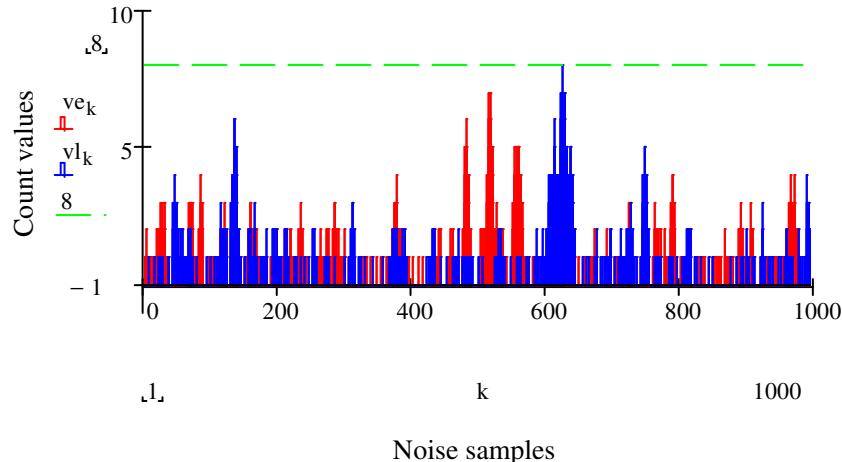


Figure E-3, Worse case VE and VL count values for BOC($2 \times f_c, f_c$) with uncorrelated signal to noise of 10 dB per correlation

However, as identified by Dr Hodgart, the noise samples are in fact strongly correlated which actually improves the performance of the BJ algorithm. For BOC($2 \times f_c, f_c$) the correlation coefficient between noise separated by T_S and therefore between VE and P and between VL and P is $\rho = -0.75$. The correlation coefficient of noise between the VE and VL samples is $\rho = -0.5$. For simulation an easy way to create the three correlated noise samples, n_x , n_y , and n_z , from three uncorrelated noise samples u, v and w is by linear combination as

$$\begin{aligned} n_x &= +u - v - w \\ n_y &= +u + v + w \\ n_z &= -u + v - w \end{aligned} \quad \text{E-1}$$

where

$$\langle u^2 \rangle = \frac{\sigma^2}{8} \quad \langle v^2 \rangle = \frac{\sigma^2}{8} \quad \langle w^2 \rangle = \frac{3\sigma^2}{4} \quad \text{E-2}$$

The Mathcad simulation program for uncorrelated noise samples is shown in Figure E-4. The resulting worse case noise induced count values for correlated noise are shown in Figure 5-26, which finds a required threshold of 5.

$$x_0 := -0.75 \quad y_0 := 1 \quad z_0 := -0.75 \quad N := 1000 \quad ve_0 := 0 \quad vl_0 := 0 \quad \sigma := \frac{1}{\sqrt{10}}$$

$$u := rnorm\left(N, 0, \frac{\sigma}{\sqrt{8}}\right) \quad v := rnorm\left(N, 0, \frac{\sigma}{\sqrt{8}}\right) \quad w := rnorm\left(N, 0, \sigma \cdot \sqrt{\frac{3}{4}}\right)$$

$$k := 1..N-1$$

$$x := u - v - w \quad y := u + v + w \quad z := -u + v - w$$

$$\frac{1}{\sigma^2 \cdot (N-1)} \cdot \left[\sum_k (x_k \cdot y_k) \right] = -0.768 \quad \frac{1}{\sigma^2 \cdot (N-1)} \cdot \left[\sum_k (y_k \cdot z_k) \right] = -0.756$$

$$\frac{1}{\sigma^2 \cdot (N-1)} \cdot \left[\sum_k (x_k \cdot z_k) \right] = 0.511$$

$$x := x - 0.75 \quad y := y + 1 \quad z := z - 0.75$$

$$f(ve, x, y, z) := \begin{cases} ve \leftarrow ve + 1 & \text{if } (|x| > |y|) \wedge (|x| > |z|) \\ ve \leftarrow ve - 1 & \text{if } (|y| > |x|) \wedge (|y| > |z|) \\ ve \leftarrow 0 & \text{if } ve < 0 \\ ve \end{cases}$$

$$g(vl, x, y, z) := \begin{cases} vl \leftarrow vl + 1 & \text{if } (|z| > |y|) \wedge (|z| > |x|) \\ vl \leftarrow vl - 1 & \text{if } (|y| > |x|) \wedge (|y| > |z|) \\ vl \leftarrow 0 & \text{if } vl < 0 \\ vl \end{cases}$$

$$ve_k := f(ve_{k-1}, x_{k-1}, y_{k-1}, z_{k-1})$$

$$vl_k := g(vl_{k-1}, x_{k-1}, y_{k-1}, z_{k-1})$$

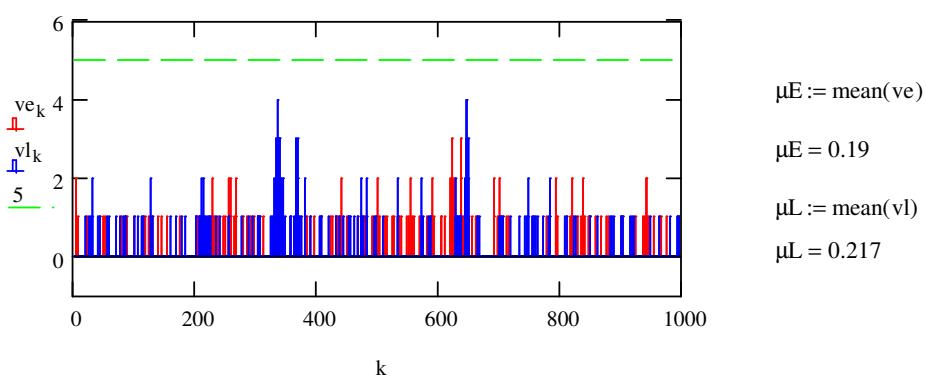


Figure E-4, Simulation of BJ threshold with correlated noise samples

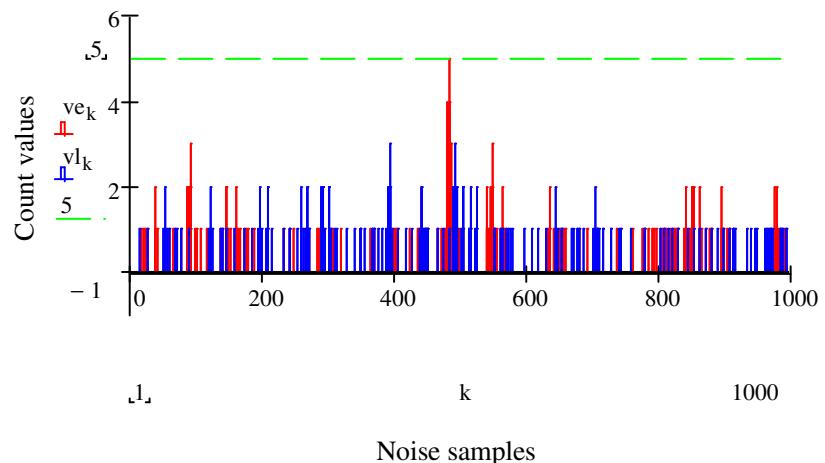


Figure E-5, Worse case VE and VL count values for BOC($2 \times f_C, f_C$) with correlated noise samples, signal to noise of 10 dB per correlation

F Digital Noise Synthesis

This appendix was kindly supplied by Dr Hodgart and provides the formulas necessary to synthesise additive noise in GNSS signal generators.

F.1 Introduction

The aim is to create a simulation on a transmitter of electrical noise to be added to an encoded GNSS signal and then together to be converted into a representation of an analogue signal at a given intermediate frequency f_0 . The proposed system in the following analogue representation is

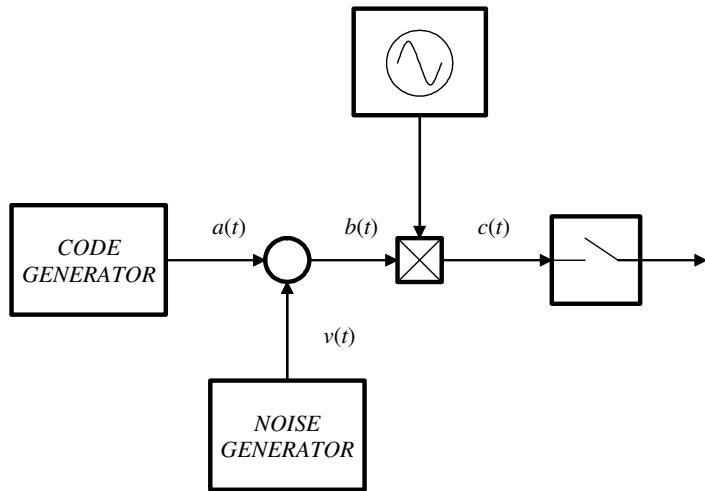


Figure F-1, Noise synthesis

Precision to the concept is provided by an arithmetic/algebraic representation. We take the GPS transmission known as ‘L1’ as an example, which generates a ‘code chip’ every 1/1.023 μ sec. Notation here for each code chip is $a[k]$, counting continuously in k . Allowed values of $a[]$ acknowledge its bipolarity i.e. two possible integer values $-A$ or $+A$.

The chip sequence is periodic in a count 1023. So $a[k] = a[n \times 1023 + k]$ where n is any integer. This periodicity is not relevant in the following analysis.

We use the example of the SSTL Galileo signal generator, which creates an i.f. of frequency $f_0 = 60 \times 1.023 = 61.38$ MHz. Therefore, in the absence of synthetic added noise, a multi-rate sequence must be created as in

$$\begin{aligned} b[k] &= a[k/120] \\ c[k] &= b[k] \times (-1)^k \end{aligned} \quad \text{F-1}$$

where the [] notation always means ‘integer’ or ‘floor’ to what may be a real number. So

$$a[119/120] = a[0]$$

but

$$a[121/120] = a[1]$$

So here

$$\begin{aligned} c[0] &= a[0] \\ c[1] &= -a[0] \end{aligned} \quad \text{F-2}$$

up to

$$c[119] = -a[0]$$

then

$$c[120] = a[1] \quad \text{F-3}$$

and so on

Each code chip in this proposal is transmitted therefore in a sequence of alternating 120 samples - so creating the ‘digital’ equivalent of an IF at 60 times the code rate. We will define a sampling rate $f_S = 2f_0 = 122.76$ MHz.

F.2 Adding noise

The proposal is to add an integer noise sequence. The particular suggestion here is to create this noise and add it to the signal before multiplication to $u[k]$. The sequence of samples is $u[0], u[1] \dots u[k]$ where each sample is uncorrelated to any other sample.

The probability distribution is quasi-Gaussian with a known standard deviation σ (which need not be integer).

The aim is to create a pseudo noise sequence which will reproduce a precisely calculated C/N_0 in a bench test transmission to a receiver.

The proposal here is to create a variable rate noise sequence to be added to the code but before multiplication. So write for example

$$\begin{aligned} b[k] &= a[k/120] + u[k/2] \\ c[k] &= b[k] \times (-1)^k \end{aligned} \quad \text{F-4}$$

which equation says to add noise on every sample but only update it every other sample - i.e. at the rate of 61.38 MHz.

At the other extreme we could write

$$\begin{aligned} b[k] &= a[k/120] + u[k/120] \\ c[k] &= b[k] \times (-1)^k \end{aligned} \quad \text{F-5}$$

which equation says to add noise on every sample but only update it on a new code bit i.e. at a rate of 1.023 MHz.

Define a sampling rate to code rate ratio $K_{SC} = f_S/f_C$ and in general write

$$\begin{aligned} b[k] &= (a[k/K_{SC}] + v[k/K_N]) \\ c[k] &= b[k] \times (-1)^k \end{aligned} \quad \text{F-6}$$

where K_N is a decimation factor (and must be divisible into the sampling to code rate ratio (which here is $K_{SC} = 120$)).

Define also a noise update rate

$$f_N = \frac{f_S}{K_N} \quad \text{F-7}$$

and since

$$f_S = K_{SC} f_C \quad \text{F-8}$$

$$f_N = \left(\frac{K_{SC}}{K_N} \right) f_C \quad \text{F-9}$$

Examples

$$61.38 = \left(\frac{120}{2} \right) \times 1.023 \quad 6.138 = \left(\frac{120}{20} \right) \times 1.023 \quad 1.023 = \left(\frac{120}{120} \right) \times 1.023$$

F.3 Achieved C/N₀

On every independent sample then the signal to noise is

$$\Gamma^2 = \frac{A^2}{\sigma^2} \quad \text{F-10}$$

where σ is the rms value of the synthesised noise . For an 8-bit representation the optimum value will be around $\sigma = 40$ units allowing deviations of near $\pm 3\sigma$. For an update rate f_N then in an observation interval T_L there will be an effective number of averages = $f_N T_L$ and the achieved signal to noise will be

$$\gamma^2 = \frac{A^2}{\sigma^2} \times f_N T_L \quad \text{F-11}$$

From standard theory it can be shown that in an equivalent analogue world with a white noise of density N_0 the achieved signal to noise in a coherent receiver

$$\gamma^2 = \frac{2A^2 T_L}{N_0} = 2 \times \frac{C}{N_0} \times T_L \quad \text{F-12}$$

Therefore the effective carrier to noise density ratio

$$\frac{C}{N_0} = \frac{2A^2 f_N}{\sigma^2}$$

F-13

or in terms of the sampling frequency f_S and decimation factor K_N

$$\frac{C}{N_0} = \frac{2}{K_N} \times \frac{A^2 f_S}{\sigma^2}$$

F-14

F.4 Effective v. actual carrier to noise density ratio

This formula (F–13) computes a value which is *double* that worked out by Fourier Analysis in a first draft of this note. Allowing for up conversion and a comparison of the carrier power against the noise density at the carrier frequency it is found that

$$\frac{C}{N_0} = \frac{A^2 f_N}{\sigma^2} \quad \text{F-15}$$

The question then is which formula is correct? The answer is that both are! Equation F–15 is the *actual C/N₀* after up-conversion while Equation F–13 is the *effective C/N₀* after up-conversion. The explanation of these different meanings is that the noise which is synthesised by this method is not a true synthesis of normal thermal noise - because *upper and lower sidebands are inherently correlated*.

F.5 Example implementation

Set a minimum possible value to $A = 1$ and a likely maximum to $\sigma = 40$ (allowing Gaussian noise with an excursion of $\pm 3\sigma$ in range ± 128). Initially we choose a rapid noise update rate of $f_N = 61.38$ MHz. This defines a decimation factor $K_N = 2$ for $f_S = 122.76$ MHz. Noise is updated every two samples of the time sequence. Then C/N_0 calculates here to

$$\frac{C}{N_0} = \frac{2}{2} \times \frac{122.76}{40^2} \times 10^6 = 76.7 \times 10^3 \text{ Hz} \quad \text{F-16}$$

or 48.8 dB-Hz

This is actually rather a high value. We should be able to synthesis down to at least a ‘representative minimum’ of say 38 dBHz, which is 10.8 dB down on this. And if we really want to test performance of the receiver we shall need to go even lower. With our current proposal this is no problem. So for example with a reduced noise update rate $f_N = 6.138 \times 10^6$ and therefore a decimation factor of 20 then

$$\frac{C}{N_0} = \frac{2}{20} \times \frac{122.76}{40^2} \times 10^6 = 2 \times \frac{6.138}{40^2} \times 10^6 = 7.67 \times 10^3 \text{ Hz} \quad \text{F-17}$$

or 38.8 dB-Hz

Even lower update rate $f_N = 1.023 \times 10^6$ and therefore a decimation factor of $K_N = 120$ finds that

$$\frac{C}{N_0} = \frac{2}{120} \times \frac{122.76}{40^2} \times 10^6 = 2 \times \frac{1.023}{40^2} \times 10^6 = 1.28 \times 10^3 \text{ Hz} \quad \text{F-18}$$

or 31.1 dB-Hz

In this scenario then there are many options in setting the decimation value. For $K_{SC} = 120$ then possible values

$$K_N = (2, 3, 4, 5, 6, 8, 10, 12, 15, 20, 30, 40, 60, 120)$$

If we want to go even lower than this then the algorithm needs to be modified so that the noise update rate is *slower* than the code rate.

F.6 Spectral analysis

Spectral analysis at the highest proposed noise update rate $f_N = 61.38$ MHz shows a pronounced ‘skew’ of the power density - which does not peak where we want it (although the spot value is correct).

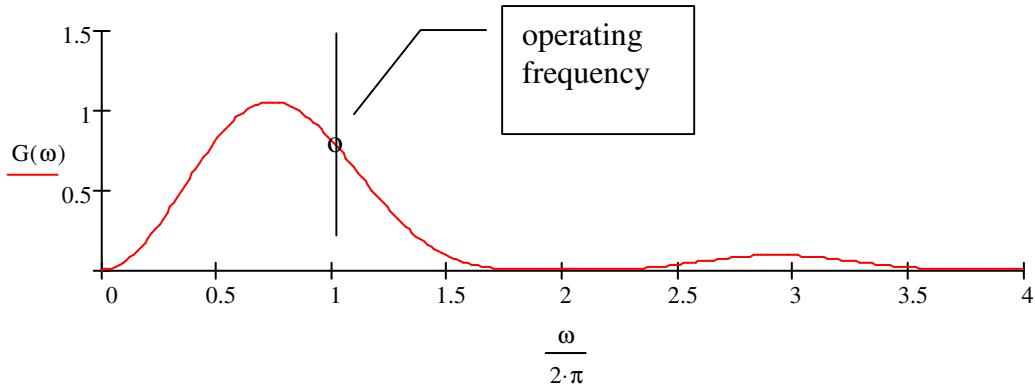


Figure F-2, Power spectrum with $N_D = 2$ noise decimation

The function being plotted is

$$G(\omega) = \left(2\sigma^2 T_0\right) \left\{ \frac{\sin\left(\frac{\omega T_0}{4}\right)^2}{\frac{\omega T_0}{4}} \right\} \quad \text{F-19}$$

where here $1/T_0 = 61.38$ MHz

There seems little point in trying to improve on this since the correlation action in the receiver effectively applies a narrow band filter in the order of kHz. In any case with higher decimation factors the spectrum increasingly centralises. For example with an increase to $K_N = 4$ the spectrum has already shifted appropriately:

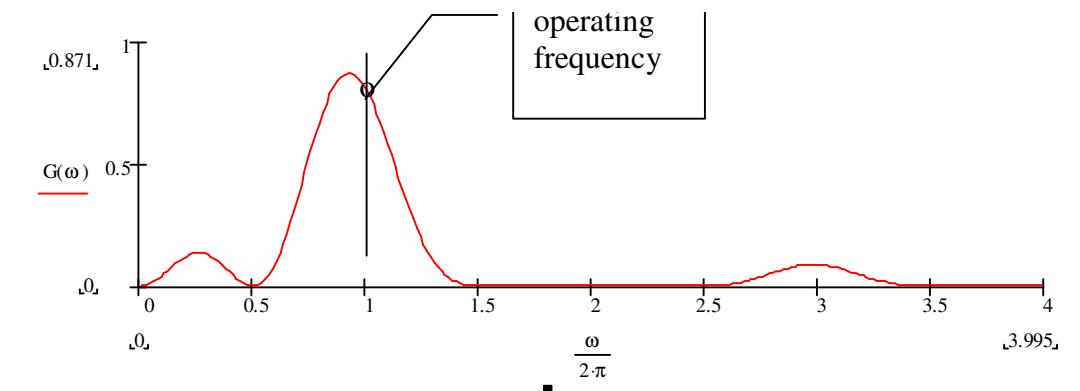


Figure F-3, Power spectrum with $N_D = 4$ noise decimation

The proposed digital simulation will provide for a highly accurate testing of receiver performance since the noise level is precisely specified.

F.7 PSK analysis

The aim is to add a precisely controlled amount of noise to otherwise ‘clean’ bench-generated GPS signal modulating an IF of 61.38 MHz.

The following analysis is first expressed in terms of standard L1 C/A code GPS.

Consider first a digital baseband construction – called a unit amplitude $a[]$ sequence in the appendix - scaled up to an amplitude A . There are 1023 chips following the prescribed code rule in interval $T = 1$ ms.

In the modulator, from $a[]$ form a what we call a $b[]$ sequence which – in the absence of noise - consists of 120 repeated samples of each chip. The sample rate $f_s = 122.76$ MHz. To form an IF sequence $c[]$ at 61.38 MHz is simply a matter of alternating the sample sequence $b[]$.

The digital noise synthesis consists of adding independent random samples $u[]$ of synthesised Gaussian noise to the $A \times b[]$ sequence. The perceived difficulty for a scheme of fixed sample rate is the difficulty in realising a sufficiently high level of noise. In a digital realisation in amplitude is that minimum signal amplitude is necessary $A = 1$ while a typical maximum $\sigma = 40$ (allowing Gaussian noise in a range $\pm 3\sigma$ over 8 bit representation ± 128).

Independent noise of r.m.s. value σ could be added on every sample at rate $f_N = 122.76$ MHz. to every term in $A \times b[]$.

We can however lower the update rate of noise in the range downward to $f_N = 1.023$ MHz by allowed multiples.

This has the effect of increasing the effective noise level after demodulation

Now consider a de-modulation stage where the $c[]$ is sign alternated back to $b[]$ and envisage a correlation stage clocked at 61.38 kHz which processes all the samples

In the case of perfect lock and no noise sequence $A \times b[]$ can be recovered will line up with a unit replica $b_R[] = b[]$. Envisage running a correlation over 1 periodic interval $T = 1$ msec. In this somewhat impractical scenario there will be a total of $N = 1023 \times 120 = 122760$ terms to be summed as in

$$\Lambda[0] = \frac{A}{N} \sum_0^{N-1} b[k] b_R[k] = A \quad \text{F-20}$$

In a correlation time T there are $f_N T$ independent noise samples
the achieved signal to noise after correlation depends on the number of independent noise samples within that interval T .

It is easily argued that achieved signal to noise

$$\gamma^2 = \frac{A^2}{\sigma^2} \times T \times f_N \quad \text{F-21}$$

which is maximum on $f_N = 122.76$ MHz when $f_N T = 122,760$ and is a minimum on $f_N = 1.023$ MHz when $f_N T = 1023$.

This gives us a noise range over 120 : 1 . We may note that this is a purely *digital* argument. This result can be generalized to an extended correlation time T_L defined by a loop response to read

$$\gamma^2 = \frac{A^2}{\sigma^2} \times T_L \times f_N \quad \text{F-22}$$

Comparing then against a standard formula for GPS base band signal in presence of analogue low pass (white approximation) of one-sided density η

$$\gamma^2 = 2 \times \frac{A^2}{\eta} \times T_L \quad \text{F-23}$$

It can be shown then for a phase locked I channel that equivalently

$$\gamma^2 = 2 \times \frac{C}{N_0} \times T_L \quad \text{F-24}$$

where C is the carrier power before demodulation and N_0 is the band-pass one sided noise density(white approximation). Therefore we have synthesised a noise channel where

$$\frac{C}{N_0} = \frac{2A^2 f_N}{\sigma^2} \quad \text{F-25}$$

F.8 Extension to BOC analysis

A similar argument finds that one can use exactly the same formulas provided an appropriate restriction on range on f_N is observed. It is necessary to have at least one independent noise sample per *sub-chip* which restricts how low one can go with f_N .

Example BOC(1,1). Here there are two sub-chips within one chip of $1/1.023 \mu\text{s}$. Therefore lowest allowed value to $f_N = 2.046 \text{ MHz}$. Highest value is still $f_N = 122.76 \text{ MHz}$. In spectral terms a ‘sub-chip’ pulse of *noise* covers the range ± 2.046 and therefore satisfactorily covers the two main lobes.

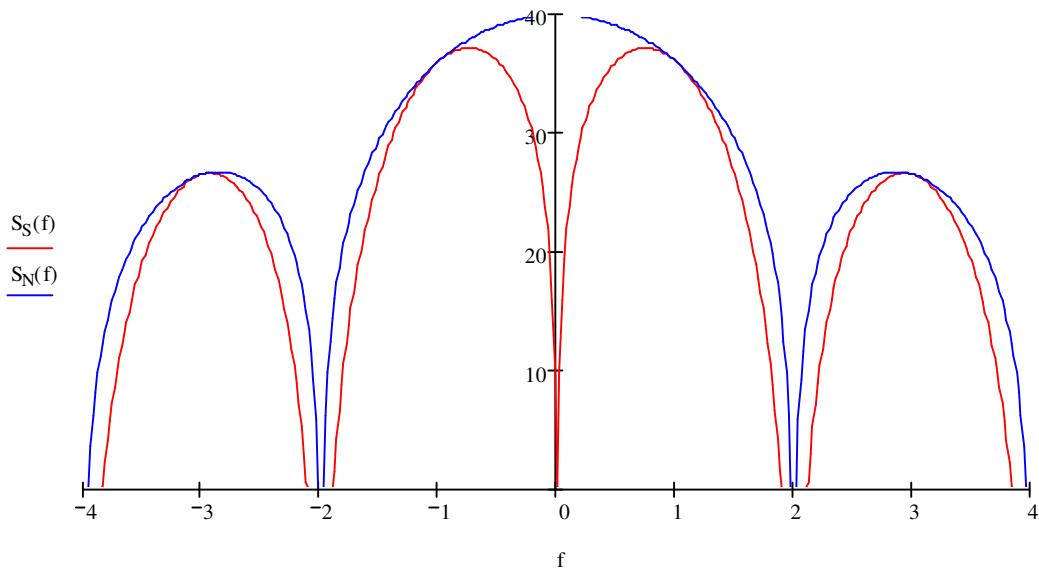


Figure F-4, Spectral plots of BOC(1, 1) signal (red) and digital noise (blue)

$$f_s = 1 \text{ MHz}, f_c = 1 \text{ MHz}, f_N = 2 \text{ MHz}$$

Example BOC(10,5). Lowest allowed $f_N = \text{subchip rate} = 20.46 \text{ MHz}$. Highest value is still $f_N = 122.76 \text{ MHz}$. In spectral terms a ‘sub-chip’ pulse of *noise* covers the range $\pm 20.46 \text{ MHz}$ and therefore satisfactorily covers the two main lobes.

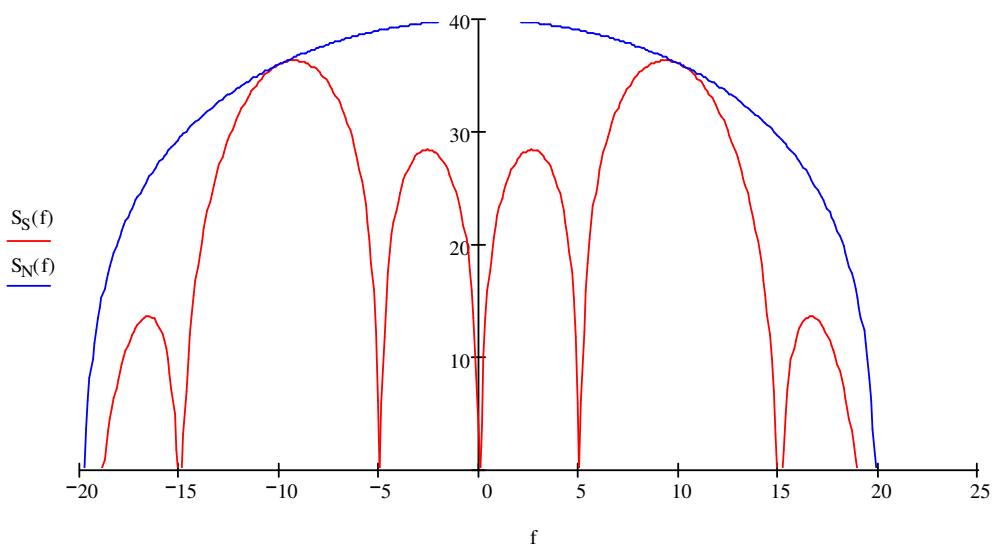


Figure F-5, Spectral plots of BOC(10, 5) signal (red) and digital noise (blue)

$$f_s = 10 \text{ MHz}, f_c = 5 \text{ MHz}, f_N = 20 \text{ MHz}$$

G FPGA Correlator Registers

Register name	Description
System registers	
PROG_ACCUM_INT	Contains a count value for generating the interrupt for the processor to read the accumulation data (nominally 854us)
PROG_TIC_HIGH	Contains the higher 16-bits of the TIC count value (nominally 0.1s)
PROG_TIC_LOW	Contains the lower 16-bits of the TIC count value (nominally 0.1s)
TEST_CONTROL	Enables
ACCUM_STATUS_A	Contains flags telling the processor new accumulation data is ready for each tracking channel
INPUT_SIGNAL	Contains samples of the input signal for AGC and noise testing
Channel registers (read)	
CODE_DCO_PHASE	Contains the fractional part of the code phase measured synchronised with the TIC from the code DCO
CODE_PHASE	Contains the half chips of the code phase measured synchronised with the TIC
CARRIER_DCO_PHASE	Contains the fractional part of the carrier phase measured synchronised with the TIC from the carrier DCO
CARRIER_CYCLE_LOW	Contains the lower 16-bits of the carrier cycle count in a single TIC
CARRIER_CYCLE_HIGH	Contains the higher 16-bits of the carrier cycle count in a single TIC
SUB_DCO_PHASE	Contains the fractional part of the sub-carrier phase measured synchronised with the TIC from the sub-carrier DCO
SUB_CYCLE_LOW	Contains the lower 16-bits of the sub-carrier cycle count in a single TIC
SUB_CYCLE_HIGH	Contains the higher 16-bits of the sub-carrier cycle count in a single TIC
w_III_LOW	Contains the lower 16-bits of the wIII correlation
w_III_HIGH	Contains the higher 16-bits of the wIII correlation
w_IIE_LOW	Contains the lower 16-bits of the wIIE correlation
w_IIE_HIGH	Contains the higher 16-bits of the wIIE correlation
w_IQI_LOW	Contains the lower 16-bits of the wIQI correlation
w_IQI_HIGH	Contains the higher 16-bits of the wIQI correlation
w_QIE_LOW	Contains the lower 16-bits of the wQIE correlation
w_QIE_HIGH	Contains the higher 16-bits of the wQIE correlation
w_QII_LOW	Contains the lower 16-bits of the wQII correlation
w_QII_HIGH	Contains the higher 16-bits of the wQII correlation

w_IIL_LOW	Contains the lower 16-bits of the wIIL correlation
w_IIL_HIGH	Contains the higher 16-bits of the wIIL correlation
w_QQI_LOW	Contains the lower 16-bits of the wQQI correlation
w_QQI_HIGH	Contains the higher 16-bits of the wQQI correlation
w_QIL_LOW	Contains the lower 16-bits of the wQIL correlation
w_QIL_HIGH	Contains the higher 16-bits of the wQIL correlation
Channel registers (write)	
SATCNTL	Selects which satellite the individual channel tracks and also selects different tracking modes
CARRIER_DCO_INCR_HIGH	Selects the higher 16-bits of the carrier DCO increment per sample clock period
CARRIER_DCO_INCR_LOW	Selects the lower 16-bits of the carrier DCO increment per sample clock period
CODE_DCO_INCR_HIGH	Selects the higher 16-bits of the code DCO increment per sample clock period
CODE_DCO_INCR_LOW	Selects the lower 16-bits of the code DCO increment per sample clock period
CODE_SLEW_COUNTER	Selects the code slew the user wish to impart on the replica signal in half chips
SUB_DCO_INCR_HIGH	Selects the higher 16-bits of the sub-carrier DCO increment per sample clock period
SUB_DCO_INCR_LOW	Selects the lower 16-bits of the sub-carrier DCO increment per sample clock period

H Derivation of exact timing formulas for sine and cosine BOC

This appendix was kindly supplied by Dr Hodgart and provides the derivation of timing jitter of both sine BOC (sBOC) and cosine BOC (cBOC) modulations.

H.1 Direct analysis for sBOC(1,1)

Identify chip width T_C , sub-chip width T_S

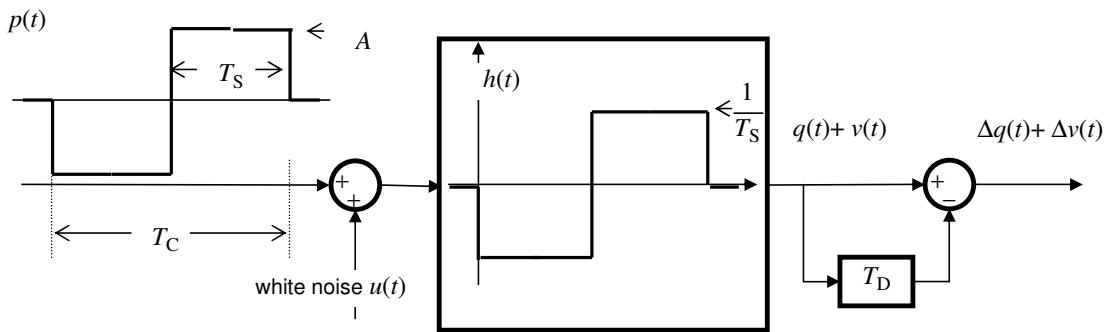


Figure H-1, Delay line subtractor for sBOC(1,1)

main peak noiseless output $q(0) = 2A$

at displacement T output $q(T_S) = -A$

Initially choose delay line subtractor also $T_D = T_S$

Therefore maximum positive and negative peak in $\Delta q(t) = \pm 3A$

Slope in $\Delta q(t) = 6A/T_S$

Equivalent difference impulse response

$$\Delta h(t) = h(t) - h(t - T_S) \quad \text{H-1}$$

Then noise out

$$\langle \Delta v^2 \rangle = \frac{\eta}{2} \int \Delta h(t)^2 dt = \frac{\eta}{2} \frac{1}{T_S} (1^2 + 2^2 + 1^2) = \frac{\eta}{2} \frac{6}{T_S} \quad \text{H-2}$$

therefore mean square noise jitter for just one pulse (duration T_C)

$$\Sigma^2 = \frac{\eta}{2} \times \frac{6}{T_S} \times \left(\frac{T_S}{6A} \right)^2 = \frac{\eta}{2} \times \frac{T_S}{6A^2} \quad \text{H-3}$$

This is reduced in a loop system of effective integration time T_L to

$$\Sigma^2 \rightarrow \frac{\eta}{2} \times \frac{T_S}{6A^2} \times \frac{T_C}{T_L} \quad \text{H-4}$$

One can show that $A^2/\eta = C/N_0$ in a phase synchronised I-channel. Also equivalent loop bandwidth

$$2B_L = \frac{1}{T_L} \quad \text{H-5}$$

Therefore

$$\Sigma^2 \rightarrow \frac{2B_L}{C/N_0} \times \frac{T_S}{6} \times \frac{T_C}{2} = \frac{2B_L}{C/N_0} \times \frac{T_S}{6} \times T_S \quad \text{H-6}$$

Further analysis finds that provided the delay time $T_D \leq T_S$ then the

$$\Sigma^2 = \frac{2B_L}{C/N_0} \times \frac{T_D}{6} \times T_S \quad \text{H-7}$$

Generalisation.

Further analysis finds that

$$\Sigma^2 = \frac{2B_L}{C/N_0} \times \frac{T_D}{4 \times \left(2 - \frac{T_S}{T_C}\right)} \times T_S \quad T_D \leq T_S \quad \text{H-8}$$

H.2 Direct analysis for cBOC(1,1)

Identify chip width T_C , sub-chip width T_S and half sub-chip width $T = T_S$ where

$$T_C = 2T_S$$

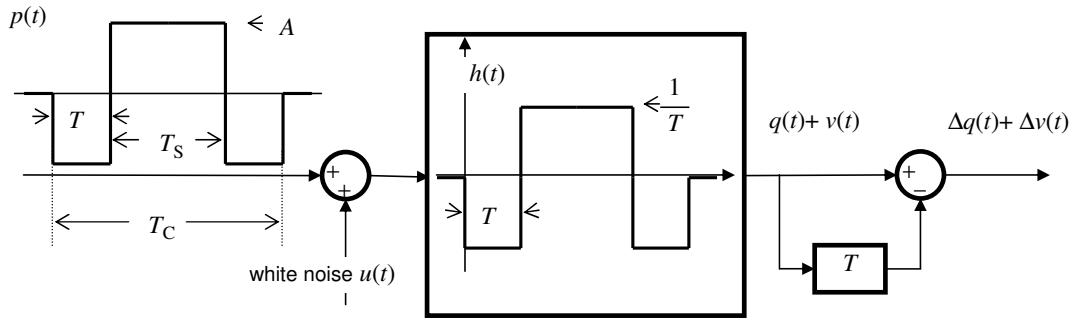


Figure H-2, Delay line subtractor for cBOC(1,1)

main peak noiseless output $q(0) = 4A$

at displacement T output $q(T) = -A$

Initially choose delay line subtractor also $T_D = T$

Therefore maximum positive and negative peak in $\Delta q(t) = \pm 5A$

Slope in $\Delta q(t) = 10A/T$

Equivalent difference impulse response

$$\Delta h(t) = h(t) - h(t-T) \quad \text{H-9}$$

Then noise out

$$\langle \Delta v^2 \rangle = \frac{\eta}{2} \int \Delta h(t)^2 dt = \frac{\eta}{2} \frac{1}{T} (1^2 + 2^2 + 0^2 + 2^2 + 1^2) = \frac{\eta}{2} \frac{10}{T} \quad \text{H-10}$$

therefore mean square noise jitter for just one pulse (duration T_C)

$$\Sigma^2 = \frac{\eta}{2} \times \frac{10}{T} \times \left(\frac{T}{10A} \right)^2 = \frac{\eta}{2} \times \frac{T}{10A^2} \quad \text{H-11}$$

This is reduced in a loop system of effective integration time T_L to

$$\Sigma^2 \rightarrow \frac{\eta}{2} \times \frac{T}{10A^2} \times \frac{T_C}{T_L} \quad \text{H-12}$$

One can show that $A^2/\eta = C/N_0$ in a phase synchronised channel. Also equivalent loop bandwidth

$$2B_L = \frac{1}{T_L} \quad \text{H-13}$$

Therefore

$$\Sigma^2 \rightarrow \frac{2B_L}{C/N_0} \times \frac{T}{10} \times \frac{T_C}{2} = \frac{2B_L}{C/N_0} \times \frac{T}{10} \times T_S \quad \text{H-14}$$

Further analysis finds that provided the delay time $T_D \leq T_S/2$ then the

$$\Sigma^2 = \frac{2B_L}{C/N_0} \times \frac{T_D}{10} \times T_S \quad \text{H-15}$$

Generalisation.

Further analysis finds that

$$\Sigma^2 = \frac{2B_L}{C/N_0} \times \frac{T_D}{4 \times \left(2 + \frac{T_S}{T_C} \right)} \times T_S \quad T_D \leq T_S / 2 \quad \text{H-16}$$

I AltBOC(15,10) lookup table

In Chapter 7 a simplified implementation technique for the generation of AltBOC 8-PSK modulation is described. The AltBOC signal can be written as follows.

$$S_{AltBOC}(t) = \text{sgn}\left[\sin\left(\frac{2\pi t}{T_s} + \theta_A\right)\right]\cos(\theta_B)\cos(\omega_{L5}t) + \text{sgn}\left[\sin\left(\frac{2\pi t}{T_s} + \theta_A\right)\right]\sin(\theta_B)\sin(\omega_{L5}t) \quad \text{I-1}$$

$\theta_A \in (0, \pi/4, \pi/2, 3\pi/4)$, $\theta_B \in (0, \pm\pi/4, \pm\pi/2, \pm 3\pi/4)$ and T_s is the sub-carrier period. θ_A defines the timing of 180° phase reversals of the carrier and θ_B chooses the pair of opposite phase points which are hopped between during the chipping interval. θ_A and θ_B are set by the 16 possible states of the input sequences using the look-up table shown in Table I-2. The AltBOC modulation can then be implemented as an 8-phase modulation shown in Figure I-1. Example mapping of the phase point to 8-bit DAC values is shown in Table I-1.

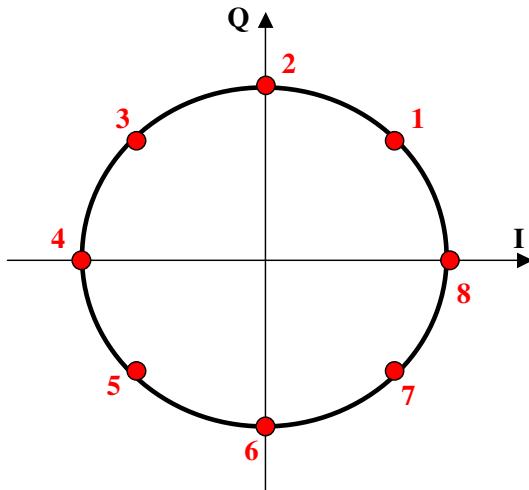


Figure I-1, AltBOC 8-PSK I/Q plot

Table I-1, Example 8-bit DAC mapping

Phase point	8-bit I value	8-bit Q value
1	218	218
2	127	255
3	36	218
4	0	127
5	36	36
6	127	0
7	218	36
8	255	127

Table I-2, AltBOC lookup table

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
θ_A	$\pi/2$	$\pi/4$	$3\pi/4$	$\pi/2$	$3\pi/4$	0	0	$\pi/4$	$\pi/4$	0	0	$3\pi/4$	$\pi/2$	$3\pi/4$	$\pi/4$	$\pi/2$
θ_B	$-3\pi/4$	π	π	$3\pi/4$	$-\pi/2$	$-\pi/4$	$-3\pi/4$	$\pi/2$	$-\pi/2$	$\pi/4$	$-3\pi/4$	$\pi/2$	$-\pi/4$	0	0	$\pi/4$
E5a data code	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
E5a pilot code	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
E5b data code	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
E5b pilot code	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1
Sub-carrier phase	Phase point															
$0 \rightarrow T_s/8$	5	4	4	3	6	7	5	2	6	1	3	2	7	8	8	1
$T_s/8 \rightarrow T_s/4$	5	8	4	3	6	7	5	6	2	1	3	2	7	8	4	1
$T_s/4 \rightarrow 3T_s/8$	1	8	4	7	6	7	5	6	2	1	3	2	3	8	4	5
$3T_s/8 \rightarrow T_s/2$	1	8	8	7	2	7	5	6	2	1	3	6	3	4	4	5
$T_s/2 \rightarrow 5T_s/8$	1	8	8	7	2	3	1	6	2	5	7	6	3	4	4	5
$5T_s/8 \rightarrow 3T_s/4$	1	4	8	7	2	3	1	2	6	5	7	6	3	4	8	5
$3T_s/4 \rightarrow 7T_s/8$	5	4	8	3	2	3	1	2	6	5	7	6	7	4	8	1
$7T_s/8 \rightarrow T_s$	5	4	4	3	6	3	1	2	6	5	7	2	7	8	8	1
$T_s \rightarrow 9T_s/8$	5	4	4	3	6	7	5	2	6	1	3	2	7	8	8	1
$9T_s/8 \rightarrow 5T_s/4$	5	8	4	3	6	7	5	6	2	1	3	2	7	8	4	1
$5T_s/4 \rightarrow 11T_s/8$	1	8	4	7	6	7	5	6	2	1	3	2	3	8	4	5
$11T_s/8 \rightarrow 3T_s/2$	1	8	8	7	2	7	5	6	2	1	3	6	3	4	4	5