// Verilated -\*- SystemC -\*-

// DESCRIPTION: Verilator output: Design implementation internals

// See Vsisc32\_core.h for the primary calling header

#include "Vsisc32\_core.h" // For This

#include "Vsisc32\_core\_\_Syms.h"

//--------------------

// STATIC VARIABLES

VL\_ST\_SIG8(Vsisc32\_core::\_\_Vtable1\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_code\_DX[128],3,0);

VL\_ST\_SIG8(Vsisc32\_core::\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_op[8],1,0);

VL\_ST\_SIG8(Vsisc32\_core::\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_1\_signed[8],0,0);

VL\_ST\_SIG8(Vsisc32\_core::\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_2\_signed[8],0,0);

VL\_ST\_SIG8(Vsisc32\_core::\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_out\_sel[8],1,0);

VL\_ST\_SIG8(Vsisc32\_core::\_\_Vtable3\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_next\_state[256],1,0);

//--------------------

VL\_SC\_CTOR\_IMP(Vsisc32\_core)

#if (SYSTEMC\_VERSION>20011000)

: clk("clk"), imem\_hwrite("imem\_hwrite"), imem\_hsize("imem\_hsize"),

imem\_hburst("imem\_hburst"), imem\_hmastlock("imem\_hmastlock"),

imem\_hprot("imem\_hprot"), imem\_htrans("imem\_htrans"),

imem\_hready("imem\_hready"), imem\_hresp("imem\_hresp"),

dmem\_hwrite("dmem\_hwrite"), dmem\_hsize("dmem\_hsize"),

dmem\_hburst("dmem\_hburst"), dmem\_hmastlock("dmem\_hmastlock"),

dmem\_hprot("dmem\_hprot"), dmem\_htrans("dmem\_htrans"),

dmem\_hready("dmem\_hready"), dmem\_hresp("dmem\_hresp"),

sup\_reset("sup\_reset"), dbg\_ndreset("dbg\_ndreset"),

dbg\_fullreset("dbg\_fullreset"), dbg\_irq("dbg\_irq"),

ext\_interrupts("ext\_interrupts"), imem\_haddr("imem\_haddr"),

imem\_hwdata("imem\_hwdata"), imem\_hrdata("imem\_hrdata"),

dmem\_haddr("dmem\_haddr"), dmem\_hwdata("dmem\_hwdata"),

dmem\_hrdata("dmem\_hrdata"), mon0("mon0"), mon1("mon1")

#endif

{

Vsisc32\_core\_\_Syms\* \_\_restrict vlSymsp = \_\_VlSymsp = new Vsisc32\_core\_\_Syms(this, name());

Vsisc32\_core\* \_\_restrict vlTOPp VL\_ATTR\_UNUSED = vlSymsp->TOPp;

// Sensitivities on all clocks and combo inputs

SC\_METHOD(eval);

sensitive << clk;

sensitive << ext\_interrupts;

sensitive << imem\_hrdata;

sensitive << imem\_hready;

sensitive << imem\_hresp;

sensitive << dmem\_hrdata;

sensitive << dmem\_hready;

sensitive << dmem\_hresp;

sensitive << sup\_reset;

sensitive << dbg\_ndreset;

sensitive << dbg\_fullreset;

sensitive << dbg\_irq;

// Reset internal values

// Reset structure values

\_ctor\_var\_reset();

}

void Vsisc32\_core::\_\_Vconfigure(Vsisc32\_core\_\_Syms\* vlSymsp, bool first) {

if (0 && first) {} // Prevent unused

this->\_\_VlSymsp = vlSymsp;

}

Vsisc32\_core::~Vsisc32\_core() {

delete \_\_VlSymsp; \_\_VlSymsp=NULL;

}

//--------------------

void Vsisc32\_core::eval() {

VL\_DEBUG\_IF(VL\_DBG\_MSGF("+++++TOP Evaluate Vsisc32\_core::eval\n"); );

Vsisc32\_core\_\_Syms\* \_\_restrict vlSymsp = this->\_\_VlSymsp; // Setup global symbol table

Vsisc32\_core\* \_\_restrict vlTOPp VL\_ATTR\_UNUSED = vlSymsp->TOPp;

#ifdef VL\_DEBUG

// Debug assertions

\_eval\_debug\_assertions();

#endif // VL\_DEBUG

// Initialize

if (VL\_UNLIKELY(!vlSymsp->\_\_Vm\_didInit)) \_eval\_initial\_loop(vlSymsp);

// Evaluate till stable

int \_\_VclockLoop = 0;

QData \_\_Vchange = 1;

do {

VL\_DEBUG\_IF(VL\_DBG\_MSGF("+ Clock loop\n"););

vlSymsp->\_\_Vm\_activity = true;

\_eval(vlSymsp);

if (VL\_UNLIKELY(++\_\_VclockLoop > 100)) {

// About to fail, so enable debug to see what's not settling.

// Note you must run make with OPT=-DVL\_DEBUG for debug prints.

int \_\_Vsaved\_debug = Verilated::debug();

Verilated::debug(1);

\_\_Vchange = \_change\_request(vlSymsp);

Verilated::debug(\_\_Vsaved\_debug);

VL\_FATAL\_MT(\_\_FILE\_\_,\_\_LINE\_\_,\_\_FILE\_\_,"Verilated model didn't converge");

} else {

\_\_Vchange = \_change\_request(vlSymsp);

}

} while (VL\_UNLIKELY(\_\_Vchange));

}

void Vsisc32\_core::\_eval\_initial\_loop(Vsisc32\_core\_\_Syms\* \_\_restrict vlSymsp) {

vlSymsp->\_\_Vm\_didInit = true;

\_eval\_initial(vlSymsp);

vlSymsp->\_\_Vm\_activity = true;

// Evaluate till stable

int \_\_VclockLoop = 0;

QData \_\_Vchange = 1;

do {

\_eval\_settle(vlSymsp);

\_eval(vlSymsp);

if (VL\_UNLIKELY(++\_\_VclockLoop > 100)) {

// About to fail, so enable debug to see what's not settling.

// Note you must run make with OPT=-DVL\_DEBUG for debug prints.

int \_\_Vsaved\_debug = Verilated::debug();

Verilated::debug(1);

\_\_Vchange = \_change\_request(vlSymsp);

Verilated::debug(\_\_Vsaved\_debug);

VL\_FATAL\_MT(\_\_FILE\_\_,\_\_LINE\_\_,\_\_FILE\_\_,"Verilated model didn't DC converge");

} else {

\_\_Vchange = \_change\_request(vlSymsp);

}

} while (VL\_UNLIKELY(\_\_Vchange));

}

//--------------------

// Internal Methods

void Vsisc32\_core::\_initial\_\_TOP\_\_1(Vsisc32\_core\_\_Syms\* \_\_restrict vlSymsp) {

VL\_DEBUG\_IF(VL\_DBG\_MSGF("+ Vsisc32\_core::\_initial\_\_TOP\_\_1\n"); );

Vsisc32\_core\* \_\_restrict vlTOPp VL\_ATTR\_UNUSED = vlSymsp->TOPp;

// Body

// INITIAL at ../../src/verilog/core/sisc32\_core.v:14

VL\_ASSIGN\_SII(3,vlTOPp->imem\_hsize, 2U);

// INITIAL at ../../src/verilog/core/sisc32\_core.v:13

VL\_ASSIGN\_SII(1,vlTOPp->imem\_hwrite, 0U);

}

void Vsisc32\_core::\_settle\_\_TOP\_\_2(Vsisc32\_core\_\_Syms\* \_\_restrict vlSymsp) {

VL\_DEBUG\_IF(VL\_DBG\_MSGF("+ Vsisc32\_core::\_settle\_\_TOP\_\_2\n"); );

Vsisc32\_core\* \_\_restrict vlTOPp VL\_ATTR\_UNUSED = vlSymsp->TOPp;

// Variables

VL\_SIGW(\_\_Vtemp9,95,0,3);

VL\_SIGW(\_\_Vtemp32,95,0,3);

VL\_SIGW(\_\_Vtemp34,95,0,3);

VL\_SIGW(\_\_Vtemp36,95,0,3);

VL\_SIGW(\_\_Vtemp38,95,0,3);

VL\_SIGW(\_\_Vtemp40,95,0,3);

VL\_SIGW(\_\_Vtemp42,95,0,3);

VL\_SIGW(\_\_Vtemp44,95,0,3);

VL\_SIGW(\_\_Vtemp46,95,0,3);

VL\_SIGW(\_\_Vtemp48,95,0,3);

VL\_SIGW(\_\_Vtemp50,95,0,3);

VL\_SIGW(\_\_Vtemp52,95,0,3);

VL\_SIGW(\_\_Vtemp54,95,0,3);

VL\_SIGW(\_\_Vtemp56,95,0,3);

VL\_SIGW(\_\_Vtemp58,95,0,3);

VL\_SIGW(\_\_Vtemp61,95,0,3);

VL\_SIGW(\_\_Vtemp64,95,0,3);

VL\_SIGW(\_\_Vtemp66,95,0,3);

VL\_SIGW(\_\_Vtemp68,95,0,3);

VL\_SIGW(\_\_Vtemp70,95,0,3);

VL\_SIGW(\_\_Vtemp72,95,0,3);

VL\_SIGW(\_\_Vtemp74,95,0,3);

VL\_SIGW(\_\_Vtemp76,95,0,3);

VL\_SIGW(\_\_Vtemp78,95,0,3);

VL\_SIGW(\_\_Vtemp80,95,0,3);

VL\_SIGW(\_\_Vtemp82,95,0,3);

VL\_SIGW(\_\_Vtemp84,95,0,3);

VL\_SIGW(\_\_Vtemp86,95,0,3);

VL\_SIGW(\_\_Vtemp88,95,0,3);

VL\_SIGW(\_\_Vtemp90,95,0,3);

VL\_SIGW(\_\_Vtemp92,95,0,3);

VL\_SIGW(\_\_Vtemp103,95,0,3);

VL\_SIGW(\_\_Vtemp113,95,0,3);

VL\_SIGW(\_\_Vtemp123,95,0,3);

VL\_SIGW(\_\_Vtemp136,255,0,8);

VL\_SIGW(\_\_Vtemp138,255,0,8);

// Body

VL\_ASSIGN\_SII(4,vlTOPp->dmem\_hprot, 0U);

VL\_ASSIGN\_SII(1,vlTOPp->dmem\_hmastlock, 0U);

VL\_ASSIGN\_SII(32,vlTOPp->imem\_hwdata, 0U);

VL\_ASSIGN\_SII(4,vlTOPp->imem\_hprot, 0U);

VL\_ASSIGN\_SII(1,vlTOPp->imem\_hmastlock, 0U);

VL\_ASSIGN\_SII(3,vlTOPp->imem\_hburst, 0U);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_imem\_hresp, vlTOPp->imem\_hresp);

VL\_ASSIGN\_ISI(32,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata, vlTOPp->dmem\_hrdata);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dbg\_fullreset, vlTOPp->dbg\_fullreset);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dbg\_ndreset, vlTOPp->dbg\_ndreset);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hresp, vlTOPp->dmem\_hresp);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_clk, vlTOPp->clk);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_imem\_hready, vlTOPp->imem\_hready);

// ALWAYS at ../../src/verilog/core/sisc32\_csr\_file.v:190

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_next\_sup\_state

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_sup\_state;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_a\_geq

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_a

>= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_b);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_partialA

= (3U & (IData)((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_a

>> (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_counter)

<< 1U)))));

// ALWAYS at ../../src/verilog/core/sisc32\_mul\_div.v:80

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_b

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_b;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_a

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_a;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_t[1U]

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_a;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_Vfuncout

= ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_Vfuncout))

| ((vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_t

[1U] >= (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_b

<< 1U)) << 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_t[0U]

= (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_t

[1U] - ((QData)((IData)((1U & ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_Vfuncout)

>> 1U))))

\* (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_b

<< 1U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_Vfuncout

= ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_Vfuncout))

| (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_t

[0U] >= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_partialQ

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_cal\_partialQ\_\_5\_\_Vfuncout;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result\_muxed

= ((2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_out\_sel))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_a

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result);

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_word\_WB

= ((9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_pe))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_c)

: 0U));

// ALWAYS at ../../src/verilog/core/msb1.v:11

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x3fU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x5fU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

if ((0U != (0xffffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_ext\_interrupts\_st

>> 0x10U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x10U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_16

= (0xffffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_ext\_interrupts\_st

>> 0x10U));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x6fU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_16

= (0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_ext\_interrupts\_st);

}

if ((0U != (0xffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_16)

>> 8U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (8U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_8

= (0xffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_16)

>> 8U));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x77U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_8

= (0xffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_16));

}

if ((0U != (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_8)

>> 4U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_4

= (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_8)

>> 4U));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x7bU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_4

= (0xfU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_8));

}

if ((0U != (3U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_4)

>> 2U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_2

= (3U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_4)

>> 2U));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= (0x7dU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_2

= (3U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_4));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1

= ((0x7eU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1))

| (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_u\_msb1\_\_DOT\_\_int\_2)

>> 1U)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rs\_self = (1U & (

((((3U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (5U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (7U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (1U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? 0U

:

(((4U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (6U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? 1U

:

(((8U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (2U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? 1U

: 0U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mcause

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mint)

<< 0x1fU) | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mecode));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_single\_WB

= ((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt\_hit

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt)

== ((IData)(1U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_acnt\_max)));

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dbg\_irq, vlTOPp->dbg\_irq);

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hready, vlTOPp->dmem\_hready);

// ALWAYS at ../../src/verilog/core/sisc32\_pipeline.v:548

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_mem\_type

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dmem\_type\_WB;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_WB;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_Vfuncout

= ((0U == (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_mem\_type))

? ((0xff000000U & (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data

<< 0x18U)) | ((0xff0000U

& (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data

<< 0x10U))

| ((0xff00U

& (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data

<< 8U))

| (0xffU

& vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data))))

: ((1U == (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_mem\_type))

? ((0xffff0000U & (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data

<< 0x10U)) | (0xffffU

& vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data))

: vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_data));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wdata\_delayed

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_2\_\_Vfuncout;

// ALWAYS at ../../src/verilog/core/sisc32\_pipeline.v:526

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_data\_WB

= ((2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_wb\_src\_sel\_WB))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata\_WB

: ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_wb\_src\_sel\_WB))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result)

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_out\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_load\_in\_WB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_WB)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_store\_in\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rda

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_r\_griu\_res)

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_r\_friu\_res)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_rda\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw\_WB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_ldmw\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_stmw\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_byp\_alu\_WB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_WB)

& (0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_im5\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_alu\_WB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_WB)

& (0xfU != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_im5\_WB)));

VL\_ASSIGN\_ISI(24,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_ext\_interrupts, vlTOPp->ext\_interrupts);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_step\_window

= (1U & ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr

>> 2U) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_debug))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_a

= ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_pe))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_a

: 0U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_pe))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_b)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_a

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_pe))

? (0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_a)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd

= (7U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_WB)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_im5\_WB)

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_fcsr

>> 8U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_pe))

? (0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_a)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_a

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_pe))

? (0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_a)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_b

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_pe))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_b)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_oe

= ((7U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_oe

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b

= ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_pe))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_b)

: 0x3c00U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a

= (0xffffU & ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_pe))

? (0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_a)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mip

= ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_ext\_interrupts\_st

<< 8U) | ((0xffffff80U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtip)

<< 7U) & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mie))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msip)

<< 3U)));

VL\_ASSIGN\_ISI(32,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_imem\_hrdata, vlTOPp->imem\_hrdata);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_epc\_hit

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mepc

== vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX);

// ALWAYS at ../../src/verilog/core/sisc32\_ctrl.v:446

vlTOPp->\_\_Vtableidx2 = (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_op

= vlTOPp->\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_op

[vlTOPp->\_\_Vtableidx2];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_1\_signed

= vlTOPp->\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_1\_signed

[vlTOPp->\_\_Vtableidx2];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_2\_signed

= vlTOPp->\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_2\_signed

[vlTOPp->\_\_Vtableidx2];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_out\_sel

= vlTOPp->\_\_Vtable2\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_out\_sel

[vlTOPp->\_\_Vtableidx2];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dpc\_hit

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dpc

== vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX);

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked = ((0xffe0U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU))

| (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U)));

// ALWAYS at ../../src/verilog/core/sisc32\_ctrl.v:487

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_alu\_op\_arith

= (((((((((0U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))) | (1U ==

(7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))))

| (2U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) | (3U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))))

| (4U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) | (5U ==

(7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))))

| (6U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) | (7U == (7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))))

? ((0U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))) ? (((0x33U

== (0x7fU

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1eU))

? 0xaU : 0U)

: ((1U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))) ? 1U :

((2U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))) ? 0xcU

: ((3U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))) ? 0xeU

: ((4U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

? 4U : ((5U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

? ((0x40000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)

? 0xbU : 5U)

: ((6U == (7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

? 6U : 7U)))))))

: 0U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop

= ((0x18U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x16U)) | (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)));

VL\_ASSIGN\_ISI(1,vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_sup\_reset, vlTOPp->sup\_reset);

// ALWAYS at ../../src/verilog/core/sisc32\_pipeline.v:535

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_mem\_type

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dmem\_type\_WB;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_data

= vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_addr

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_out\_WB;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data

= (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_data

>> (0x18U & (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_addr

<< 3U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_b\_extend

= (0xffffff00U & (VL\_NEGATE\_I((IData)((1U &

(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data

>> 7U))))

<< 8U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_h\_extend

= (0xffff0000U & (VL\_NEGATE\_I((IData)((1U &

(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data

>> 0xfU))))

<< 0x10U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_Vfuncout

= ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_mem\_type))

? ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_mem\_type))

? vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data

: ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_mem\_type))

? (0xffffU & vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data)

: (0xffU & vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data)))

: ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_mem\_type))

? vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data

: ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_mem\_type))

? ((0xffffU & vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data)

| vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_h\_extend)

: ((0xffU & vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_shifted\_data)

| vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_b\_extend))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_WB

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_\_0\_\_Vfuncout;

// ALWAYS at ../../src/verilog/core/sisc32\_ctrl.v:643

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_code\_WB

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_prev\_ex\_code\_WB;

if ((1U & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_had\_ex\_WB)))) {

if (vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hresp) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_code\_WB

= (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_WB)

? 4U : 6U));

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_had\_ex\_WB)

| (IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hresp));

vlTOPp->sisc32\_core\_\_DOT\_\_imem\_bridge\_\_DOT\_\_m\_htrans

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_imem\_bridge\_\_DOT\_\_hold\_bus)

? 0U : ((IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_imem\_hready)

? 2U : 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_ibuf\_wait = (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_imem\_bridge\_\_DOT\_\_hold\_bus)

| (~ (IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_imem\_hready))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_partialP

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_b

\* (QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_partialA)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result\_muxed\_negated

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_negate\_output)

? VL\_NEGATE\_Q(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result\_muxed)

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result\_muxed);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_handler\_PC

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtvec

+ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_msb1)

<< 2U));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await = ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt\_hit)));

// ALWAYS at ../../src/verilog/core/sisc32\_csr\_file.v:403

if ((0x80000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x40000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x20000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x10000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x8000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtime\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

}

}

}

}

}

}

} else {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

}

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtime\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0x100100U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

} else {

if ((0x10000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x8000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_instret\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_time\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_cycle\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

} else {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_instret\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_time\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_cycle\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

}

}

}

} else {

if ((0x20000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x10000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x8000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_instret\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_time\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_cycle\_full

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

} else {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_instret\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_time\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_cycle\_full);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

}

}

} else {

if ((0x40000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x20000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x10000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x8000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_intcfg;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_dscratch;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dpc;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

=

(0x40000000U

| (((IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dbg\_ndreset)

<< 0x1dU)

| (((IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dbg\_fullreset)

<< 0x1cU)

| ((0x8000U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr)

| ((0x2000U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr)

| ((0x1000U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_dcsr\_cause)

<< 6U)

| (((IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dbg\_irq)

<< 5U)

| ((8U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr)

| ((4U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr)

| (3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_tdata1;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_from\_host;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_to\_host;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

} else {

if ((0x20000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x10000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x8000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mip\_status;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mbadaddr;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mcause;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mepc;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mscratch;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtimecmp;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

}

}

}

}

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtvec;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mie;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0x40801100U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

}

}

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

} else {

if ((0x10000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x8000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x4000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x2000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x1000000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

} else {

if ((0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_fcsr;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined = 0U;

}

}

}

}

}

}

}

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_cmd\_done

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt\_hit)

& (IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hready));

// ALWAYS at ../../src/verilog/core/sisc\_i2f.v:211

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_a;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_LZ = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_EXP = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_STK = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

= ((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? ((0x80000000U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai)

? ((IData)(1U) + (~ vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai)

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg

= ((0x7fffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg))

| (0x8000U & (((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

<< 0xfU) & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai

>> 0x10U))));

if ((0U == vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= (1U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg = 0U;

} else {

if (((0U != (0xffffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0x10U))) | (0xfffU

== (0xfffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 4U))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= (0x10U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg

= (0x7c00U | (0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= (0x20U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg));

} else {

if ((((0xffU == (0xffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 8U))) & (0xd1U

<=

(0xffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2)))

& (0xefU >= (0xffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= (0x10U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg

= (0x7bffU | (0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= (0x20U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg));

} else {

// Function: rnd\_eval at ../../src/verilog/core/sisc\_i2f.v:346

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai1

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_LZ1 = 0U;

while ((1U & (~ (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai1

>> 0x1fU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai1

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai1

<< 1U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_LZ1

= ((IData)(1U) + vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_LZ1);

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai3

= ((0U == (0x7fffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 1U))) ?

(0x80000000U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x1fU)) :

((0U == (0x3fffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 2U)))

? (0xc0000000U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x1eU))

: ((0U == (0x1fffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 3U)))

? (0xe0000000U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x1dU))

: ((0U == (0xfffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 4U)))

? (0xf0000000U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x1cU))

: ((0U == (0x7ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 5U)))

? (0xf8000000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x1bU))

: ((0U == (0x3ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 6U)))

? (0xfc000000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x1aU))

: ((0U ==

(0x1ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 7U)))

? (0xfe000000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x19U))

: ((0U

==

(0xffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 8U)))

?

(0xff000000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x18U))

:

((0U

==

(0x7fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 9U)))

?

(0xff800000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x17U))

:

((0U

==

(0x3fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xaU)))

?

(0xffc00000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x16U))

:

((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xbU)))

?

(0xffe00000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x15U))

:

((0U

==

(0xfU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xcU)))

?

(0xfff00000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x14U))

:

((0U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xdU)))

?

(0xfff80000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x13U))

:

((0U

==

(3U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xeU)))

?

(0xfffc0000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x12U))

:

((0x8000U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2)

?

(0xffff0000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x10U))

:

(0xfffe0000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

<< 0x11U)))))))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_LZ

= ((0U == (0x7fffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 1U))) ? 0xfU

: ((0U == (0x3fffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 2U)))

? 0xeU : ((0U == (0x1fffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 3U)))

? 0xdU : ((0U

==

(0xfffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 4U)))

? 0xcU

:

((0U

==

(0x7ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 5U)))

? 0xbU

:

((0U

==

(0x3ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 6U)))

? 0xaU

:

((0U

==

(0x1ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 7U)))

? 9U

:

((0U

==

(0xffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 8U)))

? 8U

:

((0U

==

(0x7fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 9U)))

? 7U

:

((0U

==

(0x3fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xaU)))

? 6U

:

((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xbU)))

? 5U

:

((0U

==

(0xfU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xcU)))

? 4U

:

((0U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xdU)))

? 3U

:

((0U

==

(3U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2

>> 0xeU)))

? 2U

:

((0x8000U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai2)

? 0U

: 1U)))))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_EXP

= (0x3fU & ((IData)(0xfU) + ((IData)(0xfU)

- vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_LZ)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf

= ((0x2001U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf))

| (0x1ffeU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai3

>> 0x13U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_STK

= (0U != (0xfffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Ai3));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf

= ((0x3ffeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_STK));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_stk

= (1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf)

>> 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_L

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf)

>> 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg)

>> 0xfU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xdU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| (((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_stk))

<< 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

if ((VL\_ULL(0) < VL\_TIME\_Q())) {

if ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd))) {

if (VL\_UNLIKELY((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd)))) {

VL\_WRITEF("Error! illegal rounding mode.\n\n");

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

VL\_WRITEF("a : %b\n",32,

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_a);

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

VL\_WRITEF("rnd : %b\n",

3,vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd);

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_stk)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (8U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

}

}

} else {

if ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd))) {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign)

<< 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign)

<< 3U));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign))

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| (4U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign))

<< 2U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| (8U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Sign))

<< 3U)));

}

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_R)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_L)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout));

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_val

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_eval\_\_6\_\_Vfuncout;

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_val))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf

= (0x3fffU & ((IData)(4U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf)));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg

= ((0xdfU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_status\_reg))

| (0x20U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_rnd\_val)

<< 4U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf2

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf;

if ((0x2000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_EXP

= (0x3fU & ((IData)(1U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_EXP)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf2

= (0x1fffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf)

>> 1U));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg

= ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_z\_reg))

| ((0x7c00U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_EXP)

<< 0xaU)) | (0x3ffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_\_DOT\_\_Mf)

>> 2U))));

}

}

}

// ALWAYS at ../../src/verilog/core/sisc\_f2i.v:214

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_a;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[0U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U] = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_stk = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_num = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_sig

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_inf\_input

= ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_sig)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_nan\_input

= ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_sig)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_denorm\_input

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_sig)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_zero\_input

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_sig)));

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_inf\_input) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_nan\_input) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_zero\_input) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (1U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

= (2U | vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]

= ((0x7fffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])

| (0xff800000U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af)

<< 0x17U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

= ((0xfffffffeU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U])

| (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af)

>> 9U)));

if ((1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf)

>> 4U) | (0xfU == (0xfU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf)))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf)

- (IData)(0xfU)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[1U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[2U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp;

while ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1))) {

if ((1U & (~ (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[2U]

>> 1U)))) {

VL\_SHIFTL\_WWI(66,66,32, \_\_Vtemp9, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1, 1U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U]

= \_\_Vtemp9[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[1U]

= \_\_Vtemp9[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[2U]

= (3U & \_\_Vtemp9[2U]);

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1)

- (IData)(1U)));

}

\_\_Vtemp32[1U] = (((2U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (3U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U])))

? ((3U & ((IData)(

(((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x1eU))

| (0xfffffffcU

& ((IData)(

((((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

>> 0x20U))

<< 2U)))

: (((1U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (~ (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

>> 1U)))

? ((1U &

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]

>> 0x1fU))

| (0xfffffffeU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

<< 1U)))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]));

\_\_Vtemp34[0U] = (((3U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (7U

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 1U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1fU)))))

? (0xfffffff8U

& ((IData)(

(VL\_ULL(0x7fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 3U))

: (((2U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(3U &

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U])))

? (0xfffffffcU

& ((IData)(

(((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

<< 2U))

: (((1U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (~

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

>> 1U)))

? (0xfffffffeU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]

<< 1U))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])));

\_\_Vtemp34[2U] = (((3U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (7U

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 1U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1fU)))))

? (7U & ((IData)(

((VL\_ULL(0x7fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x1dU))

: (((2U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(3U &

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U])))

? (3U & ((IData)(

((((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

>> 0x20U))

>> 0x1eU))

: (((1U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (~

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

>> 1U)))

? ((1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1fU))

| (2U

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 1U)))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U])));

\_\_Vtemp36[1U] = (((4U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0xfU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 2U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1eU)))))

? ((0xfU & ((IData)(

(VL\_ULL(0x3fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x1cU))

| (0xfffffff0U

& ((IData)(

((VL\_ULL(0x3fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 4U)))

: (((3U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(7U &

((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 1U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1fU)))))

? ((7U &

((IData)(

(VL\_ULL(0x7fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x1dU))

| (0xfffffff8U

& ((IData)(

((VL\_ULL(0x7fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 3U)))

: \_\_Vtemp32[1U]));

\_\_Vtemp38[0U] = (((5U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x1fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 3U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1dU)))))

? (0xffffffe0U

& ((IData)(

(VL\_ULL(0x1fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 5U))

: (((4U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0xfU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 2U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1eU)))))

? (0xfffffff0U

& ((IData)(

(VL\_ULL(0x3fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 4U))

: \_\_Vtemp34[0U]));

\_\_Vtemp38[2U] = (((5U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x1fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 3U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1dU)))))

? (0x1fU & ((IData)(

((VL\_ULL(0x1fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x1bU))

: (((4U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0xfU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 2U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1eU)))))

? (0xfU &

((IData)(

((VL\_ULL(0x3fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x1cU))

: \_\_Vtemp34[2U]));

\_\_Vtemp40[1U] = (((6U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x3fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 4U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1cU)))))

? ((0x3fU & ((IData)(

(VL\_ULL(0xfffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x1aU))

| (0xffffffc0U

& ((IData)(

((VL\_ULL(0xfffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 6U)))

: (((5U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x1fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 3U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1dU)))))

? ((0x1fU

& ((IData)(

(VL\_ULL(0x1fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x1bU))

| (0xffffffe0U

& ((IData)(

((VL\_ULL(0x1fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 5U)))

: \_\_Vtemp36[1U]));

\_\_Vtemp42[0U] = (((7U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 5U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1bU)))))

? (0xffffff80U

& ((IData)(

(VL\_ULL(0x7ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 7U))

: (((6U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x3fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 4U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1cU)))))

? (0xffffffc0U

& ((IData)(

(VL\_ULL(0xfffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 6U))

: \_\_Vtemp38[0U]));

\_\_Vtemp42[2U] = (((7U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 5U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1bU)))))

? (0x7fU & ((IData)(

((VL\_ULL(0x7ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x19U))

: (((6U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x3fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 4U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1cU)))))

? (0x3fU

& ((IData)(

((VL\_ULL(0xfffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x1aU))

: \_\_Vtemp38[2U]));

\_\_Vtemp44[1U] = (((8U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0xffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 6U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1aU)))))

? ((0xffU & ((IData)(

(VL\_ULL(0x3ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x18U))

| (0xffffff00U

& ((IData)(

((VL\_ULL(0x3ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 8U)))

: (((7U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x7fU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 5U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1bU)))))

? ((0x7fU

& ((IData)(

(VL\_ULL(0x7ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x19U))

| (0xffffff80U

& ((IData)(

((VL\_ULL(0x7ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 7U)))

: \_\_Vtemp40[1U]));

\_\_Vtemp46[0U] = (((9U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x1ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 7U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x19U)))))

? (0xfffffe00U

& ((IData)(

(VL\_ULL(0x1ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 9U))

: (((8U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0xffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 6U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1aU)))))

? (0xffffff00U

& ((IData)(

(VL\_ULL(0x3ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 8U))

: \_\_Vtemp42[0U]));

\_\_Vtemp46[2U] = (((9U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x1ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 7U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x19U)))))

? (0x1ffU & ((IData)(

((VL\_ULL(0x1ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x17U))

: (((8U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0xffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 6U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x1aU)))))

? (0xffU

& ((IData)(

((VL\_ULL(0x3ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x18U))

: \_\_Vtemp42[2U]));

\_\_Vtemp48[1U] = (((0xaU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x3ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 8U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x18U)))))

? ((0x3ffU &

((IData)(

(VL\_ULL(0xffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x16U))

| (0xfffffc00U

& ((IData)(

((VL\_ULL(0xffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 0xaU)))

: (((9U <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x1ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 7U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x19U)))))

? ((0x1ffU

& ((IData)(

(VL\_ULL(0x1ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x17U))

| (0xfffffe00U

& ((IData)(

((VL\_ULL(0x1ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 9U)))

: \_\_Vtemp44[1U]));

\_\_Vtemp50[0U] = (((0xbU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 9U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x17U)))))

? (0xfffff800U

& ((IData)(

(VL\_ULL(0x7fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 0xbU))

: (((0xaU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x3ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 8U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x18U)))))

? (0xfffffc00U

& ((IData)(

(VL\_ULL(0xffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 0xaU))

: \_\_Vtemp46[0U]));

\_\_Vtemp50[2U] = (((0xbU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 9U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x17U)))))

? (0x7ffU & ((IData)(

((VL\_ULL(0x7fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x15U))

: (((0xaU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x3ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 8U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x18U)))))

? (0x3ffU

& ((IData)(

((VL\_ULL(0xffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x16U))

: \_\_Vtemp46[2U]));

\_\_Vtemp52[1U] = (((0xcU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0xfffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xaU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x16U)))))

? ((0xfffU &

((IData)(

(VL\_ULL(0x3fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x14U))

| (0xfffff000U

& ((IData)(

((VL\_ULL(0x3fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 0xcU)))

: (((0xbU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x7ffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 9U)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x17U)))))

? ((0x7ffU

& ((IData)(

(VL\_ULL(0x7fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x15U))

| (0xfffff800U

& ((IData)(

((VL\_ULL(0x7fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 0xbU)))

: \_\_Vtemp48[1U]));

\_\_Vtemp54[0U] = (((0xdU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x1fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xbU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x15U)))))

? (0xffffe000U

& ((IData)(

(VL\_ULL(0x1fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 0xdU))

: (((0xcU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0xfffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xaU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x16U)))))

? (0xfffff000U

& ((IData)(

(VL\_ULL(0x3fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 0xcU))

: \_\_Vtemp50[0U]));

\_\_Vtemp54[2U] = (((0xdU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x1fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xbU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x15U)))))

? (0x1fffU &

((IData)((

(VL\_ULL(0x1fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x13U))

: (((0xcU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0xfffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xaU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x16U)))))

? (0xfffU

& ((IData)(

((VL\_ULL(0x3fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x14U))

: \_\_Vtemp50[2U]));

\_\_Vtemp56[1U] = (((0xeU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x3fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xcU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x14U)))))

? ((0x3fffU &

((IData)(

(VL\_ULL(0xfffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x12U))

| (0xffffc000U

& ((IData)(

((VL\_ULL(0xfffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 0xeU)))

: (((0xdU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x1fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xbU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x15U)))))

? ((0x1fffU

& ((IData)(

(VL\_ULL(0x1fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x13U))

| (0xffffe000U

& ((IData)(

((VL\_ULL(0x1fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 0xdU)))

: \_\_Vtemp52[1U]));

\_\_Vtemp58[0U] = (((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xdU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x13U)))))

? (0xffff8000U

& ((IData)(

(VL\_ULL(0x7ffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 0xfU))

: (((0xeU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x3fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xcU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x14U)))))

? (0xffffc000U

& ((IData)(

(VL\_ULL(0xfffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

<< 0xeU))

: \_\_Vtemp54[0U]));

\_\_Vtemp58[2U] = (((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xdU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x13U)))))

? (0x7fffU &

((IData)((

(VL\_ULL(0x7ffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x11U))

: (((0xeU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U ==

(0x3fffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xcU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x14U)))))

? (0x3fffU

& ((IData)(

((VL\_ULL(0xfffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

>> 0x12U))

: \_\_Vtemp54[2U]));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U]

= \_\_Vtemp58[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]

= (((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

& (0U == (0x7fffU & ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]

<< 0xdU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]

>> 0x13U)))))

? ((0x7fffU & ((IData)(

(VL\_ULL(0x7ffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))))

>> 0x11U))

| (0xffff8000U & ((IData)(

((VL\_ULL(0x7ffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))))

>> 0x20U))

<< 0xfU)))

: \_\_Vtemp56[1U]);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U]

= \_\_Vtemp58[2U];

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp

= (0x1fU & ((IData)(0xfU) - (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_eaf)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[1U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[2U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp;

while ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_stk

= (1U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U]);

VL\_SHIFTR\_WWI(66,66,32, \_\_Vtemp61, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1, 1U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U]

= \_\_Vtemp61[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[1U]

= \_\_Vtemp61[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[2U]

= (3U & \_\_Vtemp61[2U]);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U]

= ((0xfffffffeU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U])

| (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_stk)

| vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi1[0U])));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp1)

- (IData)(1U)));

}

VL\_EXTEND\_WQ(65,50, \_\_Vtemp64,

(VL\_ULL(0x3ffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x30U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x10U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0x10U)))));

VL\_EXTEND\_WQ(65,51, \_\_Vtemp66,

(VL\_ULL(0x7ffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x31U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x11U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0xfU)))));

VL\_EXTEND\_WQ(65,52, \_\_Vtemp68,

(VL\_ULL(0xfffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x32U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x12U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0xeU)))));

VL\_EXTEND\_WQ(65,53, \_\_Vtemp70,

(VL\_ULL(0x1fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x33U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x13U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0xdU)))));

VL\_EXTEND\_WQ(65,54, \_\_Vtemp72,

(VL\_ULL(0x3fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x34U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x14U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0xcU)))));

VL\_EXTEND\_WQ(65,55, \_\_Vtemp74,

(VL\_ULL(0x7fffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x35U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x15U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0xbU)))));

VL\_EXTEND\_WQ(65,56, \_\_Vtemp76,

(VL\_ULL(0xffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x36U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x16U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 0xaU)))));

VL\_EXTEND\_WQ(65,57, \_\_Vtemp78,

(VL\_ULL(0x1ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x37U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x17U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 9U)))));

VL\_EXTEND\_WQ(65,58, \_\_Vtemp80,

(VL\_ULL(0x3ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x38U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x18U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 8U)))));

VL\_EXTEND\_WQ(65,59, \_\_Vtemp82,

(VL\_ULL(0x7ffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x39U) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x19U)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 7U)))));

VL\_EXTEND\_WQ(65,60, \_\_Vtemp84,

(VL\_ULL(0xfffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x3aU) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x1aU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 6U)))));

VL\_EXTEND\_WQ(65,61, \_\_Vtemp86,

(VL\_ULL(0x1fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x3bU) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x1bU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 5U)))));

VL\_EXTEND\_WQ(65,62, \_\_Vtemp88,

(VL\_ULL(0x3fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x3cU) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x1cU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 4U)))));

VL\_EXTEND\_WQ(65,63, \_\_Vtemp90,

(VL\_ULL(0x7fffffffffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x3dU) | (

((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x1dU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 3U)))));

VL\_EXTEND\_WQ(65,64, \_\_Vtemp92,

(((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U]))

<< 0x3eU) | (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U]))

<< 0x1eU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U]))

>> 2U))));

\_\_Vtemp103[0U] = ((5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp84[0U]

<< 1U))

| (0U !=

(0x3fU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp86[0U]

<< 1U))

| (0U

!=

(0x1fU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp88[0U]

<< 1U))

| (0U

!=

(0xfU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((2U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((0xfffffffeU

& (\_\_Vtemp90[0U]

<< 1U))

| (0U

!=

(7U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

:

((1U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((0xfffffffeU

& (\_\_Vtemp92[0U]

<< 1U))

| (0U

!=

(3U

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

:

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))));

\_\_Vtemp103[1U] = ((5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U & (\_\_Vtemp84[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp84[1U]

<< 1U)))

: ((4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U &

(\_\_Vtemp86[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp86[1U]

<< 1U)))

: ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U

& (\_\_Vtemp88[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp88[1U]

<< 1U)))

: ((2U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp90[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp90[1U]

<< 1U)))

:

((1U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp92[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp92[1U]

<< 1U)))

:

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[1U])))));

\_\_Vtemp103[2U] = ((5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U & (\_\_Vtemp84[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp84[2U]

<< 1U)))

: ((4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U &

(\_\_Vtemp86[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp86[2U]

<< 1U)))

: ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U

& (\_\_Vtemp88[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp88[2U]

<< 1U)))

: ((2U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp90[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp90[2U]

<< 1U)))

:

((1U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp92[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp92[2U]

<< 1U)))

:

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[2U])))));

\_\_Vtemp113[0U] = ((0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp74[0U]

<< 1U))

| (0U !=

(0x7ffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp76[0U]

<< 1U))

| (0U

!=

(0x3ffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp78[0U]

<< 1U))

| (0U

!=

(0x1ffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((7U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((0xfffffffeU

& (\_\_Vtemp80[0U]

<< 1U))

| (0U

!=

(0xffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

:

((6U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((0xfffffffeU

& (\_\_Vtemp82[0U]

<< 1U))

| (0U

!=

(0x7fU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

:

\_\_Vtemp103[0U])))));

\_\_Vtemp113[1U] = ((0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U & (\_\_Vtemp74[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp74[1U]

<< 1U)))

: ((9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U &

(\_\_Vtemp76[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp76[1U]

<< 1U)))

: ((8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U

& (\_\_Vtemp78[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp78[1U]

<< 1U)))

: ((7U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp80[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp80[1U]

<< 1U)))

:

((6U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp82[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp82[1U]

<< 1U)))

:

\_\_Vtemp103[1U])))));

\_\_Vtemp113[2U] = ((0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U & (\_\_Vtemp74[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp74[2U]

<< 1U)))

: ((9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U &

(\_\_Vtemp76[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp76[2U]

<< 1U)))

: ((8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U

& (\_\_Vtemp78[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp78[2U]

<< 1U)))

: ((7U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp80[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp80[2U]

<< 1U)))

:

((6U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp82[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp82[2U]

<< 1U)))

:

\_\_Vtemp103[2U])))));

\_\_Vtemp123[0U] = ((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp64[0U]

<< 1U))

| (0U !=

(0xffffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((0xeU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp66[0U]

<< 1U))

| (0U

!=

(0x7fffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((0xdU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((0xfffffffeU

& (\_\_Vtemp68[0U]

<< 1U))

| (0U

!=

(0x3fffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

: ((0xcU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((0xfffffffeU

& (\_\_Vtemp70[0U]

<< 1U))

| (0U

!=

(0x1fffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

:

((0xbU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((0xfffffffeU

& (\_\_Vtemp72[0U]

<< 1U))

| (0U

!=

(0xfffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi[0U])))

:

\_\_Vtemp113[0U])))));

\_\_Vtemp123[1U] = ((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U & (\_\_Vtemp64[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp64[1U]

<< 1U)))

: ((0xeU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U &

(\_\_Vtemp66[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp66[1U]

<< 1U)))

: ((0xdU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U

& (\_\_Vtemp68[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp68[1U]

<< 1U)))

: ((0xcU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp70[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp70[1U]

<< 1U)))

:

((0xbU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp72[0U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp72[1U]

<< 1U)))

:

\_\_Vtemp113[1U])))));

\_\_Vtemp123[2U] = ((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U & (\_\_Vtemp64[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp64[2U]

<< 1U)))

: ((0xeU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U &

(\_\_Vtemp66[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp66[2U]

<< 1U)))

: ((0xdU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

? ((1U

& (\_\_Vtemp68[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp68[2U]

<< 1U)))

: ((0xcU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp70[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp70[2U]

<< 1U)))

:

((0xbU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_exp))

?

((1U

& (\_\_Vtemp72[1U]

>> 0x1fU))

| (0xfffffffeU

& (\_\_Vtemp72[2U]

<< 1U)))

:

\_\_Vtemp113[2U])))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U]

= \_\_Vtemp123[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]

= \_\_Vtemp123[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U]

= \_\_Vtemp123[2U];

}

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U])) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (0x40U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[0U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (0x20U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_stk

= (0U != vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U]);

// Function: rnd\_eval at ../../src/verilog/core/sisc\_f2i.v:333

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_num = 0x1fU;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U]

= ((0x7fffffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U])

| (0x80000000U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_stk)

<< 0x1fU)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_stk

= (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U]

>> 0x1fU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R

= (1U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]);

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_L

= (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]

>> 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af)

>> 0xfU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xdU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| (((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_stk))

<< 1U));

if ((VL\_ULL(0) < VL\_TIME\_Q())) {

if ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd))) {

if (VL\_UNLIKELY((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd)))) {

VL\_WRITEF("Error! illegal rounding mode.\n\n");

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

VL\_WRITEF("a : %b\n",

16,vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_a);

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

VL\_WRITEF("rnd : %b\n",

3,vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd);

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_stk)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (8U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

}

}

} else {

if ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd))) {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign)

<< 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign)

<< 3U));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign))

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| (4U &

((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign))

<< 2U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| (8U &

((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Sign))

<< 3U)));

}

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_R)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_L)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout));

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_val

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_eval\_\_7\_\_Vfuncout;

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_val))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

= ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U])

| (0xfffffffeU & ((IData)(

(VL\_ULL(0x1ffffffff)

& (VL\_ULL(1)

+

(((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U]))

<< 0x1fU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]))

>> 1U)))))

<< 1U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

= ((1U & ((IData)((VL\_ULL(0x1ffffffff)

& (VL\_ULL(1)

+

(((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U]))

<< 0x1fU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]))

>> 1U)))))

>> 0x1fU)) |

(0xfffffffeU & ((IData)(

((VL\_ULL(0x1ffffffff)

& (VL\_ULL(1)

+

(((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U]))

<< 0x1fU)

| ((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]))

>> 1U))))

>> 0x20U))

<< 1U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[0U]

= (IData)((VL\_ULL(0x1ffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U])))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

= ((0xfffffffeU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U])

| (IData)(((VL\_ULL(0x1ffffffff)

& (((QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U]))

<< 0x20U)

| (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U]))))

>> 0x20U)));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[0U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[0U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[1U];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi2[2U];

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= ((0xdfU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg))

| (0x20U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_rnd\_val)

<< 4U))));

if ((0U == ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

<< 0x1fU) | (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

>> 1U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (1U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_denorm\_input) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (8U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

}

}

}

}

}

}

if ((1U & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af)

>> 0xfU) & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

& (0U != (0x7fffffffU

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

<< 0x1fU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

>> 1U))))))

| ((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af)

>> 0xfU)) & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U])))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (0x40U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg

= (0x20U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_z\_reg

= ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_af))

? ((1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg)

>> 6U) | ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg)

>> 2U))) ? 0x80000000U

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg))

? 0U : VL\_NEGATE\_I(((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

<< 0x1fU)

| (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

>> 1U)))))

: ((1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg)

>> 6U) | ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg)

>> 2U))) ? 0x7fffffffU

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_status\_reg))

? 0U : ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[2U]

<< 0x1fU) | (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_\_DOT\_\_mi3[1U]

>> 1U)))));

// ALWAYS at ../../src/verilog/core/sisc\_fcmp.v:118

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b = 0U;

if ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a

= (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ma

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ma

= (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)));

}

if ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b

= (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Mb

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Mb

= (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b)));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_sign

= (1U & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a)))

^ (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b)

>> 0xfU) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_aeqb\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_unordered\_int = 0U;

if ((((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)))

| ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_unordered\_int = 1U;

} else {

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))

& (0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb)))) {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_sign) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_aeqb\_int = 1U;

}

} else {

if ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

}

} else {

if ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

}

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_aeqb\_int = 1U;

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

}

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

}

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_sign) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

}

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea)

!= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))) {

if ((((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea)

> (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea)

< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

}

} else {

if ((((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)

> (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)

< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int = 1U;

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_aeqb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int = 1U;

}

}

}

}

}

}

}

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_chk

= (3U & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_agtb\_int)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_aeqb\_int))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_unordered\_int)));

if (VL\_UNLIKELY((1U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_chk)))) {

VL\_WRITEF("Error! agtb, aeqb, altb, and unordered are NOT mutually exclusive.\n");

}

if ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_altb\_int)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_aeqb\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_unordered\_int))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_z0\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_z1\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= (0x80U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int));

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_z0\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_b;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_z1\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a;

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Eb))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Ea))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status0\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_zer\_a));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int

= (0x80U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int));

}

// ALWAYS at ../../src/verilog/core/sisc\_fcmp.v:118

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b = 0U;

if ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a

= (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ma

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ma

= (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)));

}

if ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b

= (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Mb

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Mb

= (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c)));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_sign

= (1U & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a)))

^ (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c)

>> 0xfU) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_aeqb\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_unordered\_int = 0U;

if ((((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)))

| ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_unordered\_int = 1U;

} else {

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))

& (0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb)))) {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_sign) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_aeqb\_int = 1U;

}

} else {

if ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

}

} else {

if ((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

}

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_aeqb\_int = 1U;

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

}

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

}

} else {

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_sign) {

if ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

}

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea)

!= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))) {

if ((((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea)

> (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea)

< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

}

} else {

if ((((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)

> (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)

>> 0xfU)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)

< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int = 1U;

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_aeqb\_int = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int = 1U;

}

}

}

}

}

}

}

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_chk

= (3U & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_agtb\_int)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_aeqb\_int))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_unordered\_int)));

if (VL\_UNLIKELY((1U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_chk)))) {

VL\_WRITEF("Error! agtb, aeqb, altb, and unordered are NOT mutually exclusive.\n");

}

if ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_altb\_int)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_aeqb\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_unordered\_int))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_z0\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_z1\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= (0x80U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int));

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_z0\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_c;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_z1\_int

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a;

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Eb))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int));

}

if (((0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Ea))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_Fa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status0\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= ((0xfeU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_zer\_a));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int

= (0x80U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_swap

= ((0x7fffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_a))

< (0x7fffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_b)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_b\_int

= ((0x8000U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_op)

? (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_b)

>> 0xfU)) : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_b)

>> 0xfU))

<< 0xfU)) | (0x7fffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_b)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_z

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_oe)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_i2f\_z)

: ((6U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_f2i\_z

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_oe)

? (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_fadd\_z)

& VL\_NEGATE\_I((IData)((1U &

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_pe)

>> 2U)))))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r1\_fmul\_z)

& VL\_NEGATE\_I((IData)((1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe)

>> 2U))))))

: ((((2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

| (0xdU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r1\_fmul\_z)

: (((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (0xcU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

? (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_z\_reg)

& VL\_NEGATE\_I((IData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_req\_r2))))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r1\_fmul\_z)

& VL\_NEGATE\_I((IData)(

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe)

>> 2U))))))

: ((8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1z0)

: ((9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1z1)

: ((0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1altb)

: ((0xbU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1agtb)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1aeqb))

: ((0xeU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1aeqb)

: (

(4U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1altb)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u1z1)

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u2agtb)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_u2z0)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_a)))

: 0U)))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_int\_rdy

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_oe)

? (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_i2f\_pe)

>> 1U)) : ((6U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

? (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_f2i\_pe)

>> 1U))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_oe)

? (1U &

(((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_pe)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe))

>> 2U))

: ((((2U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (5U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

| (0xdU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

? (1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe)

>> 2U))

: ((

(3U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (0xcU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_req\_r2)

| (1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe)

>> 2U)))

:

(((((((8U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op))

| (9U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

| (0xaU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

| (0xbU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

| (4U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

| (0xeU

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

?

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_pe)

>> 1U))

: 0U)))))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_SUBNb

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 0xaU))) & (0U != (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_INFb

= ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 0xaU))) & (0U ==

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_ZEROb

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 0xaU))) & (0U == (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:302

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Sign

= (1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

^ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b))

>> 0xfU));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_SUBNa

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 0xaU))) & (0U != (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_INFa

= ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 0xaU))) & (0U ==

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_NaNa

= ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 0xaU))) & (0U !=

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:311

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_ZEROa

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 0xaU))) & (0U == (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[0U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mcause;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[1U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mip;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[2U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mie;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[3U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mepc;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[4U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mtvec;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[5U]

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mbadaddr;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[6U]

= (IData)((QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_fcsr)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[7U]

= (IData)(((QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_fcsr))

>> 0x20U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_minterrupt

= (0U != (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mie

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mip));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_step\_redirect

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dpc\_hit)

& ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_i\_dcsr

>> 2U) & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_debug)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_burst\_mark

= (0xfU & (((((((((((((((((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 1U)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 2U)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 3U))) +

(1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 4U))) + (1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 5U)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 6U))) + (1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 7U)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 8U))) + (1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 9U)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 0xaU))) + (1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 0xbU)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 0xcU))) + (1U &

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 0xdU)))

+ (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 0xeU))) + (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

>> 0xfU)))

- (IData)(1U)));

// ALWAYS at ../../src/verilog/core/sisc32\_ctrl.v:223

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ecall = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ebreak = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_eret\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dret\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_fence\_i = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs1 = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs2 = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md\_unkilled = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wfi\_unkilled\_DX = 0U;

if ((0x40U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x20U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x10U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 2U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX

= (0U != (7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)));

if ((0U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

if (((0U == (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

& (0U == (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U))))) {

if ((0x80000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((0x40000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x20000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x10000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x8000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x4000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x2000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x1000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dret\_unkilled = 1U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if (

(0x20000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x10000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x8000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x4000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x2000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x1000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_eret\_unkilled = 1U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if (

(0x10000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x8000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x4000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x2000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x1000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (

(0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wfi\_unkilled\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

if (

(0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_eret\_unkilled = 1U;

}

}

}

}

}

}

}

}

}

} else {

if (

(0x8000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x4000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x2000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x1000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x800000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x400000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x200000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if (

(0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ebreak = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ecall = 1U;

}

}

}

}

}

}

}

}

}

}

}

}

}

} else {

if ((1U == (7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled

= (7U &

((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

? 4U

: 5U));

} else {

if ((2U ==

(7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled

= (7U

& ((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

? 4U

: 6U));

} else {

if ((3U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled

=

(7U

& ((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

? 4U

: 7U));

} else {

if (

(5U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled

=

(7U

& ((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

? 4U

: 5U));

} else {

if (

(6U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled

=

(7U

& ((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

? 4U

: 6U));

} else {

if (

(7U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled

=

(7U

& ((0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)))

? 4U

: 7U));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

} else {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs1 = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel = 2U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction

= (0U != (7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel = 2U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs2 = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken\_unkilled

= (1U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_out);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel = 0U;

if ((0U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 8U;

} else {

if ((1U == (7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 9U;

} else {

if ((4U ==

(7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 0xcU;

} else {

if ((6U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 0xeU;

} else {

if (

(5U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 0xdU;

} else {

if (

(7U

==

(7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op = 0xfU;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

}

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

}

} else {

if ((0x10U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((3U != (3U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

if ((0x4000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 6U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 5U;

}

} else {

if ((0x4000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 0xaU;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 9U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

if ((0x20U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0x10U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs1 = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel = 2U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 2U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs2 = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_alu\_op\_arith;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

if ((1U == (0x7fU &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x19U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 3U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

} else {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((3U != (3U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

if ((0x4000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 4U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 3U;

}

} else {

if ((0x4000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 8U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 7U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs2 = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

}

} else {

if ((0x10U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs1 = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 2U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_alu\_op\_arith;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

} else {

if ((8U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((0U == (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

if ((1U & (~ ((

(0U

==

(0xfU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1cU)))

& (0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU))))

& (0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U))))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if ((1U == (7U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))) {

if ((((0U ==

(0xfffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U)))

& (0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU))))

& (0U

==

(0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_fence\_i = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if (((2U == (3U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x19U)))

& (7U == (7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 6U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 1U;

}

if (((3U == (3U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x19U)))

& (0U == (7U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 4U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type = 6U;

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type = 2U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

} else {

if ((4U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

} else {

if ((2U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

if ((1U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_DX = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wb\_src\_sel\_DX = 1U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction = 1U;

}

}

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (2U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (9U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (3U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (4U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (5U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (1U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (0U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (6U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (7U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_unkilled

= ((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)))

& (0U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)))

& (1U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)))

& (2U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)))

& (3U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)))

& (4U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub\_unkilled

= ((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul\_unkilled

= ((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv\_unkilled

= ((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat\_unkilled

= ((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (5U == (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop))))

& (8U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

VL\_ASSIGN\_SII(2,vlTOPp->imem\_htrans, vlTOPp->sisc32\_core\_\_DOT\_\_imem\_bridge\_\_DOT\_\_m\_htrans);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_final\_result

= ((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_out\_sel))

? (IData)((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result\_muxed\_negated

>> 0x20U)) : (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_result\_muxed\_negated));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_handler\_hit

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_handler\_PC

== vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX);

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait = (1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_in\_burst)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_cmd\_done)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt\_hit)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_in\_burst))

| (~ (IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hready)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp\_sta

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp1\_\_DOT\_\_status1\_int)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fcmp2\_\_DOT\_\_status1\_int));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_subtract

= (1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_a)

^ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_b\_int))

>> 0xfU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_swap)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_b\_int)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_a));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_swap)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_a)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_b\_int));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rdd

= ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_byp\_alu\_WB))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_wr\_data\_WB

: (((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvc\_WB))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_WB)

? ((0x8000U & ((~ (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_wr\_data\_WB

>> 0xfU)) << 0xfU))

| (0x7fffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_wr\_data\_WB))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_WB)

? (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_wr\_data\_WB

>> 0xfU)) : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_WB)

? (0x7fffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_wr\_data\_WB)

: (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvc\_sign\_WB)

<< 0xfU)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_im5\_WB)

<< 0xaU)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_rs2a\_WB)

<< 5U)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_rs1a\_WB)))))))

: ((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_alu\_WB))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_z

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_wr\_data\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a\_update

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_need\_scl)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_int\_rdy));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rdy

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_int\_rdy)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_need\_scl)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:337

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsNaN

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_NaNa)

| ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 0xaU))) & (0U

!=

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsAInfOrDivZ

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_INFa)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_ZEROb));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsAZorDivInf

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_ZEROa)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_INFb));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsInfDivInf

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_INFa)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_INFb));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsZDivZ

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_ZEROa)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_ZEROb));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsSpecInvalid

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsNaN)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsInfDivInf))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsZDivZ));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsValid

= (1U & (~ (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsSpecInvalid)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsAInfOrDivZ))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsAZorDivInf))));

\_\_Vtemp136[0U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[6U];

\_\_Vtemp136[1U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[1U];

\_\_Vtemp136[2U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[2U];

\_\_Vtemp136[3U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[3U];

\_\_Vtemp136[4U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[4U];

\_\_Vtemp136[5U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[5U];

\_\_Vtemp136[6U] = (IData)((((QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[7U]))

<< 0x20U) | (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[6U]))));

\_\_Vtemp136[7U] = (IData)(((((QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[7U]))

<< 0x20U) | (QData)((IData)(

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[6U])))

>> 0x20U));

VL\_ASSIGN\_SWW(256,vlTOPp->mon1, \_\_Vtemp136);

\_\_Vtemp138[0U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[0U];

\_\_Vtemp138[1U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[1U];

\_\_Vtemp138[2U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[2U];

\_\_Vtemp138[3U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[3U];

\_\_Vtemp138[4U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[4U];

\_\_Vtemp138[5U] = vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_mon\_csr[5U];

\_\_Vtemp138[6U] = (IData)((((QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

<< 0x20U) | (QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX))));

\_\_Vtemp138[7U] = (IData)(((((QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

<< 0x20U) | (QData)((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX)))

>> 0x20U));

VL\_ASSIGN\_SWW(256,vlTOPp->mon0, \_\_Vtemp138);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken

= ((((0U == (3U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U))) ? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_minterrupt)

: ((3U != (3U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U))) | ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_minterrupt))))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_mask)))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_step\_window)));

// ALWAYS at ../../src/verilog/core/sisc32\_imm\_gen.v:8

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm =

((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((0xfffff800U & (VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0xbU)) | (0x7ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U)))

: ((0xfffffe00U & (VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 9U)) | ((0x1e0U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x16U))

| (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U)))))

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((0xffff0000U & (VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1eU))))

<< 0x10U)) | (

(0xffe0U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU))

| (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U))))

: 0U)) : ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((0xfff00000U &

(VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0x14U)) |

((0xff000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)

| ((0x800U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 9U))

| ((0x7e0U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))

| (0x1eU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))))))

: (0xfffff000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm\_type))

? ((0xfffff800U &

(VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0xbU)) | (

(0x7e0U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))

| (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U))))

: ((0xfffff800U &

(VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0xbU)) | (0x7ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_sisc\_jump

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken\_unkilled));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_size =

(7U & (((((9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

| (9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? 2U : 1U));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_single

= ((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

| (2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_ldmw =

(((((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

| (3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (7U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_stmw =

(((((2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

| (4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (6U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_system\_wen

= (1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled)

>> 1U) | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_uses\_gprs1

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_unkilled));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_uses\_fprs1

= ((((((((((((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql\_unkilled));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_dvalid\_mix

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_single\_WB)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_in\_burst)

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt)))

& (IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hready)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wait = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_incr\_type\_WB)

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_wait\_d))

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large\_is\_zero

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU))) & (0U == (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large\_is\_INF

= ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU))) & (0U ==

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Denormal\_Large

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU))) & (0U != (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small\_is\_INF

= ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

>> 0xaU))) & (0U ==

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small\_is\_zero

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

>> 0xaU))) & (0U == (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_in\_is\_NaN

= (((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU))) & (0U !=

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))))

| ((0x1fU == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

>> 0xaU))) & (0U

!=

(0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Denormal\_Small

= ((0U == (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

>> 0xaU))) & (0U != (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_wd

= ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rda))

? (0xffff0000U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rdd

<< 0x10U)) : (0xffffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rdd));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_is\_scl

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a\_update)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_scl\_r)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_int\_rdy))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd

= ((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB))

| ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_alu\_WB))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rdy)))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_byp\_alu\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvc\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_w

= (1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_r\_u\_res)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_r\_griu\_res))

: ((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_alu\_WB))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rdy)

: 0U)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:352

if ((1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsValid)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_SUBNa)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fa\_rcvr

= ((0U == (0x1ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 1U))) ? (0x400U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 0xaU))

: ((0U == (0xffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 2U))) ? (0x600U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 9U))

: ((0U == (0x7fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 3U))) ?

(0x700U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 8U)) : ((0U ==

(0x3fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 4U)))

? (0x780U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 7U))

: ((0U

==

(0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 5U)))

?

(0x7c0U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 6U))

:

((0U

==

(0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 6U)))

?

(0x7e0U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 5U))

:

((0U

==

(7U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 7U)))

?

(0x7f0U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 4U))

:

((0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 8U)))

?

(0x7f8U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 3U))

:

((0U

==

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 9U)))

?

(0x7fcU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 2U))

:

(0x7feU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

<< 1U)))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_LZ\_Fa

= (0xffU & ((0U == (0x1ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 1U))) ? 0xaU

: ((0U == (0xffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 2U)))

? 9U : ((0U == (0x7fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 3U)))

? 8U : ((0U ==

(0x3fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 4U)))

? 7U

: ((0U

==

(0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 5U)))

? 6U

:

((0U

==

(0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 6U)))

? 5U

:

((0U

==

(7U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 7U)))

? 4U

:

((0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 8U)))

? 3U

:

((0U

==

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 9U)))

? 2U

: 1U))))))))));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_LZ\_Fa = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fa\_rcvr

= (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)));

}

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:381

if ((1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsValid)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_SUBNb)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_rcvr

= ((0U == (0x1ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 1U))) ? (0x400U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 0xaU))

: ((0U == (0xffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 2U))) ? (0x600U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 9U))

: ((0U == (0x7fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 3U))) ?

(0x700U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 8U)) : ((0U ==

(0x3fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 4U)))

? (0x780U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 7U))

: ((0U

==

(0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 5U)))

?

(0x7c0U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 6U))

:

((0U

==

(0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 6U)))

?

(0x7e0U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 5U))

:

((0U

==

(7U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 7U)))

?

(0x7f0U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 4U))

:

((0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 8U)))

?

(0x7f8U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 3U))

:

((0U

==

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 9U)))

?

(0x7fcU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 2U))

:

(0x7feU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

<< 1U)))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_LZ\_Fb

= (0xffU & ((0U == (0x1ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 1U))) ? 0xaU

: ((0U == (0xffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 2U)))

? 9U : ((0U == (0x7fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 3U)))

? 8U : ((0U ==

(0x3fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 4U)))

? 7U

: ((0U

==

(0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 5U)))

? 6U

:

((0U

==

(0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 6U)))

? 5U

:

((0U

==

(7U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 7U)))

? 4U

:

((0U

==

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 8U)))

? 3U

:

((0U

==

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 9U)))

? 2U

: 1U))))))))));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_LZ\_Fb = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_rcvr

= (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)));

}

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw =

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_ldmw)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_stmw));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_illegal\_csr\_access

= (1U & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_system\_wen)

& (3U == (3U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1eU)))) | (

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled)

>> 2U)

& ((3U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1cU))

>

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

>> 1U)))))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled)

>> 2U) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_defined)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_ins\_valid

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_uses\_gprs1))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_uses\_fprs1));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_wb\_reg\_en =

(((~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wait))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_dmem\_wait\_d))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_incr\_type\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Large

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Denormal\_Large)

? (0x1ff8U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

<< 3U)) : (0x2000U | (0x1ff8U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

<< 3U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_unnormal\_case

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_in\_is\_NaN)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large\_is\_INF))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small\_is\_zero));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Diff

= (0x1fU & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Denormal\_Large)

^ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Denormal\_Small))

? (((0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU)) - (0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

>> 0xaU)))

- (IData)(1U)) : ((0x1fU &

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU))

- (0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

>> 0xaU)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Denormal\_Small)

? (0x1ff8U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

<< 3U)) : (0x2000U | (0x1ff8U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Small)

<< 3U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_b

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_is\_scl)

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_scl)

<< 0xaU) : ((0U != (3U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe)))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_b)

: 0x3c00U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a

= (0xffffU & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_is\_scl)

& (2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a\_update)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r1\_fmul\_z)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_rb\_fmul\_z))

: (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_is\_scl)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_oe))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_fadd\_z)

: (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_is\_scl)

& (3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_op)))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_z\_reg)

: ((0U != (3U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_pe)))

? (0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_r\_a)

: 0U)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_wen

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_WB))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rdy))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_r)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_w));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_WB

= ((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wait)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_WB))

| ((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_alu\_WB))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_w))))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md\_WB)

& (3U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_state))))

| (((~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_prev\_killed\_WB))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wfi\_unkilled\_WB))

& (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken)

| (0U != vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mip)))))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs

= (((((((((((((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_w))))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql\_unkilled));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:445

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_tmp0

= (0x7fU & ((IData)(0xfU) + ((((0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a)

>> 0xaU))

- (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_LZ\_Fa))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_SUBNa))

- (((0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b)

>> 0xaU))

- (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_LZ\_Fb))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_SUBNb)))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:412

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaEQFb

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fa\_rcvr)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_rcvr));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaNotEQFb

= ((~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaEQFb))

& (0U != (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_b))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:412

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_ieee\_rcvrd

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_rcvr;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_faith\_rcvrd

= (0x7feU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_ieee\_rcvrd)

<< 1U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_9\_1

= (0x1ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_faith\_rcvrd)

>> 1U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_a1\_Fb\_9\_1

= (0x200U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_9\_1));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:424

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2

= (0x7fffffU & VL\_DIV\_III(23, ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fa\_rcvr)

<< 0xcU), (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_rcvr)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_dmem\_burst

= (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw)

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_single)

? 0U : (((((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

| (4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (6U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

? ((0U == (3U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

? 3U : ((1U ==

(3U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

? 7U :

((2U ==

(3U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

? 0xfU

: 0U)))

: (((((7U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

| (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

| (0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type)))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_burst\_mark)

: 0U))) : 0U));

// ALWAYS at ../../src/verilog/core/sisc32\_ctrl.v:203

vlTOPp->\_\_Vtableidx1 = ((0x60U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_priv\_stack)

<< 4U)) | (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ecall)

<< 4U)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ebreak)

<< 3U)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_illegal\_csr\_access)

<< 2U)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction)

<< 1U)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_had\_ex\_DX))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_code\_DX

= vlTOPp->\_\_Vtable1\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_code\_DX

[vlTOPp->\_\_Vtableidx1];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_DX

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_had\_ex\_DX)

| ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ebreak)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ecall))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_illegal\_instruction))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_illegal\_csr\_access)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wdata = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_dvalid\_mix)

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_word\_WB)

? vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_high\_half\_WB)

?

((0xffff0000U

& vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata)

| (0xffffU

& (vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata

>> 0x10U)))

:

((0xffff0000U

& (vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata

<< 0x10U))

| (0xffffU

& vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hrdata))))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_wb\_reg\_en)

? vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_dmem\_addr\_WB

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr = (0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_wb\_reg\_en)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_base\_idx\_WB)

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw\_WB)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_reg\_addr\_WB)

: 0U)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen = (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_ldmw\_WB)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_dvalid\_mix))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_wb\_reg\_en));

// ALWAYS at ../../src/verilog/core/sisc\_fadd.v:311

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din

= (0x7ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small)

>> 3U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_Vfuncout

= (0x1fU & ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 4U : ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 5U : ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 6U : ((8U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 7U

: (

(0x10U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 8U

:

((0x20U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 9U

:

((0x40U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 0xaU

:

((0x80U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 0xbU

:

((0x100U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 0xcU

:

((0x200U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 0xdU

:

((0x400U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_din))

? 0xeU

: 0xfU))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_clz

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_clz11\_\_9\_\_Vfuncout;

// ALWAYS at ../../src/verilog/core/sisc\_fadd.v:309

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din

= (0x7ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small)

>> 3U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_Vfuncout

= (0x1fU & ((0x400U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 0xeU : ((0x200U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 0xdU : ((0x100U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 0xcU :

((0x80U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 0xbU :

((0x40U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 0xaU

: ((0x20U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 9U

:

((0x10U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 8U

:

((8U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 7U

:

((4U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 6U

:

((2U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 5U

:

((1U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_din))

? 4U

: 0U))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_cmo

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmo11\_\_8\_\_Vfuncout;

// ALWAYS at ../../src/verilog/core/sisc\_fmult.v:269

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EB

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_b)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGB

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_b));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_B

= (0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_InfSIG\_B

= (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_B

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EB))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_B

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EB))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_B)

? (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_b))

: (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_b))));

// ALWAYS at ../../src/verilog/core/sisc\_fmult.v:269

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGN

= (1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a)

^ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_b))

>> 0xfU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Inf\_Reg

= (0x7c00U | ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGN)

<< 0xfU));

// ALWAYS at ../../src/verilog/core/sisc\_fmult.v:269

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EA

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a)

>> 0xaU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGA

= (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_A

= (0x1fU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EA));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_InfSIG\_A

= (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGA));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_A

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EA))

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGA)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_A

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EA))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGA)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MA

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_A)

? (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a))

: (0x400U | (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd)

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_wd

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_wen)

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rdd

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_data\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_griu\_res

= (0x1fU & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta))

? (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U) : (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta))

? (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU) : (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_r\_griu\_res)))

+ ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta))

? 0U : (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB))

? 1U : 0U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_friu\_res

= (0x1fU & ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta))

? (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU) : (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta))

? (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U) : (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_r\_friu\_res)))

+ ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_sta))

? 0U : (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB))

? 1U : 0U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_WB

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_ren

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_int\_done\_w))))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_unkilled)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:454

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb

= (0xfffffU & ((0x1ffU & VL\_DIV\_III(32, (IData)(0x40000U),

((IData)(1U)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_a1\_Fb\_9\_1))))

\* (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fa\_rcvr)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:545

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0

= (0x7ffU & ((0x1000U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2)

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2

>> 2U) : (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2

>> 1U)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:563

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp

= (0x7fU & ((0x1000U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_tmp0)

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_tmp0)

- (IData)(1U))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp\_is\_Neg

= (1U & (VL\_GTES\_III(1,32,32, 0U, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)

>> 6U)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rd\_self = (1U & (

((3U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (5U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_wb\_reg\_en)))

:

(((7U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (1U

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen)

: 0U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_shift\_cnt

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_cmo)

< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Diff))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_cmo)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Diff));

// ALWAYS at ../../src/verilog/core/sisc\_fmult.v:322

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_INA = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_INB = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_IN = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_STK\_EXT = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_RND\_val = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ = 0U;

if ((1U & (~ (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_A)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_InfSIG\_A)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_B)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_InfSIG\_B))))))) {

if ((1U & (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_A)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_B))))) {

if ((1U & (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_A)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_B))))) {

// Function: CLZ11 at ../../src/verilog/core/sisc\_fmult.v:371

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MA;

// Function: CLZ11 at ../../src/verilog/core/sisc\_fmult.v:372

// Function: rnd\_eval at ../../src/verilog/core/sisc\_fmult.v:419

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_Vfuncout

= (0x3ffU & ((0x400U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 0U : ((0x200U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 1U : (

(0x100U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 2U

:

((0x80U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 3U

:

((0x40U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 4U

:

((0x20U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 5U

:

((0x10U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 6U

:

((8U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 7U

:

((4U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 8U

:

((2U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 9U

:

((1U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_din))

? 0xaU

: 0U))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_INA

= (0x3ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_A)

? (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_13\_\_Vfuncout)

: 0U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MB;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_Vfuncout

= (0x3ffU & ((0x400U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 0U : ((0x200U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 1U : (

(0x100U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 2U

:

((0x80U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 3U

:

((0x40U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 4U

:

((0x20U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 5U

:

((0x10U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 6U

:

((8U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 7U

:

((4U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 8U

:

((2U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 9U

:

((1U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_din))

? 0xaU

: 0U))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_INB

= (0x3ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_B)

? (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_CLZ11\_\_14\_\_Vfuncout)

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_IN

= (0x3ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_INA)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_INB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ

= (0x7fU & (((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EA)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EB))

- (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_IN))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_A))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_B)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x7fffffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MA)

\* (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MB)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x7fffffU & ((0x16U >= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_IN))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

<< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_IN))

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ\_Movf1

= (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0x15U));

if ((0x200000U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ

= (0x7fU & ((IData)(1U) + VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_minnorm\_case = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x7fffffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

<< 1U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_minnorm\_case

= (1U & ((0U == (VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))

- (IData)(0xfU)))

? 1U : 0U));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Range\_Check

= (0x7fU & ((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EA)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EB))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_A))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Denorm\_B))

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ\_Movf1))

- (IData)(0xfU))

- (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_LZ\_IN))

- (IData)(1U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Shift

= (0x7fU & VL\_NEGATE\_I((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Range\_Check)));

if (VL\_LTES\_III(1,32,32, 0U, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Shift)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_STK\_EXT

= (0x7ffU & ((((0x1fU >= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Shift))

? ((IData)(1U)

<< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Shift))

: 0U) - (IData)(1U))

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x7fffffU & ((0x16U >= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Shift))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Shift))

: 0U));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_STK

= (0U != ((0x1ff800U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

<< 0xbU))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_STK\_EXT)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_stk

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_STK;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R

= (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0xaU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_L

= (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0xbU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGN;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xdU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| (((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_stk))

<< 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

if ((VL\_ULL(0) < VL\_TIME\_Q())) {

if ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd))) {

if (VL\_UNLIKELY((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd)))) {

VL\_WRITEF("Error! illegal rounding mode.\n\n");

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

VL\_WRITEF("a : %b\n",16,

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_a);

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

VL\_WRITEF("rnd : %b\n",

3,vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd);

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_stk)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (8U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

}

}

} else {

if ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd))) {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign)

<< 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign)

<< 3U));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign))

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| (4U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign))

<< 2U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| (8U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Sign))

<< 3U)));

}

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_R)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_L)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_stk))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout));

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_RND\_val

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_rnd\_eval\_\_15\_\_Vfuncout;

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_RND\_val))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x7fffffU & ((IData)(0x800U)

+ vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ));

}

if ((0x400000U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ)) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ

= (0x7fU & ((IData)(1U) + VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x7fffffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 1U));

}

if ((1U & (VL\_GTES\_III(32,32,32, 0xfU,

VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)))

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0x15U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ

= (0x7fU & ((IData)(1U) + VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ\_Zero

= (0xfU == VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ

= (0x7fU & (((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)

>> 6U)) & VL\_LTES\_III(1,32,32, 0xfU,

VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))))

? (VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))

- (IData)(0xfU))

: 0U));

if (VL\_LTES\_III(1,32,32, 0x1fU, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)))) {

if ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_RND\_val))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x6007ffU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ = 0x1fU;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ = 0x1eU;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

= (0x1ff800U | vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ);

}

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_r1a

= (0x1fU & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_WB))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_friu\_res)

: (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_WB))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_griu\_res)

: (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_retire\_WB

= (1U & (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_WB)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_prev\_killed\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_WB)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra3

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rs\_self)

? (0x10U | (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr)

>> 1U))) :

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs)

? (0x10U | (0xfU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1cU)))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_ren)

? (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU) : (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra2

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs)

? (0x10U | (0xfU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x15U)))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_ren)

? (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U) : (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:459

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFbMsb

= (1U & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb

>> 0x13U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFbRnd

= (0x1ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFbMsb)

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb

>> 0xbU) : (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb

>> 0xaU)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:470

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp0

= (0x3fffU & ((vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb

>> 6U) + (0x7fU & (((0x7fU &

(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb

>> 0xdU))

\* (0x7fU

& (~

(0x7fffU

& (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_faith\_rcvrd)

\*

(0x1ffU

& VL\_DIV\_III(32, (IData)(0x40000U),

((IData)(1U)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_a1\_Fb\_9\_1)))))

>> 5U)))))

>> 7U))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:567

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsEzTmpBig

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsValid)

& (VL\_GTES\_III(1,32,32, 0U, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)

>> 6U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd)

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rda))

? 2U : 1U) : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rd\_self)

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr))

? 2U : 1U) : 3U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wd

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd)

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_wd

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rd\_self)

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr))

? (0xffff0000U & (vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wdata

<< 0x10U)) :

(0xffffU & vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wdata))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_wen)

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rdd

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen)

? vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wdata

: ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_wb\_src\_sel\_WB))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_data\_WB

: ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_wb\_src\_sel\_WB))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_data\_WB

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_wb\_src\_sel\_WB))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_load\_data\_WB

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_data\_WB)))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wa

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd)

? (0x10U | (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rda)

>> 1U))) : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rd\_self)

? (0x10U

| (0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr)

>> 1U)))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_wen)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_rda)

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_to\_wr\_WB)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wen

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_w\_fprd)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_wen)

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rd\_self)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen)

: (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_wen)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_wen))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_wr\_reg\_unkilled\_WB)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_WB))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_STK

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_shift\_cnt)

>= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_clz));

// ALWAYS at ../../src/verilog/core/sisc\_fmult.v:489

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg = 0U;

if ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_A)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_InfSIG\_A)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_B)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_InfSIG\_B))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg = 0x7c01U;

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_A)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MaxEXP\_B))) {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_A)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_B))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (4U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg = 0x7c01U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Inf\_Reg;

}

} else {

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_A)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_B))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (1U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg

= ((0x7fffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGN)

<< 0xfU));

} else {

if (VL\_LTES\_III(1,32,32, 0x1fU, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (0x10U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (0x20U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

if ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_RND\_val))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (2U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

}

} else {

if ((0U == VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (8U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

if (((0U == (0x3ffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0xbU)))

& (0U == (0x1fU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (1U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_z\_reg

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_SIGN)

<< 0xfU) | ((0x7c00U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ)

<< 0xaU))

| (0x3ffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0xbU))));

if ((1U & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_RND\_val)

>> 1U) | (((~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_A)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_Zero\_B)))

& (0U == (0x1fU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_EZ))))

& (0U == (0x3ffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_MZ

>> 0xbU))))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg

= (0x20U | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fmul\_\_DOT\_\_status\_reg));

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra1

= (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs)

? (0x10U | (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_r1a)

>> 1U))) :

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_reg\_ren)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_r1a)

: (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data

= ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra3))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra3]

: 0U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data

= ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra2))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra2]

: 0U);

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:473

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_MSB\_sum\_tmp0

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp0)

>> 0xdU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp1

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_MSB\_sum\_tmp0)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp0)

: (0x3ffeU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp0)

<< 1U)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:586

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp2

= (0x7ffU & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsEzTmpBig)

? ((0U == (0x7fU & ((IData)(1U)

- VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 0xbU) : ((1U == (0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 0xaU)

: ((2U ==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 9U)

: ((3U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 8U)

:

((4U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 7U)

:

((5U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 6U)

:

((6U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 5U)

:

((7U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 4U)

:

((8U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 3U)

:

((9U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 2U)

:

((0xaU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 1U)

:

((0xbU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

:

((0xcU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x3ffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 1U))

:

((0xdU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x1ffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 2U))

:

((0xeU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0xffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 3U))

:

((0xfU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x7fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 4U))

:

((0x10U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x3fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 5U))

:

((0x11U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 6U))

:

((0x12U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 7U))

:

((0x13U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(7U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 8U))

:

((0x14U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 9U))

:

((0x15U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 0xaU))

: 0U))))))))))))))))))))))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 0xbU)) >> 0xbU));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:586

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp3

= (0x7ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsEzTmpBig)

? ((0U == (0x7fU & ((IData)(1U)

- VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 0xbU) : ((1U == (0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 0xaU)

: ((2U ==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 9U)

: ((3U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 8U)

:

((4U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 7U)

:

((5U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 6U)

:

((6U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 5U)

:

((7U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 4U)

:

((8U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 3U)

:

((9U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 2U)

:

((0xaU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 1U)

:

((0xbU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

:

((0xcU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x3ffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 1U))

:

((0xdU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x1ffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 2U))

:

((0xeU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0xffU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 3U))

:

((0xfU

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x7fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 4U))

:

((0x10U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x3fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 5U))

:

((0x11U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0x1fU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 6U))

:

((0x12U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 7U))

:

((0x13U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(7U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 8U))

:

((0x14U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(3U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 9U))

:

((0x15U

==

(0x7fU

& ((IData)(1U)

-

VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

?

(1U

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

>> 0xaU))

: 0U))))))))))))))))))))))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp0)

<< 0xbU)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_wen\_internal

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wen)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_step\_mask)))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wa)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs3

= ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wen)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra3)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wa)))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra3)))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat\_unkilled)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_stmw\_WB)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_dvalid\_mix))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs2

= ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wen)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra2)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wa)))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra2)))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs2)

| ((((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_unkilled)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx\_unkilled))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql\_unkilled))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small\_nor

= (0x7fffU & (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small)

>> (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_small\_shift\_cnt))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_STK)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data

= ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra1))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_regfile\_\_DOT\_\_data

[vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra1]

: 0U);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs1

= ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wen)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra1)

== (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_wa)))

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_ra1)))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_rs1)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_uses\_gprs1)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_uses\_fprs1))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:488

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp2

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp1;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_MSB\_sum\_tmp2

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp2)

>> 0xdU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp3

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_MSB\_sum\_tmp2)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp2)

: (0x3ffeU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp2)

<< 1U)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:556

if (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsEzTmpBig) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1

= ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1))

| (2U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp2)

<< 1U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1

= ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1))

| (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp3)

>> 0xaU)));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1

= (3U & ((0x1000U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2)

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2

>> 1U) : vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_FaDivFb2));

}

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:573

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_stk0

= (1U & ((0U == (0x7ffU & VL\_MODDIV\_III(23,

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fa\_rcvr)

<< 0xcU), (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Fb\_rcvr))))

? 0U : 1U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_STK

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_stk0)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_IsEzTmpBig)

& ((0xbU < (0x7fU & ((IData)(1U) - VL\_EXTENDS\_II(7,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))))

| (0U != (0x3ffU & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp3))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data\_bypassed

= (((~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_load\_in\_WB))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs3))

? ((0xffff0000U & (((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

>> 0x10U) : (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data

>> 0x10U))

<< 0x10U)) | (0xffffU

& ((1U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data)))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed

= (((~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_load\_in\_WB))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs2))

? ((0xffff0000U & (((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

>> 0x10U) : (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data

>> 0x10U))

<< 0x10U)) | (0xffffU

& ((1U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data)))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z

= (0x7fffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_subtract)

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Large)

- (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small\_nor))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Large)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Small\_nor))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed

= (((~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_load\_in\_WB))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs1))

? ((0xffff0000U & (((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

>> 0x10U) : (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data

>> 0x10U))

<< 0x10U)) | (0xffffU

& ((1U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_reg\_bwen))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_bypass\_reg

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data)))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_DX

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_WB)

| (((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wait)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_load\_in\_WB)

& (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs1)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs2))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs3))))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md\_WB)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs1)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_raw\_rs2)))

& (3U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_state))))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_fence\_i)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_store\_in\_WB)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md\_unkilled)

& (0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_state))))

& (~ (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_DX)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken)))));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:507

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_MSB\_sum\_tmp4

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp3)

>> 0xdU));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp5

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_MSB\_sum\_tmp4)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp3)

: (0x3ffeU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_sum\_tmp3)

<< 1U)));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:614

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_STK

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_STK;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R

= (1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_L

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp1)

>> 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_Sign;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xdU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| (((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_STK))

<< 1U));

if ((VL\_ULL(0) < VL\_TIME\_Q())) {

if ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd))) {

if (VL\_UNLIKELY((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd)))) {

VL\_WRITEF("error! illegal rounding mode.\n\n");

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

VL\_WRITEF("a : %b\n",16,vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_a);

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

VL\_WRITEF("rnd : %b\n",3,vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd);

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_STK)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (8U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

}

}

} else {

if ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd))) {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_STK))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign)

<< 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign)

<< 3U));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign))

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_STK))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| (4U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign))

<< 2U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| (8U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Sign))

<< 3U)));

}

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_rnd))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_R)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_L)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_STK))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout));

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_rnd\_v\_tmp

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_RND\_eval\_\_12\_\_Vfuncout;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp

= (0x7ffU & ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_rnd\_v\_tmp))

? ((IData)(1U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp2))

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp2)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_rdata = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_rs\_self)

? (

(1U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr))

?

(0xffffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data\_bypassed

>> 0x10U))

:

(0xffffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data\_bypassed))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs3\_data\_bypassed);

// ALWAYS at ../../src/verilog/core/sisc32\_pipeline.v:547

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_mem\_type

= (7U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_Vfuncout

= ((0U == (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_mem\_type))

? ((0xff000000U & (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data

<< 0x18U)) | ((0xff0000U

& (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data

<< 0x10U))

| ((0xff00U

& (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data

<< 8U))

| (0xffU

& vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data))))

: ((1U == (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_mem\_type))

? ((0xffff0000U & (vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data

<< 0x10U)) | (0xffffU

& vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data))

: vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_data));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wdata = vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_store\_data\_\_1\_\_Vfuncout;

// ALWAYS at ../../src/verilog/core/sisc32\_src\_b\_mux.v:10

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed

: ((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_imm

: ((2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_b\_sel))

? 4U : 0U)));

// ALWAYS at ../../src/verilog/core/sisc32\_mul\_div.v:59

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_is\_signed

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_2\_signed;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_data

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_Vfuncout

= (((vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_data

>> 0x1fU) & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_is\_signed))

? VL\_NEGATE\_I(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_data)

: vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_data);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_in\_2

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_4\_\_Vfuncout;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp

= (0x7fU & ((0x4000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z))

? ((IData)(1U) + (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU)))

: (0x1fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xaU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_p2

= (0x7fffU & ((0x4000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z))

? (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z)

>> 1U) | (1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z)))

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_sign\_in\_1

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_1\_signed)

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed

>> 0x1fU));

// ALWAYS at ../../src/verilog/core/sisc32\_src\_a\_mux.v:10

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

= ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed

: ((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_src\_a\_sel))

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX

: 0U));

// ALWAYS at ../../src/verilog/core/sisc32\_mul\_div.v:57

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_is\_signed

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_req\_in\_1\_signed;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_data

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_Vfuncout

= (((vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_data

>> 0x1fU) & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_is\_signed))

? VL\_NEGATE\_I(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_data)

: vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_data);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_in\_1

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_abs\_input\_\_3\_\_Vfuncout;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_wdata

= ((0x4000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)

? (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xfU)) : vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_r1d

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs)

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_r1a))

? (0xffffU & (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed

>> 0x10U)) : (0xffffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX

= ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_DX)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_DX))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken));

// ALWAYS at ../../src/verilog/core/sisc\_fdiv\_macro.v:619

if ((VL\_LTES\_III(1,32,32, 0x1fU, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))

& (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)

>> 6U)))) {

if ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_rnd\_v\_tmp))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_reg = 0x400U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_reg = 0x1fU;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_reg = 0x7ffU;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_reg = 0x1eU;

}

} else {

if ((1U & (VL\_GTES\_III(1,32,32, 0U, VL\_EXTENDS\_II(32,7, (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp)

>> 6U)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_reg

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_reg

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp)

>> 0xaU));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_reg

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_F\_z\_tmp;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_reg

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fdiv\_\_DOT\_\_E\_z\_tmp;

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wdata = (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw\_WB))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_word\_WB)

? vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_rdata

:

((0xffff0000U

& (vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_rdata

<< 0x10U))

| (0xffffU

& vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_rdata)))

: vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wdata\_delayed);

// ALWAYS at ../../src/verilog/core/sisc\_fadd.v:353

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_p2;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_Vfuncout

= (0x7fU & ((0x2000U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 0U : ((0x1000U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 1U : ((0x800U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 2U : ((0x400U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 3U

: (

(0x200U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 4U

:

((0x100U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 5U

:

((0x80U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 6U

:

((0x40U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 7U

:

((0x20U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 8U

:

((0x10U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 9U

:

((8U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 0xaU

:

((4U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 0xbU

:

((2U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 0xcU

:

((1U

& (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_din))

? 0xdU

: 0xeU)))))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_cmz

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_cmz15\_\_10\_\_Vfuncout;

// ALWAYS at ../../src/verilog/core/sisc32\_alu.v:13

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_out

= ((8U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

>= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

< vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? VL\_GTES\_III(32,32,32, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)

: VL\_LTS\_III(32,32,32, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)))

: ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? VL\_SHIFTRS\_III(32,32,5, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a,

(0x1fU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

- vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

!= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

== vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))))

: ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

| vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))

: ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

>> (0x1fU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

^ vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)))

: ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? 0U : ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_op))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

<< (0x1fU & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b))

: (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_a

+ vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_src\_b)))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fneg\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsgn\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fabs\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mfrr\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_mrfr\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvc

= (((0xbU == (0x7fU & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX))

& (4U == (7U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_ins\_extop)

>> 2U)))) & (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

// ALWAYS at ../../src/verilog/core/sisc32\_csr\_file.v:133

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_wdata\_internal

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_wdata;

if (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_system\_wen)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_wdata\_internal

= ((6U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

| vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_wdata)

: ((7U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_csr\_cmd\_unkilled))

? (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_rdata

& (~ vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_wdata))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_wdata));

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wen = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_wen\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_eret =

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_eret\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dret =

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dret\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_en = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_dmem\_en\_unkilled)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_DX)));

VL\_ASSIGN\_SII(32,vlTOPp->dmem\_hwdata, vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wdata);

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_shift\_cnt

= (0x7fU & ((((IData)(1U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_cmz))

< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_cmz)

: ((0U < (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp)

- (IData)(1U)) : 0U)));

// ALWAYS at ../../src/verilog/core/sisc32\_mul\_div.v:92

vlTOPp->\_\_Vtableidx3 = (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_counter)

<< 3U) | (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_uses\_md)

<< 2U) | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_state)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_next\_state

= vlTOPp->\_\_Vtable3\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_md\_\_DOT\_\_next\_state

[vlTOPp->\_\_Vtableidx3];

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_need\_alu

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr)

& (0xfU != (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_redirect = ((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_eret))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dret))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_step\_redirect));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_addr = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_en)

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_alu\_out

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await)

? vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_dmem\_addr\_WB

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_en = ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_en)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor

= (0x7fU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp)

- (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_shift\_cnt)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor

= (0x7fffU & ((0xeU >= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_shift\_cnt))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_p2)

<< (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_shift\_cnt))

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_b

= (0xffffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp)

? vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_r1d

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_need\_alu)

? (((0U == (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU)))

| (0x1fU == (0x1fU &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))))

? 0x3c00U : (0x7c00U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x11U)))

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd)

? ((0x800U & vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_fcsr)

? ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_uTRNG\_\_DOT\_\_data))

| ((0x7c00U &

((0x3ffffc00U

& (((~

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))

<< 0xaU)

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_fcsr

>> 2U)))

| (0x7c00U

& ((vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x11U)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_uTRNG\_\_DOT\_\_data)))))

| (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_uTRNG\_\_DOT\_\_data))))

: ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_uTRNG\_\_DOT\_\_data))

| ((0x7c00U &

(vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x11U))

| (0x3ffU

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_uTRNG\_\_DOT\_\_data)))))

: (0xffffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fpu\_r\_fp\_rs)

? ((0x100000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)

?

(0xffffU

& (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed

>> 0x10U))

:

(0xffffU

& vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed))

: vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs2\_data\_bypassed))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_req

= (((((((((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fadd))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_need\_alu));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op

= (0xfU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsub)

? 1U : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmul)

? 2U : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fdiv)

? 3U : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fsat)

? 4U

: ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frnd)

? 5U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fr2i)

? 6U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_i2fr)

?

((0x8000000U

& vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)

? 0xfU

: 7U)

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmvr\_need\_alu)

? 0xdU

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmin)

? 8U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_fmax)

? 9U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famn)

? 0xaU

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_famx)

? 0xbU

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_frcp)

? 0xcU

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_feql)

? 0xeU

: 0U)))))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_IF

= ((((IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_imem\_hresp)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_ibuf\_wait)))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_redirect)))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_replay\_IF)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_IF

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_DX)

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_ibuf\_wait)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_redirect)))

& (~ ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken)))));

VL\_ASSIGN\_SII(32,vlTOPp->dmem\_haddr, vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_addr);

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_m\_hwrite

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_en)

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wen)

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_dmem\_wen\_WB)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await))));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_size = (7U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_en)

?

(((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_xxmw)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_size)

:

(3U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0xcU)))

: 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_wait\_cmd

= (((~ (IData)((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt))))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_burst\_cnt\_hit))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_en));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_burst\_len = (0xfU

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_en)

?

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_dmem\_burst\_WB)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_dmem\_burst))

: 0U));

// ALWAYS at ../../src/verilog/core/sisc\_fadd.v:358

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_STK

= (0U != (3U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)

>> 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_L

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)

>> 3U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign

= (1U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large)

>> 0xfU));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd;

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xdU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| (((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_STK))

<< 1U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

if ((VL\_ULL(0) < VL\_TIME\_Q())) {

if ((4U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND))) {

if (VL\_UNLIKELY((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND)))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

VL\_WRITEF("Error! illegal rounding mode = %x\n\n",

3,vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND);

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_STK)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (8U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

}

}

} else {

if ((2U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND))) {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_STK))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign)

<< 2U));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign)

<< 3U));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign))

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_STK))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| (4U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign))

<< 2U)));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| (8U & ((~ (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Sign))

<< 3U)));

}

} else {

if ((1U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_RND))) {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (0xbU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

} else {

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= ((0xeU & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout))

| ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_R)

& ((IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_L)

| (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_STK))));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (4U | (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout

= (7U & (IData)(vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout));

}

}

}

}

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_val

= vlTOPp->\_\_Vfunc\_sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_eval\_\_11\_\_Vfuncout;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_start

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_req)

& (0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op)))

| (1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_req\_scl

= ((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_req)

& ((((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op))

| (1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op)))

| (2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op)))

| (3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_op))))

& (0U != (0x1fU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU)))) & (0xfU

!= (0x1fU

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_kill\_IF

= ((((((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_IF)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_IF))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_DX))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_redirect)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_sisc\_force\_IF))))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_redirect)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_ibuf\_wait)))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_replay\_IF))

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken));

// ALWAYS at ../../src/verilog/core/sisc32\_ctrl.v:582

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_taken)

? 5U : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_WB)

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_debug)

? 9U : ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_ex\_code\_WB))

? 7U : 5U)) : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_step\_ret)

? 7U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_dbg\_req)

? 7U

:

((((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_interrupt\_replay)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_replay\_IF))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_stall\_IF)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_ibuf\_wait))))

? 4U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_eret)

? 6U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dret)

? 8U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_branch\_taken)

? 1U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jal)

? 2U

:

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_ctrl\_\_DOT\_\_jalr)

? 3U

: 0U))))))))));

VL\_ASSIGN\_SII(1,vlTOPp->dmem\_hwrite, vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_m\_hwrite);

VL\_ASSIGN\_SII(3,vlTOPp->dmem\_hsize, vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_size);

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_m\_htrans

= ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_wait\_cmd)

? 2U : ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_await)

? 3U : 0U));

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_m\_hburst

= ((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_burst\_len))

? ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_burst\_len))

? 3U : ((7U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_burst\_len))

? 5U : ((0xfU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_burst\_len))

? 7U : 1U))) : 0U);

vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_aready = (((0U != (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_burst\_len))

& (IData)(vlTOPp->\_\_Vcellinp\_\_sisc32\_core\_\_dmem\_hready))

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_en));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_rnd

= (0x7fffU & ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_val))

? ((IData)(8U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor))

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)));

// ALWAYS at ../../src/verilog/core/sisc32\_PC\_mux.v:21

if ((8U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

if ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_IF;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 4U;

} else {

if ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_IF;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 4U;

} else {

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base = 0x800U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 8U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_dpc;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 0U;

}

}

}

} else {

if ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

if ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base = 0x800U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_csr\_\_DOT\_\_mepc;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 0U;

}

} else {

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_handler\_PC;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 0U;

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_IF;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 0U;

}

}

} else {

if ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_rs1\_data\_bypassed;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset

= ((0xfffff800U & (VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0xbU))

| (0x7feU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U)));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset

= ((0xfff00000U & (VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0x14U))

| ((0xff000U & vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX)

| ((0x800U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 9U))

| ((0x7e0U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))

| (0x1eU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))))));

}

} else {

if ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_src\_sel))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_DX;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset

= ((0xfffff000U & (VL\_NEGATE\_I((IData)(

(1U

& (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1fU))))

<< 0xcU))

| ((0x800U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

<< 4U)) |

((0x7e0U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x14U))

| (0x1eU & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 7U)))));

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

= vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_IF;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset = 4U;

}

}

}

}

VL\_ASSIGN\_SII(2,vlTOPp->dmem\_htrans, vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_m\_htrans);

VL\_ASSIGN\_SII(3,vlTOPp->dmem\_hburst, vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_bridge\_\_DOT\_\_m\_hburst);

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_vld\_ldmw\_cmd

= (((1U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_ldmw)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_aready))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wait))));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_vld\_stmw\_cmd

= (((2U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_type))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait)))

| (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_stmw)

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_aready))

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_dmem\_wait))));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor\_rnd

= (0x7fffU & ((0x4000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_rnd))

? ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_rnd)

>> 1U) : (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_rnd)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd

= (0x7fU & ((0x4000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_rnd))

? ((IData)(1U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor))

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_PIF

= (vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_base

+ vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PCmux\_\_DOT\_\_offset);

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_vld\_xxmw\_cmd

= (((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_single)

& (~ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_dmem\_wait)))

| ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_vld\_ldmw\_cmd)

| (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_vld\_stmw\_cmd)));

// ALWAYS at ../../src/verilog/core/sisc\_fadd.v:372

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_z\_p2 = 0U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_status\_p2 = 0U;

if ((0U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_status\_p2 = 1U;

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_z\_p2

= ((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_rnd))

? 0x8000U : 0U);

} else {

if ((0U == (3U & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)

>> 0xdU)))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_z\_p2

= ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))

| (0x3ffU & ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)

>> 3U)));

if ((1U & (((0x4000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z))

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_STK))

| (0U != (7U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor)))))) {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_status\_p2 = 0x20U;

}

} else {

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_status\_p2

= (((0x1fU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd))

& ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_val)

>> 2U)) ? 0x32U : ((0x1fU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd))

? 0x30U :

((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_val))

? 0x20U

: 0U)));

vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_z\_p2

= ((0x8000U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_Large))

| ((0x7c00U & (((0x1fU <= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd))

? (0x7fU & ((4U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_val))

? 0x1fU

: 0x1eU))

: ((0U >= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd))

? 1U : (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd)))

<< 0xaU)) | (0x3ffU

& (((0x1fU

<= (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_E\_Comp\_nor\_rnd))

?

((4U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_RND\_val))

?

(0x6007U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor\_rnd))

:

(0x1ff8U

| (0x6007U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor\_rnd))))

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_fpu\_\_DOT\_\_falu\_\_DOT\_\_fadd\_\_DOT\_\_M\_Z\_nor\_rnd))

>> 3U))));

}

}

VL\_ASSIGN\_SII(32,vlTOPp->imem\_haddr, vlTOPp->sisc32\_core\_\_DOT\_\_pipeline\_\_DOT\_\_PC\_PIF);

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark =

((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_vld\_xxmw\_cmd)

? (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked)

: (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_marked\_WB));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_zero =

(0xfU & ((1U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0U : ((2U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 1U : ((4U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 2U : ((8U & (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 3U :

((0x10U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 4U :

((0x20U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 5U

: ((0x40U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 6U

:

((0x80U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 7U

:

((0x100U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 8U

:

((0x200U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 9U

:

((0x400U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0xaU

:

((0x800U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0xbU

:

((0x1000U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0xcU

:

((0x2000U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0xdU

:

((0x4000U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0xeU

:

((0x8000U

& (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_mark))

? 0xfU

: 0U)))))))))))))))));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_idx\_marked

= ((0x10U & (vlTOPp->sisc32\_core\_\_DOT\_\_inst\_DX

>> 0x1bU)) | (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_zero));

vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_reg\_addr\_next

= (0x1fU & (((((7U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (8U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (9U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (0xaU == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? ((IData)(1U) + ((IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_reg\_addr\_WB)

+ (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_cur\_zero)))

: (((((3U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB))

| (4U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (5U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

| (6U == (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_\_DOT\_\_lsu\_type\_WB)))

? ((IData)(1U) + (IData)(vlTOPp->sisc32\_core\_\_DOT\_\_lsu\_reg\_addr))

: 0U)));

}