1. Description

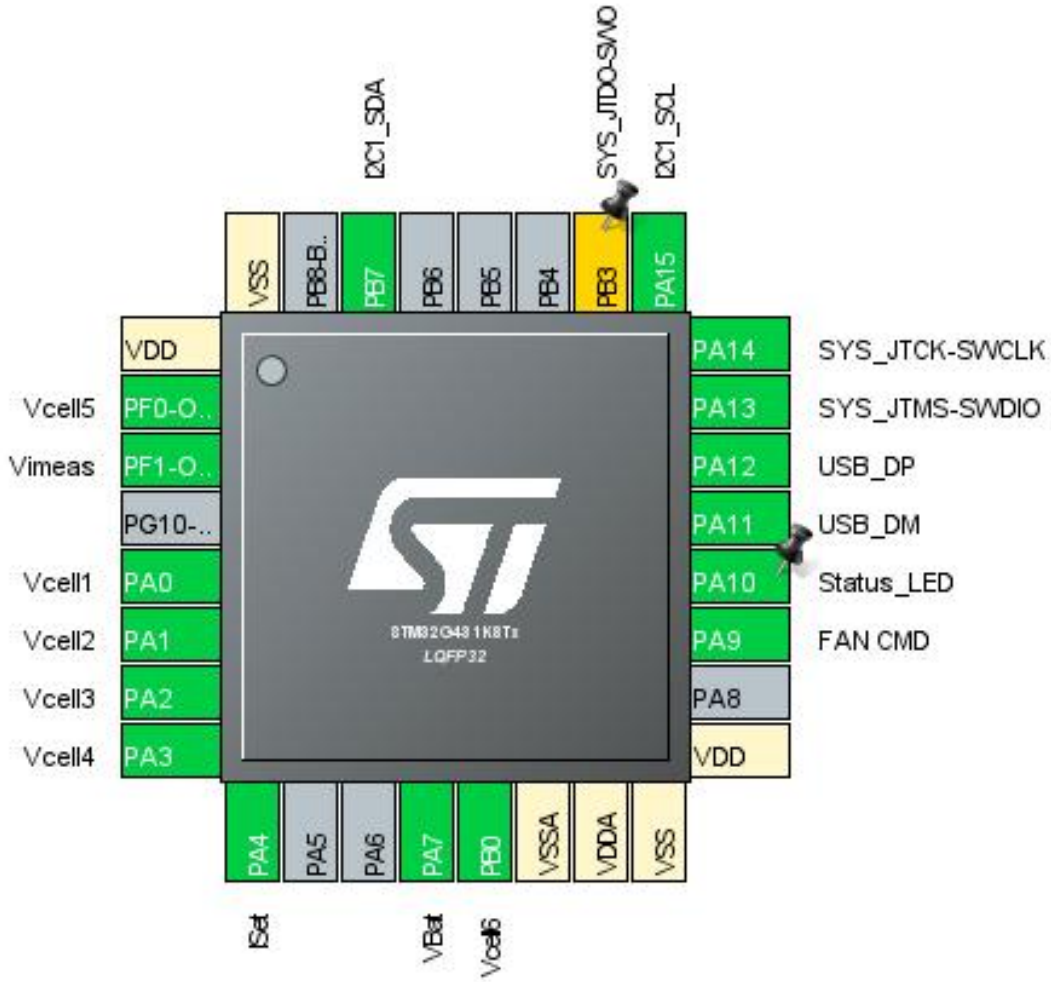
1.1. Project

Project Name	Battery_e-load
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	08/14/2019

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G431K8Tx
MCU Package	LQFP32
MCU Pin number	32

2. Pinout Configuration

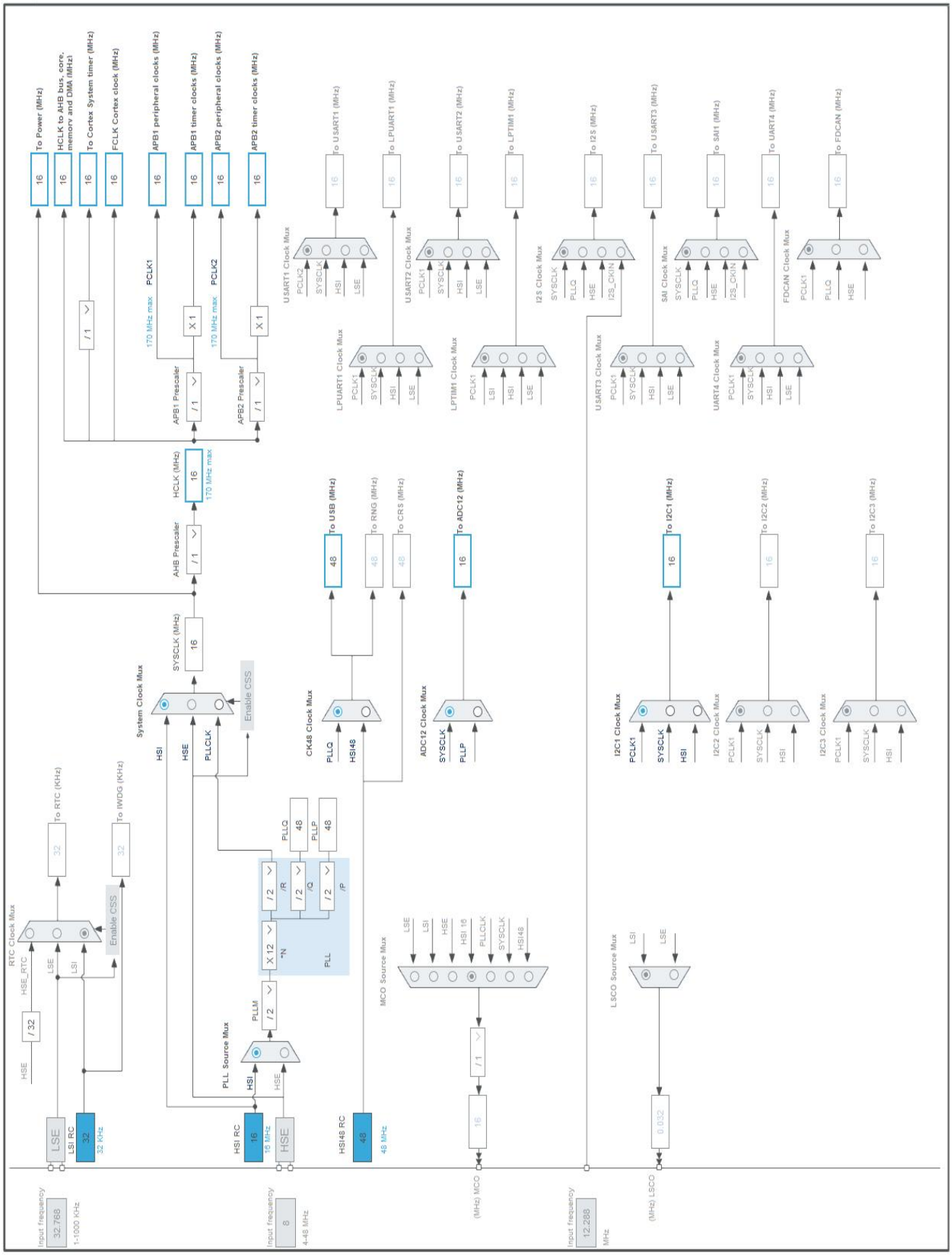


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0-OSC_IN	I/O	ADC1_IN10	Vcell5
3	PF1-OSC_OUT	I/O	ADC2_IN10	Vimeas
5	PA0	I/O	ADC1_IN1	Vcell1
6	PA1	I/O	ADC1_IN2	Vcell2
7	PA2	I/O	ADC1_IN3	Vcell3
8	PA3	I/O	ADC1_IN4	Vcell4
9	PA4	I/O	DAC1_OUT1	ISet
12	PA7	I/O	ADC2_IN4	VBat
13	PB0	I/O	ADC1_IN15	Vcell6
14	VSSA	Power		
15	VDDA	Power		
16	VSS	Power		
17	VDD	Power		
19	PA9	I/O	TIM2_CH3	FAN CMD
20	PA10	I/O	TIM1_CH3	Status_LED
21	PA11	I/O	USB_DM	
22	PA12	I/O	USB_DP	
23	PA13	I/O	SYS_JTMS-SWDIO	
24	PA14	I/O	SYS_JTCK-SWCLK	
25	PA15	I/O	I2C1_SCL	
26	PB3 *	I/O	SYS_JTDO-SWO	
30	PB7	I/O	I2C1_SDA	
32	VSS	Power		

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Battery_e-load
Project Folder	C:\Users\adamiens\STM32CubeIDE\workspace_1.0.2\Battery_e-load
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.1.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
MCU	STM32G431K8Tx
Datasheet	DS12589_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: IN4

mode: IN10

mode: IN15

mode: Vbat Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

mode: IN4

mode: IN10

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. CORDIC

mode: Activated

7.4. DAC1

OUT1 mode: Connected to external pin only

7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
DAC High Frequency	Mode Automatic
DMA Double Data	Disable
Signed Format	Disable
Trigger	None
Trigger2	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.5. I2C1

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00303D5B

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.7. TIM1

Channel3: PWM Generation CH3

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.8. TIM2

Channel3: PWM Generation CH3

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.9. USB

mode: Device (FS)

7.9.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy
Sof Enable	Disabled

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

7.10. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.10.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING_DESC (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled

USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	1000
USB CDC Tx Buffer Size	1000

7.10.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PF0-OSC_IN	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	Vcell5
	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	Vcell1
	PA1	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	Vcell2
	PA2	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	Vcell3
	PA3	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	Vcell4
	PB0	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	Vcell6
ADC2	PF1-OSC_OUT	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	Vimeas
	PA7	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	VBat
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	ISet
I2C1	PA15	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	Status_LED
TIM2	PA9	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	FAN CMD
USB	PA11	USB_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USB low priority interrupt remap	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupt	unused		
USB high priority interrupt remap	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	unused		
FPU global interrupt	unused		
CORDIC interrupt	unused		

*** User modified value**

9. Software Pack Report