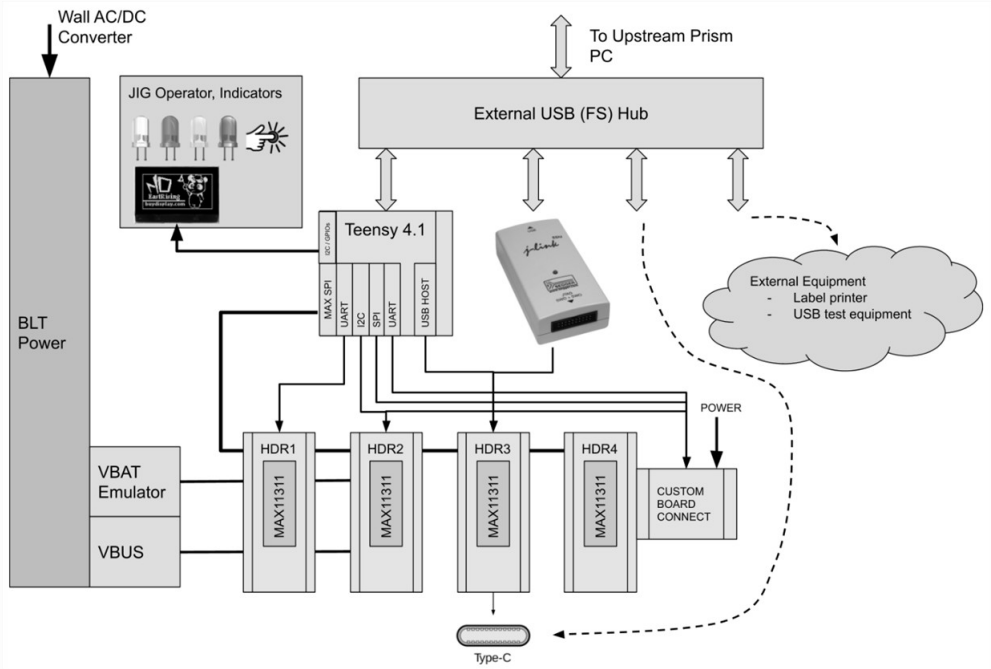


Prism Teensy Board level Test (BLT)

Refer to www.sistemi.ca for Prism/Lente Test Framework.

Testing Capabilities:

Each Header (1, 2, 3, 4) exposes the MAX11311 chip pins to the DUT. Each pin can be configured for either GPIO, DAC (12 bit) or ADC (12 bit), and output range of 0-2.5/5/10V.

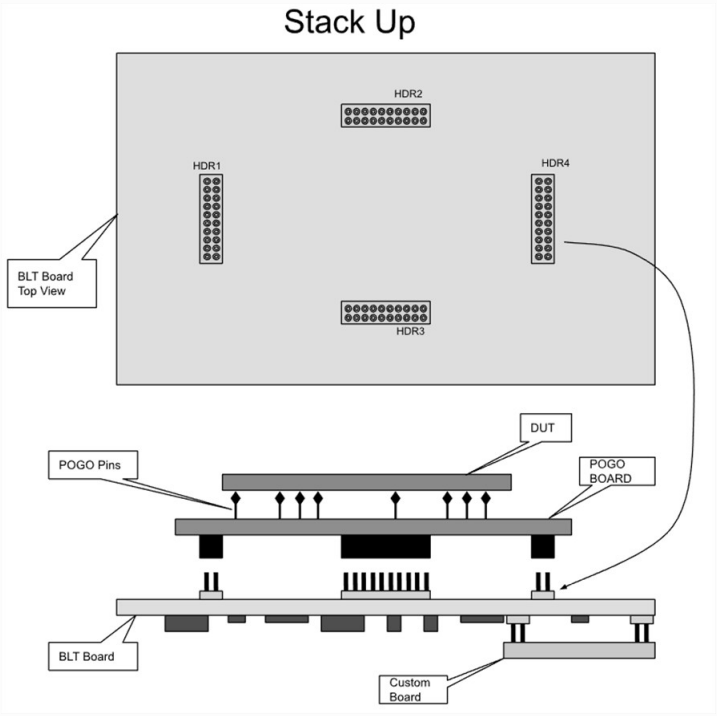
In Addition to the MAX11311 each Header provides additional functions,

1] VBAT Emulator, sinking and sourcing current, with current measurement, 1-10V.
VBUS (5V) Supply with current measurement.
Additional Supply 1-5V.
UART (with level shifter)

2] I2C (with level shifter)

3] Segger JTAG (4 wire)
USB Slave to PC or Teensy

4] Connections to expansion Custom PCB
Custom PCB - create specific test measurement or stimulous circuits
- Connections for Power (3,3V, VBAT, VBUS, 6V)
- I2C and UART connections to Teensy



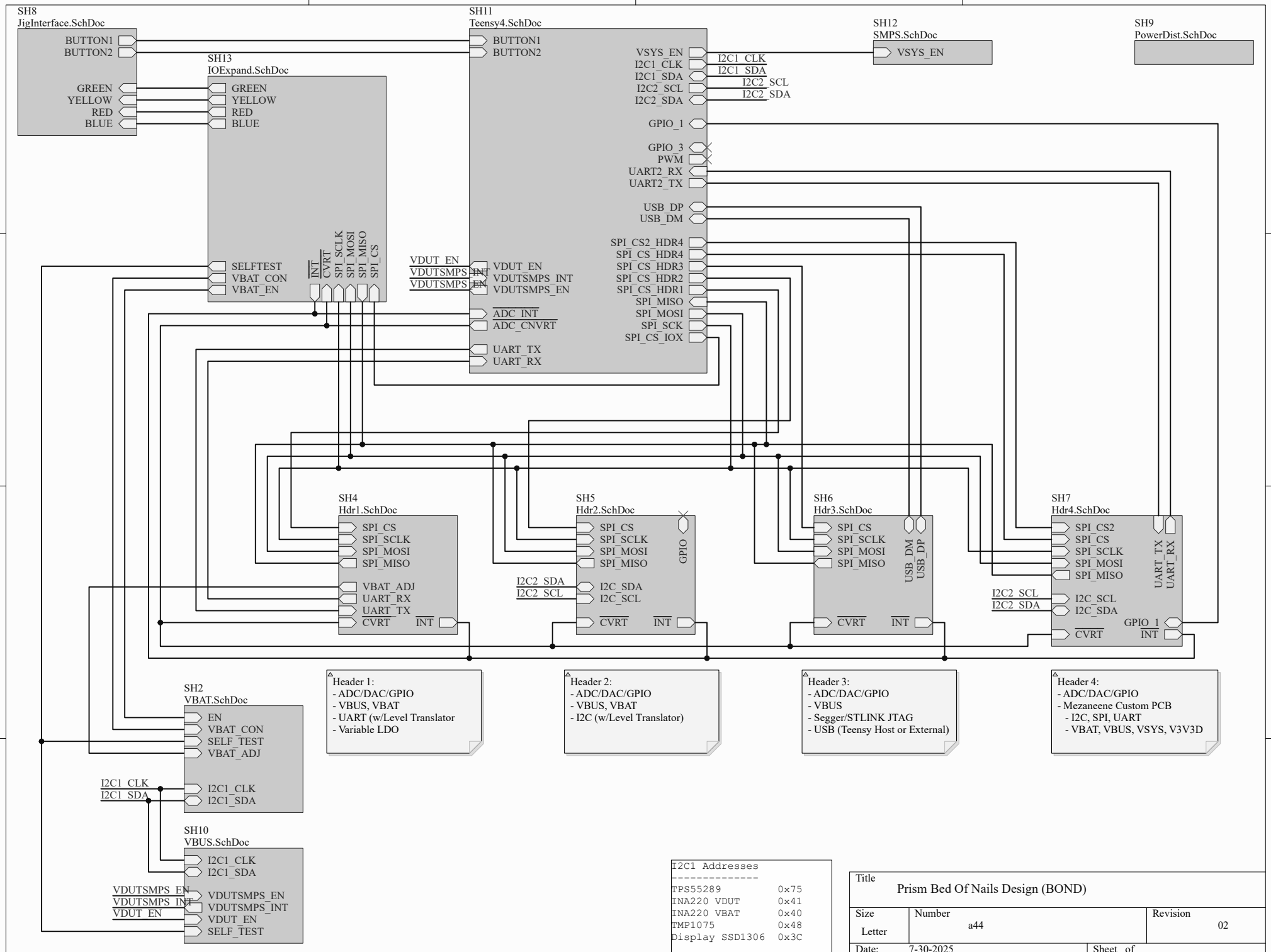
Stack Up Notes

1) The BLT board provides test measurements and stiumlous.

2) The Pogo Board interfaces the BLT board to the Device Under Test (DUT) via spring loaded probes.

Various DUTs can be supported by one BLT board by using different Pogo Boards.

Title: BOND Block Diagram and Notes		
Size: Letter	Number: a44	Revision: 02
Date: 7-30-2025		Sheet of
File: BlockDiag.SchDoc		Drawn By: Sistemi


SH8
JigInterface.SchDoc
BUTTON1
BUTTON2
GREEN
YELLOW
RED
BLUE
SH13
IOExpand.SchDoc
SELFTEST
VBAT_CON
VBAT_EN
INT
CVRT
SPI_SCLK
SPI_MOSI
SPI_MISO
SPI_CS
SH11
Teensy4.SchDoc
VDUT_EN
VDUTSMPS_INT
VDUTSMPS_EN
ADC_INT
ADC_CNVRT
UART_TX
UART_RX
VSYS_EN
I2C1_CLK
I2C1_SDA
I2C2_SCL
I2C2_SDA
GPIO_1
GPIO_3
PWM
UART2_RX
UART2_TX
USB_DP
USB_DM
SPI_CS2_HDR4
SPI_CS_HDR4
SPI_CS_HDR3
SPI_CS_HDR2
SPI_CS_HDR1
SPI_MISO
SPI_MOSI
SPI_SCK
SPI_CS_IOX
SH12
SMPS.SchDoc
VSYS_EN
SH9
PowerDist.SchDoc
SH4
Hdr1.SchDoc
SPI_CS
SPI_SCLK
SPI_MOSI
SPI_MISO
VBAT_ADJ
UART_RX
UART_TX
CVRT
INT
SH5
Hdr2.SchDoc
GPIO
I2C2_SDA
I2C2_SCL
I2C_SDA
I2C_SCL
SH6
Hdr3.SchDoc
USB_DM
USB_DP
SH7
Hdr4.SchDoc
SPI_CS2
UART_TX
UART_RX
GPIO_1
Header 1:
- ADC/DAC/GPIO
- VBUS, VBAT
- UART (w/Level Translator
- Variable LDO
Header 2:
- ADC/DAC/GPIO
- VBUS, VBAT
- I2C (w/Level Translator)
Header 3:
- ADC/DAC/GPIO
- VBUS
- Segger/STLINK JTAG
- USB (Teensy Host or External)
Header 4:
- ADC/DAC/GPIO
- Mezaneene Custom PCB
- I2C, SPI, UART
- VBAT, VBUS, VSYS, V3V3D
SH2
VBAT.SchDoc
EN
VBAT_CON
SELF_TEST
VBAT_ADJ
SH10
VBUS.SchDoc
VDUTSMPS_EN
VDUTSMPS_INT
VDUT_EN
SELF_TEST
I2C1 Addresses
TPS55289 0x75
INA220 VDUT 0x41
INA220 VBAT 0x40
TMP1075 0x48
Display SSD1306 0x3C
Title
Prism Bed Of Nails Design (BOND)
Size
Letter
Number
a44
Revision
02
Date: 7-30-2025
Sheet of
File: Top.SchDoc
Drawn By: Sistemi

Teensy Powered by VBUS

U1

Adafruit Industries TEENSY41

0	GND	Vin	47
1	D0/RX1/CS1/CRX2	GND	46
2	D1/TX1/MISO1/CTX2	3.3V	45
3	D2/OUT2	D23/A9/CRX1/MCLK1	44
4	D3/LRCLK2	D22/A8/CTX1	43
5	D4/BCLK2	D21/A7/RX5/BCLK1	42
6	D5/IN2	D20/A6/TX5/LRCLK1	41
7	D6/OUT1D	D19/A5/SCL	40
8	D7/RX2/OUT1A	D18/A4/SDA	39
9	D8/TX2/IN1	D17/A3/TX4/SDA1	38
10	D9/OUT1C	D16/A2/RX4/SCL1	37
11	D10/CS/MQSR	D15/A1/RX3/SPDIF_IN	36
12	D11/MOSI/CTX1	D14/A0/TX3/SPDIF_OUT	35
13	D12/MISO/MQSL	D13/(LED)/SCK	34
14	3.3V	GND	33
15	D24/A10/TX6/SCL2	D41/A17	32
16	D25/A11/RX6/SDA2	D40/A16	31
17	D26/A12/MOSI1	D39/A15/MISO1/OUT1A	30
18	D27/A13/SCK1	D38/A14/CS1/IN1	29
19	D28/RX7	D37/CS	28
20	D29/TX7	D36/CS	27
21	D30/CRX3	D35/TX8	26
22	D31/CTX3	D34/RX8	25
23	D32/OUT1B	D33/MCLK2	24
48	5V		
49	USB_HOST_D-	VUSB	58
50	USB_HOST_D+		
51	GND		
52	GND		
53	ON/OFF	ETH_TX+	59
54	PROGRAM	ETH_TX-	60
55	GND	ETH_RX+	61
56	3.3V	ETH_RX-	62
57	VBAT	ETH_LED	63
		GND	64

V3V3D

R3 10 KΩ

TEMP_ALERT

BUTTON1

BUTTON2

ADC_CNVRT

ADC_INT

ADC_INT

A_V6V

A_V5V

SPI_MOSI

SPI_SCK

PWM

GPIO_3

VSYS_EN

GPIO_1

USB_DM

USB_DP

GND

GND

GND

A_V3V3A

A_V3V3D

UART2_RX

UART2_TX

I2C1_CLK

I2C1_SDA

I2C2_SDA

I2C2_SCL

UART_RX

UART_TX

VDUTSMPS_EN

VDUT_EN

VDUTSMPS_INT

SPI_MISO

SPI_CS_HDR1

SPI_CS_HDR2

SPI_CS_HDR3

SPI_CS_HDR4

SPI_CS2_HDR4

SPI_CS_IOX

V3V3D

R1 2 KΩ

R2 2 KΩ

Dedicated to this PCB

I2C1_CLK

I2C1_SDA

V3V3D

R4 2 KΩ

R5 2 KΩ

I2C2_SDA

I2C2_SCL

Dedicated to DUT

V3V3D

U22

I2C1_SDA 1	SDA	V+	8
I2C1_CLK 2	SCL	A0	7
TEMP_ALERT 3	ALERT	A1	6
4,9 GND	GND	A2	5

Texas Instruments TMP1075DSGR

I2C ADDR 0x48

GND

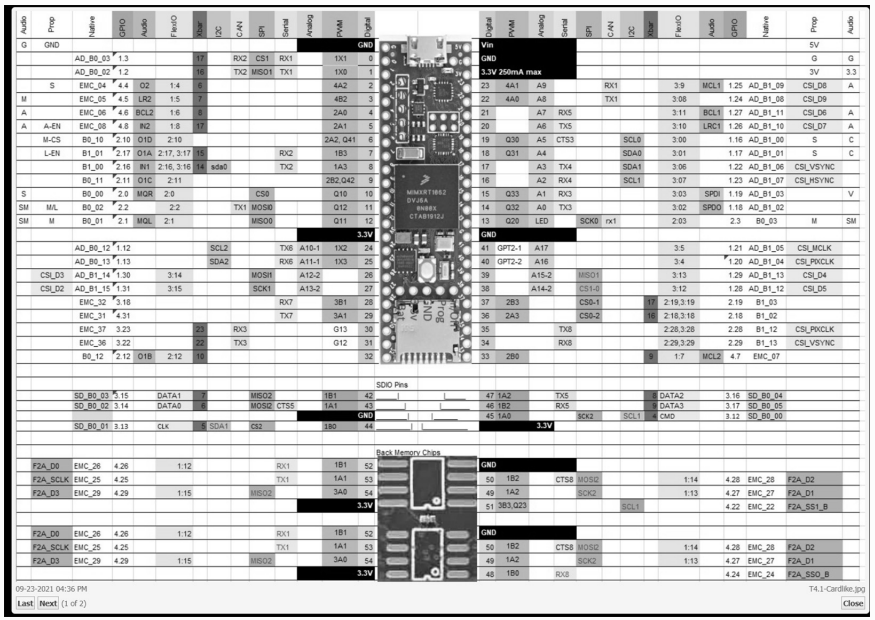
Debug Header

J1

I2C1_CLK	1	2	SPI_SCK
I2C1_SDA	3	4	SPI_MOSI
I2C2_SDA	5	6	SPI_MISO
I2C2_SCL	7	8	SPI_CS_HDR1
UART_RX	9	10	SPI_CS_HDR2
UART_TX	11	12	SPI_CS_HDR3
Spare to wire	13	14	SPI_CS_HDR4
	15	16	SPI_CS2_HDR4
	17	18	ADC_INT
	19	20	

Würth Elektronik 61302021121

GND



SELF TEST Voltages

VSYS V5V V3V3A V3V3D

R6 20 KΩ R7 20 KΩ R8 20 KΩ R9 20 KΩ

A_V6V A_V5V A_V3V3A A_V3V3D

R10 10 KΩ R11 10 KΩ R12 10 KΩ R13 10 KΩ

GND

J2

4	I2C1_SDA
3	I2C1_CLK
2	
1	

4x1 Header

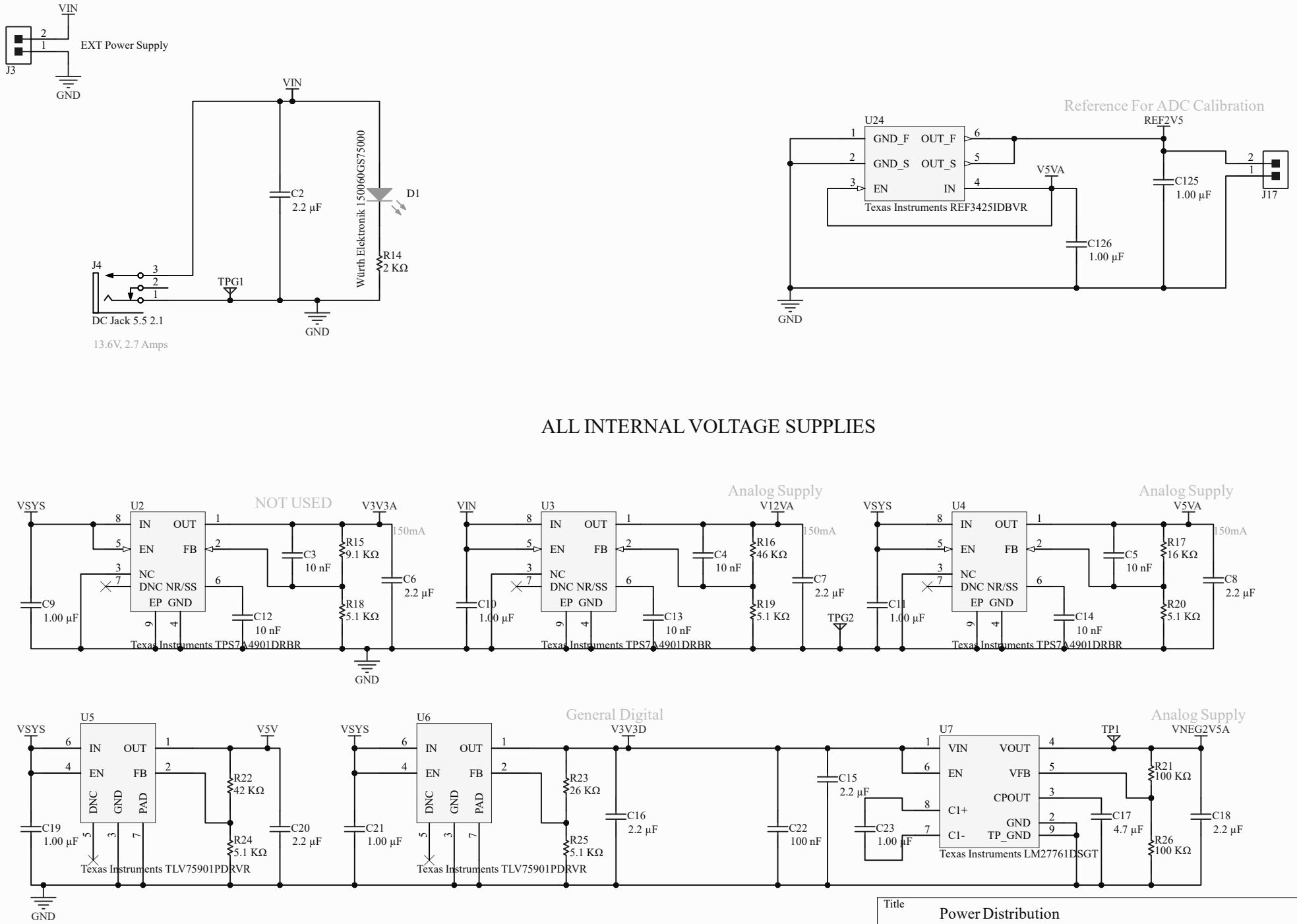
V3V3D

C1 1.00 µF

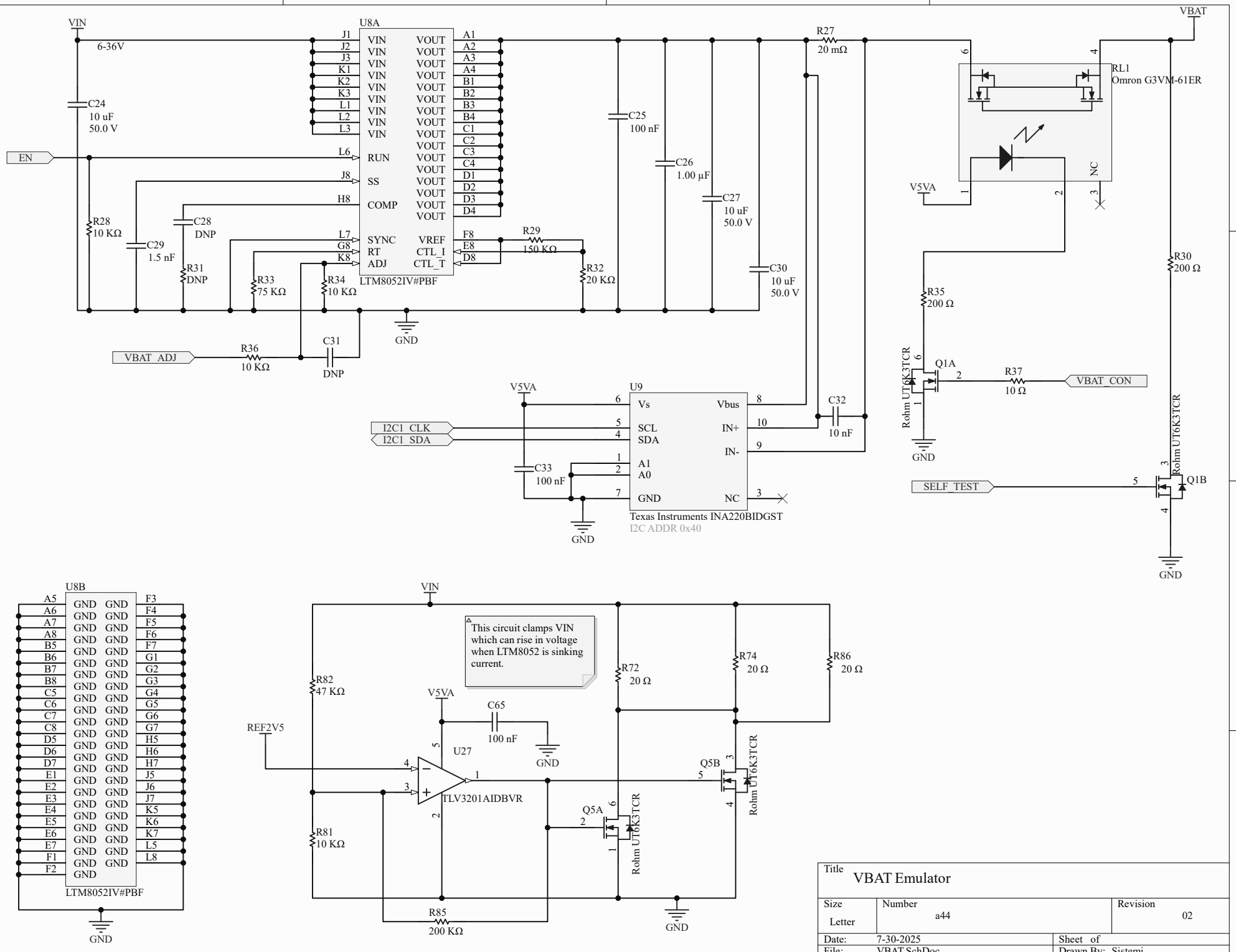
https://www.buydisplay.com/i2c-white-1-3-inch-oled-display-module-128x64-arduino-raspberry-pi

ER-OLEDM013-1W-I2C

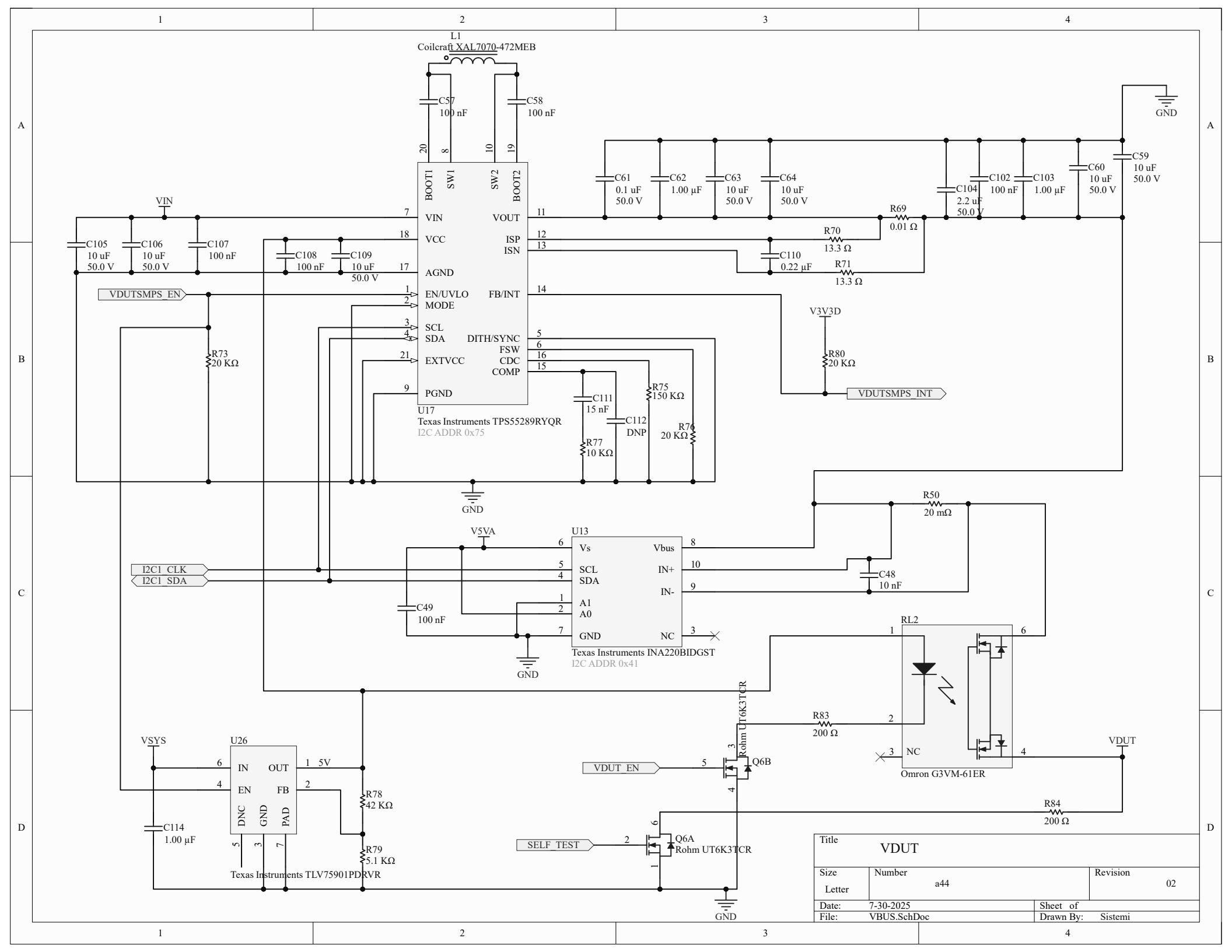
Title	Teensy 4.1		
Size: Letter	Number: a44		Revision: 02
Date: 7-30-2025		Sheet of	
File: Teensy4.SchDoc		Drawn By: Sistemi	

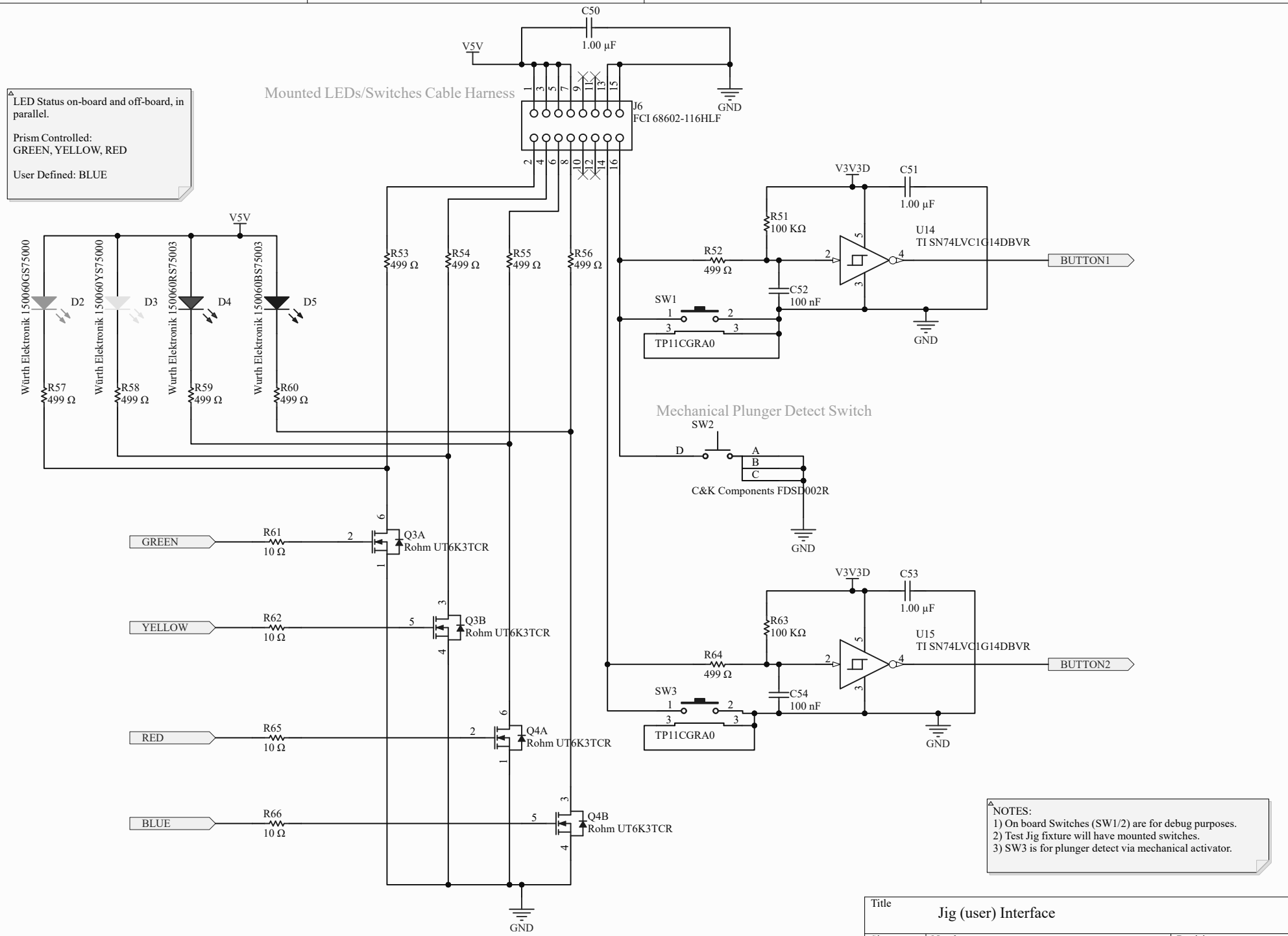


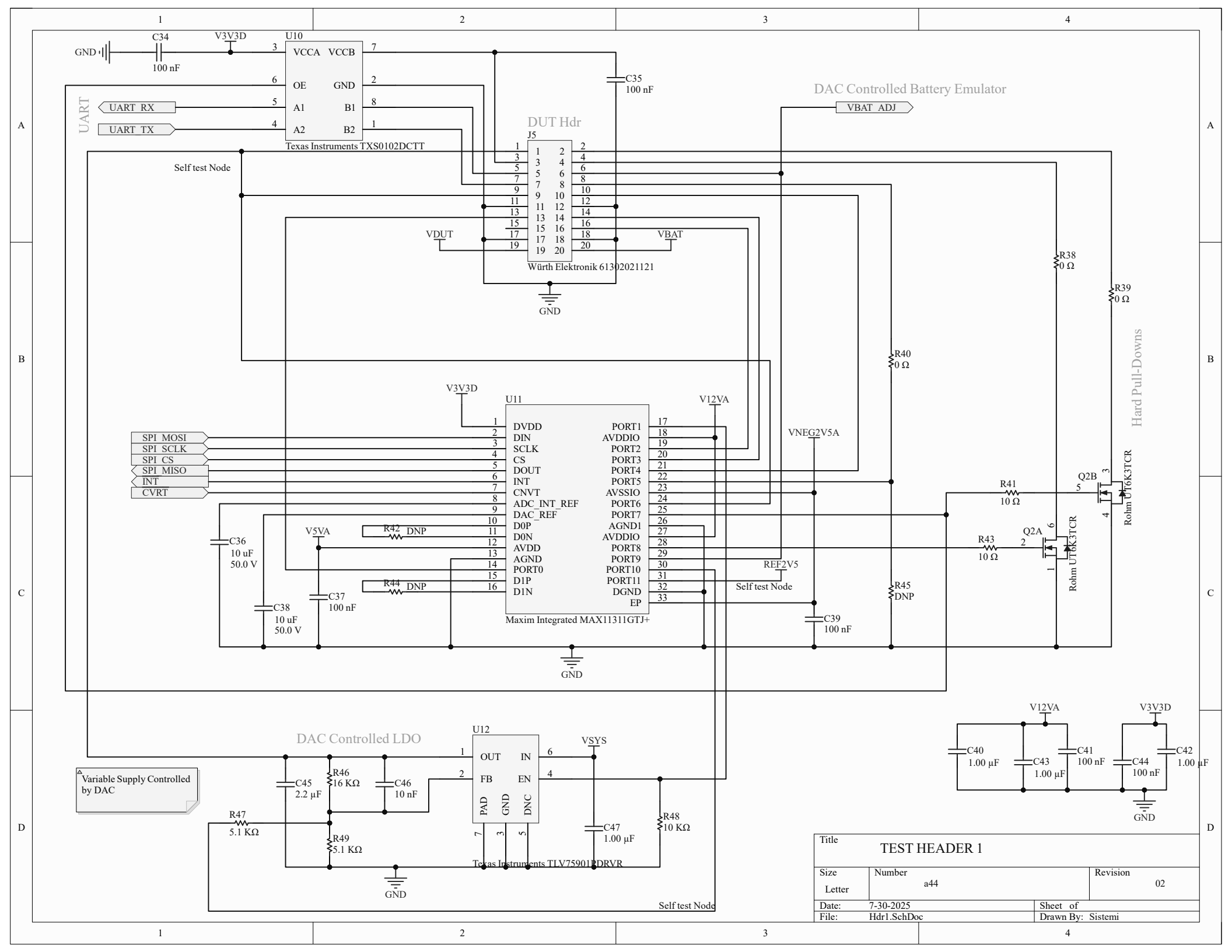
Title	Power Distribution	
Size: Letter	Number: a44	Revision: 02
Date: 7-30-2025		Sheet of
File: PowerDist.SchDoc		Drawn By: Sistemi

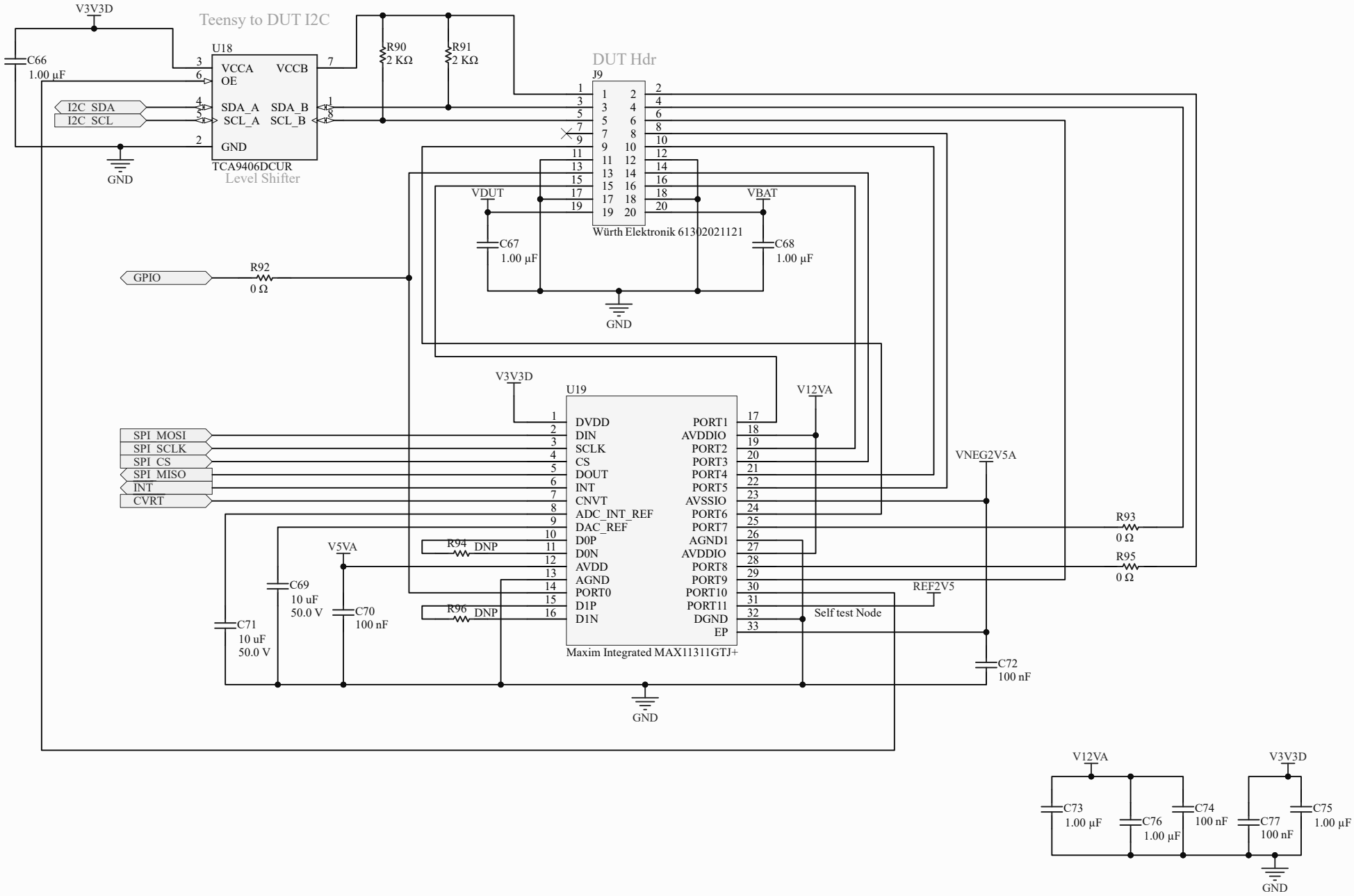


Title	VBAT Emulator	
Size: Letter	Number: a44	Revision: 02
Date: 7-30-2025		Sheet of
File: VBAT.SchDoc		Drawn By: Sistemi

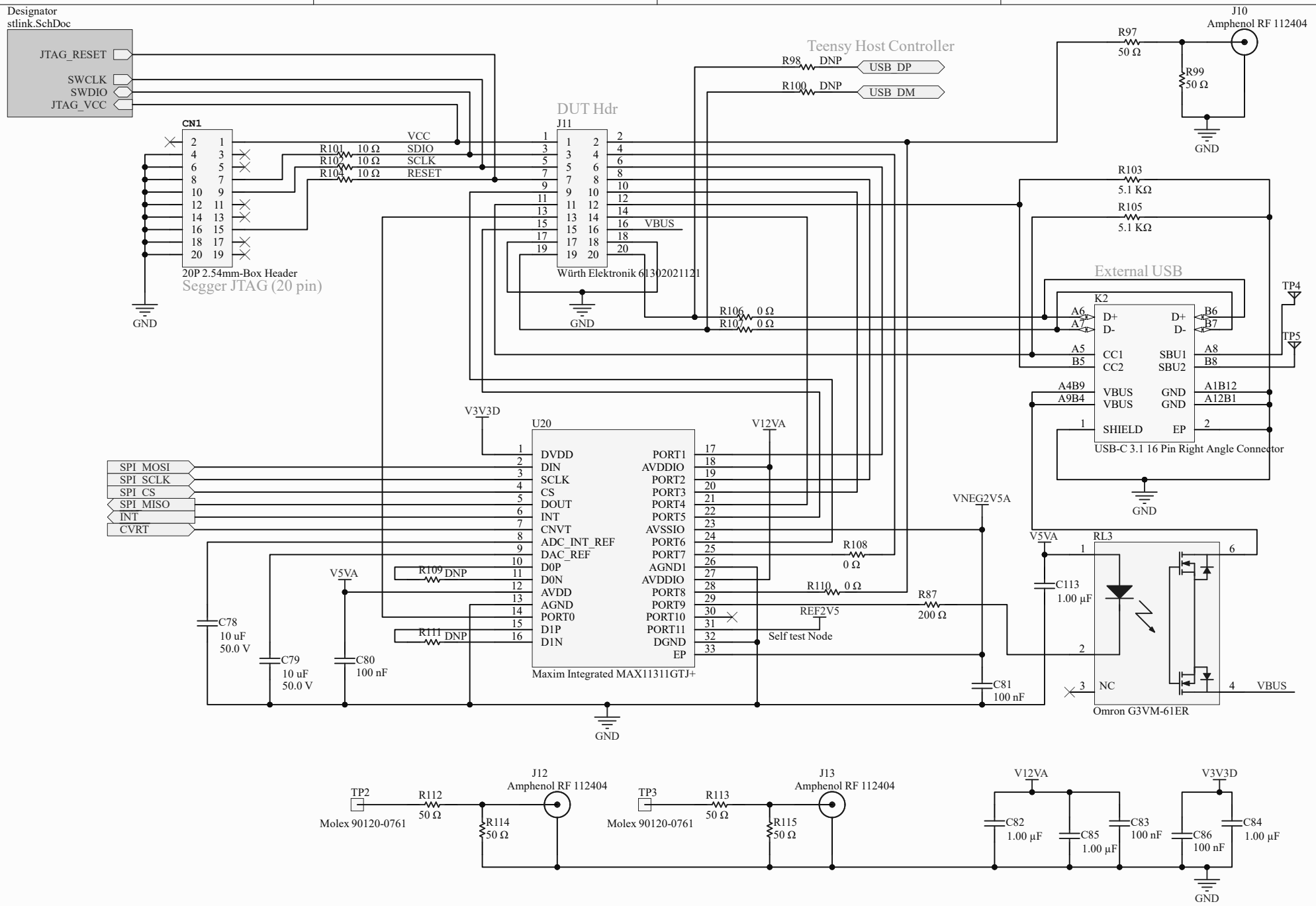

L1
Coilcraft XAL7070-472MEB
C57
100 nF
C58
100 nF
BOOT1
SW1
SW2
BOOT2
VIN
VCC
AGND
EN/UVLO
MODE
SCL
SDA
EXTVCC
PGND
VOUT
ISP
ISN
FB/INT
DITH/SYNC
FSW
CDC
COMP
U17
Texas Instruments TPS55289RYQR
I2C ADDR 0x75
C61
0.1 uF
50.0 V
C62
1.00 µF
C63
10 uF
50.0 V
C64
10 uF
50.0 V
C104
2.2 uF
50.0 V
C102
100 nF
C103
1.00 µF
C60
10 uF
50.0 V
C59
10 uF
50.0 V
GND
R69
0.01 Ω
R70
13.3 Ω
R71
13.3 Ω
C110
0.22 µF
C105
10 uF
50.0 V
C106
10 uF
50.0 V
C107
100 nF
C108
100 nF
C109
10 uF
50.0 V
VDUTSMPS_EN
R73
20 KΩ
V3V3D
R80
20 KΩ
VDUTSMPS_INT
C111
15 nF
C112
DNP
R75
150 KΩ
R76
20 KΩ
R77
10 KΩ
R50
20 mΩ
V5VA
U13
Vs
SCL
SDA
A1
A0
GND
Vbus
IN+
IN-
NC
Texas Instruments INA220BIDGST
I2C ADDR 0x41
I2C1_CLK
I2C1_SDA
C48
10 nF
C49
100 nF
RL2
Omron G3VM-61ER
R83
200 Ω
VDUT
R84
200 Ω
VSYS
U26
IN
EN
DNC
GND
PAD
OUT
FB
5V
C114
1.00 µF
R78
42 KΩ
R79
5.1 KΩ
Texas Instruments TLV75901PDRVR
VDUT_EN
Q6B
Rohm UT6K3TCR
SELF_TEST
Q6A
Rohm UT6K3TCR
Title
VDUT
Size
Letter
Number
a44
Revision
02
Date:
7-30-2025
Sheet of
File:
VBUS.SchDoc
Drawn By:
Sistemi

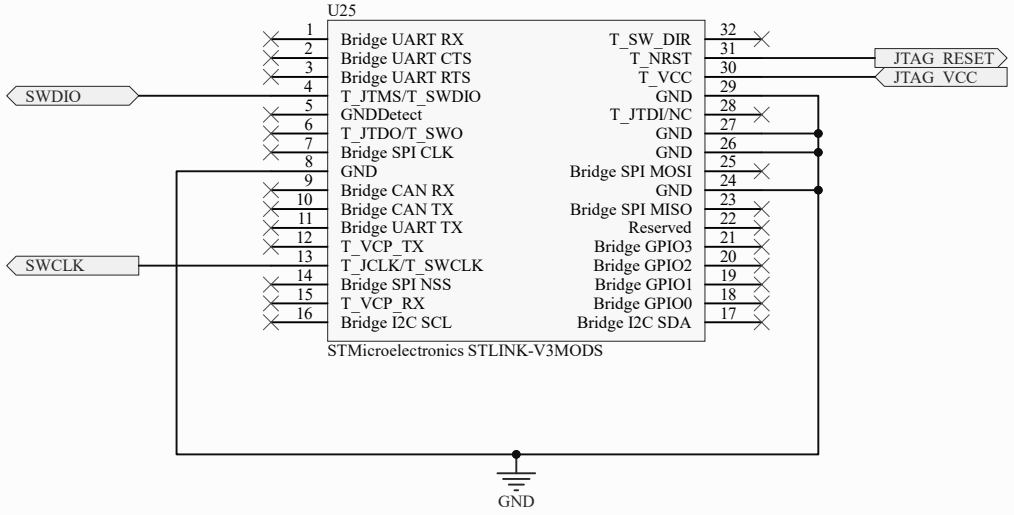

C50
1.00 µF
V5V
GND
Mounted LEDs/Switches Cable Harness
J6
FCI 68602-116HLF
LED Status on-board and off-board, in parallel.
Prism Controlled:
GREEN, YELLOW, RED
User Defined: BLUE
V3V3D
C51
1.00 µF
R51
100 KΩ
U14
TI SN74LVC1G14DBVR
R52
499 Ω
BUTTON1
C52
100 nF
SW1
TP11CGRA0
R53
499 Ω
R54
499 Ω
R55
499 Ω
R56
499 Ω
D2
D3
D4
D5
Würth Elektronik 150060GS75000
Würth Elektronik 150060YS75000
Würth Elektronik 150060RS75003
Wurth Elektronik 150060BS75003
R57
499 Ω
R58
499 Ω
R59
499 Ω
R60
499 Ω
Mechanical Plunger Detect Switch
SW2
C&K Components FDSD002R
GREEN
R61
10 Ω
Q3A
Rohm UT6K3TCR
YELLOW
R62
10 Ω
Q3B
Rohm UT6K3TCR
RED
R65
10 Ω
Q4A
Rohm UT6K3TCR
BLUE
R66
10 Ω
Q4B
Rohm UT6K3TCR
V3V3D
C53
1.00 µF
R63
100 KΩ
U15
TI SN74LVC1G14DBVR
R64
499 Ω
BUTTON2
C54
100 nF
SW3
TP11CGRA0
NOTES:
1) On board Switches (SW1/2) are for debug purposes.
2) Test Jig fixture will have mounted switches.
3) SW3 is for plunger detect via mechanical activator.
Title
Jig (user) Interface
Size
Letter
Number
a44
Revision
02
Date:
7-30-2025
Sheet of
File:
JigInterface.SchDoc
Drawn By:
Sistemi


UART
UART_RX
UART_TX
U10
VCCA
VCCB
OE
GND
A1
B1
A2
B2
Texas Instruments TXS0102DCTT
C34
100 nF
V3V3D
C35
100 nF
DUT Hdr
J5
Würth Elektronik 61302021121
Self test Node
VDUT
VBAT
DAC Controlled Battery Emulator
VBAT_ADJ
R38
0 Ω
R39
0 Ω
R40
0 Ω
Hard Pull-Downs
U11
DVDD
DIN
SCLK
CS
DOUT
INT
CNVT
ADC_INT_REF
DAC_REF
D0P
D0N
AVDD
AGND
PORT0
D1P
D1N
PORT1
AVDDIO
PORT2
PORT3
PORT4
PORT5
AVSSIO
PORT6
PORT7
AGND1
AVDDIO
PORT8
PORT9
PORT10
PORT11
DGND
EP
Maxim Integrated MAX11311GTJ+
V12VA
VNEG2V5A
SPI_MOSI
SPI_SCLK
SPI_CS
SPI_MISO
INT
CVRT
C36
10 uF
50.0 V
C38
10 uF
50.0 V
V5VA
R42 DNP
R44 DNP
C37
100 nF
REF2V5
Self test Node
C39
100 nF
R45
DNP
R41
10 Ω
R43
10 Ω
Q2B
Q2A
Rohm UT6K3TCR
Rohm UT6K3TCR
DAC Controlled LDO
U12
OUT
FB
PAD
GND
DNC
IN
EN
Texas Instruments TLV75901PDRVR
VSYS
Variable Supply Controlled by DAC
C45
2.2 µF
R46
16 KΩ
C46
10 nF
R47
5.1 KΩ
R49
5.1 KΩ
C47
1.00 µF
R48
10 KΩ
Self test Node
C40
1.00 µF
C43
1.00 µF
C41
100 nF
C44
100 nF
C42
1.00 µF
Title
TEST HEADER 1
Size
Letter
Number
a44
Revision
02
Date:
7-30-2025
File:
Hdr1.SchDoc
Sheet of
Drawn By:
Sistemi

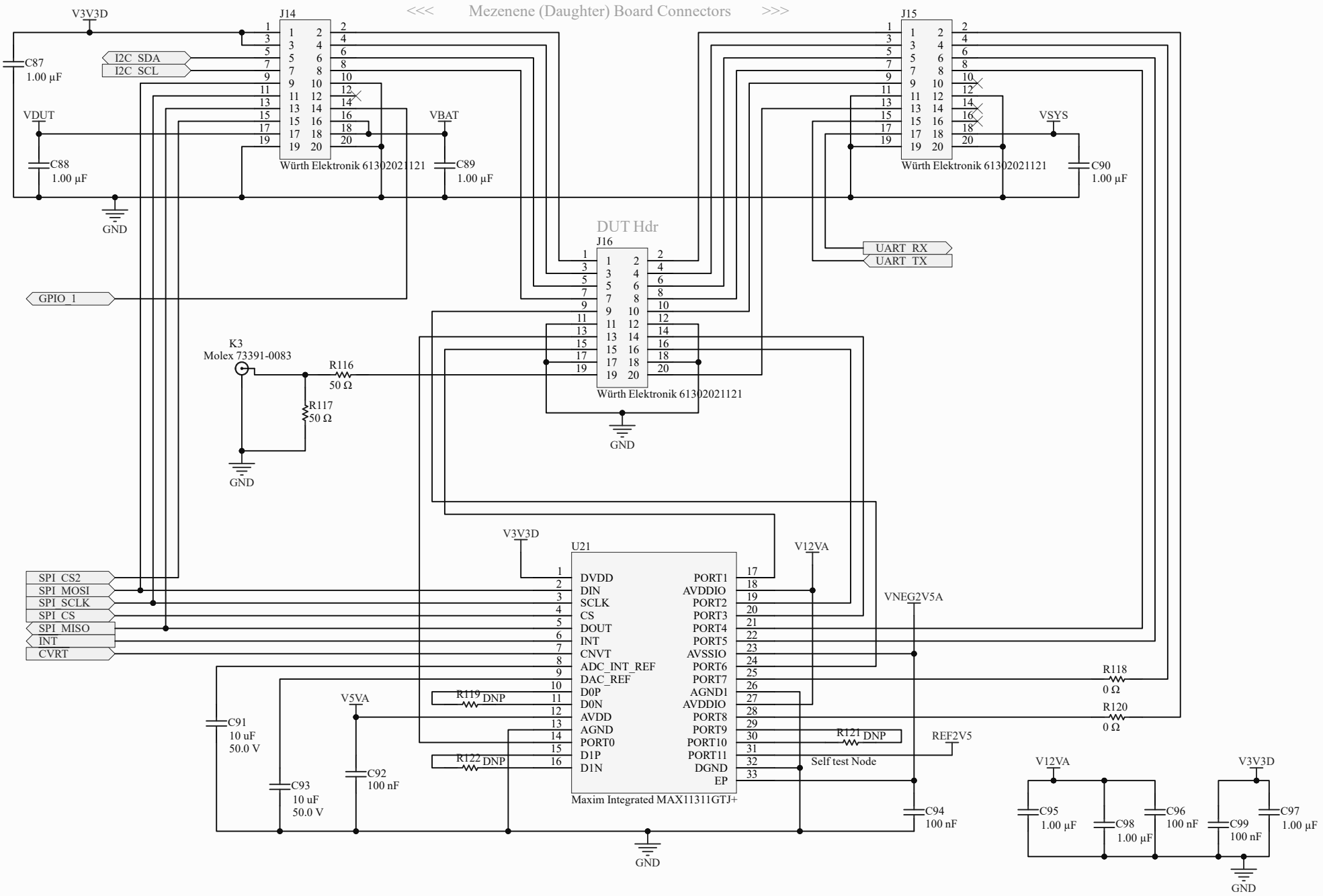


Title	TEST HEADER 2	
Size: Letter	Number: a44	Revision: 01
Date: 7-30-2025		Sheet of
File: Hdr2.SchDoc		Drawn By: Sistemi

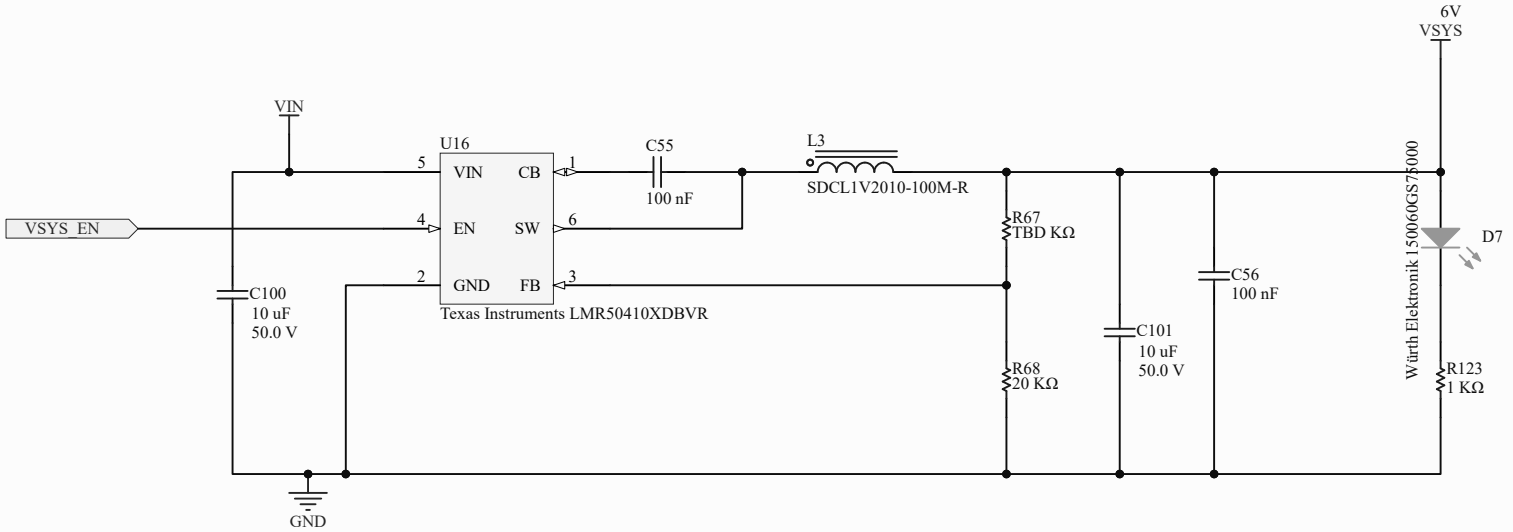

Designator
stlink.SchDoc
JTAG_RESET
SWCLK
SWDIO
JTAG_VCC
CN1
20P 2.54mm-Box Header
Segger JTAG (20 pin)
R101 10 Ω SDIO
R102 10 Ω SCLK
R104 10 Ω RESET
VCC
GND
DUT Hdr
J11
Würth Elektronik 61302021121
VBUS
Teensy Host Controller
R98 DNP
R100 DNP
USB_DP
USB_DM
R106 0 Ω
R107 0 Ω
J10
Amphenol RF 112404
R97
50 Ω
R99
50 Ω
R103
5.1 KΩ
R105
5.1 KΩ
External USB
K2
USB-C 3.1 16 Pin Right Angle Connector
TP4
TP5
V3V3D
U20
DVDD
DIN
SCLK
CS
DOUT
INT
CNVT
ADC_INT_REF
DAC_REF
D0P
D0N
AVDD
AGND
PORT0
D1P
D1N
PORT1
AVDDIO
PORT2
PORT3
PORT4
PORT5
AVSSIO
PORT6
PORT7
AGND1
AVDDIO
PORT8
PORT9
PORT10
PORT11
DGND
EP
Maxim Integrated MAX11311GTJ+
V12VA
SPI_MOSI
SPI_SCLK
SPI_CS
SPI_MISO
INT
CVRT
R109 DNP
R111 DNP
R108 0 Ω
R110 0 Ω
REF2V5
Self test Node
R87 200 Ω
VNEG2V5A
V5VA
RL3
Omron G3VM-61ER
C78 10 uF 50.0 V
C79 10 uF 50.0 V
C80 100 nF
C81 100 nF
C113 1.00 µF
J12
Amphenol RF 112404
J13
Amphenol RF 112404
TP2
TP3
Molex 90120-0761
R112 50 Ω
R113 50 Ω
R114 50 Ω
R115 50 Ω
C82 1.00 µF
C85 1.00 µF
C83 100 nF
C86 100 nF
C84 1.00 µF
Title
TEST HEADER 3
Size
Letter
Number
a44
Revision
02
Date: 7-30-2025
File: Hdr3.SchDoc
Sheet of
Drawn By: Sistemi



Title	STLINK-V3MODS		
Size: Letter	Number: a44		Revision: 02
Date: 7-30-2025		Sheet of	
File: stlink.SchDoc		Drawn By: Sistemi	



Title	TEST HEADER 4	
Size: Letter	Number: a44	Revision: 01
Date: 7-30-2025		Sheet of
File: Hdr4.SchDoc		Drawn By: Sistemi



Title	System SMPS (VSYS)	
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Date: 7-30-2025		Sheet of
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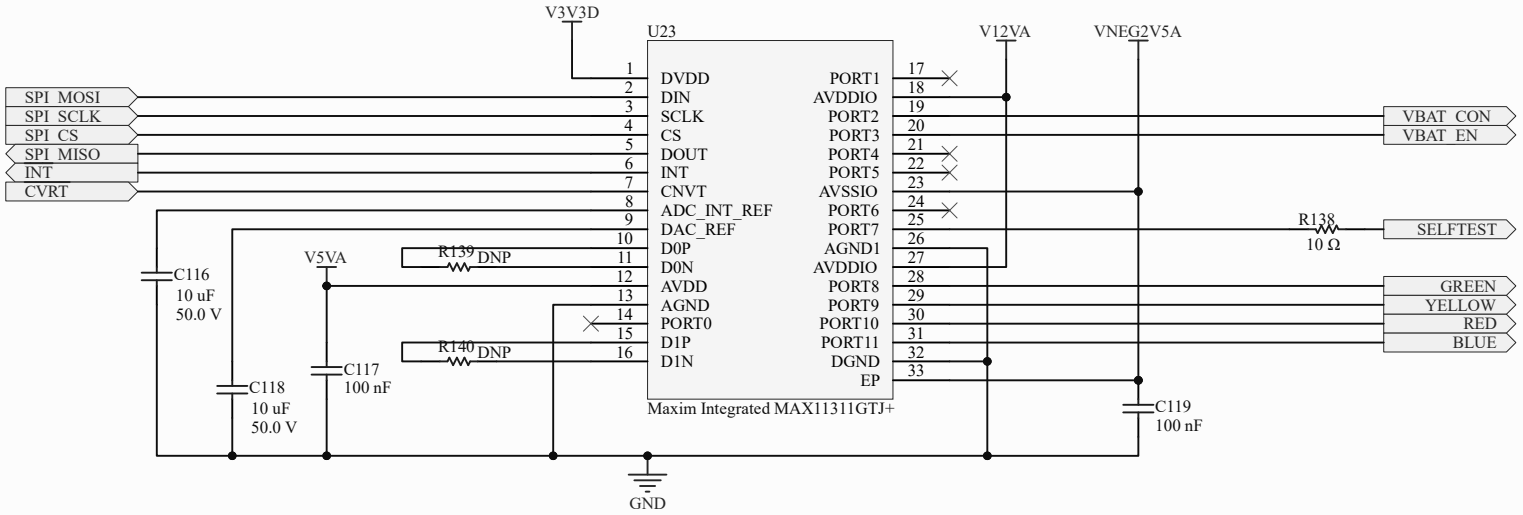

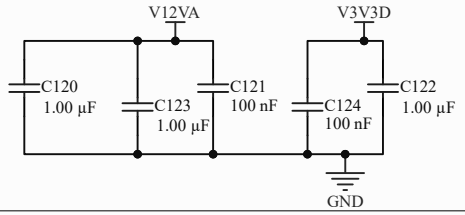

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