Battery Life Modelling, Part 2

Validating Battery Models with P1125

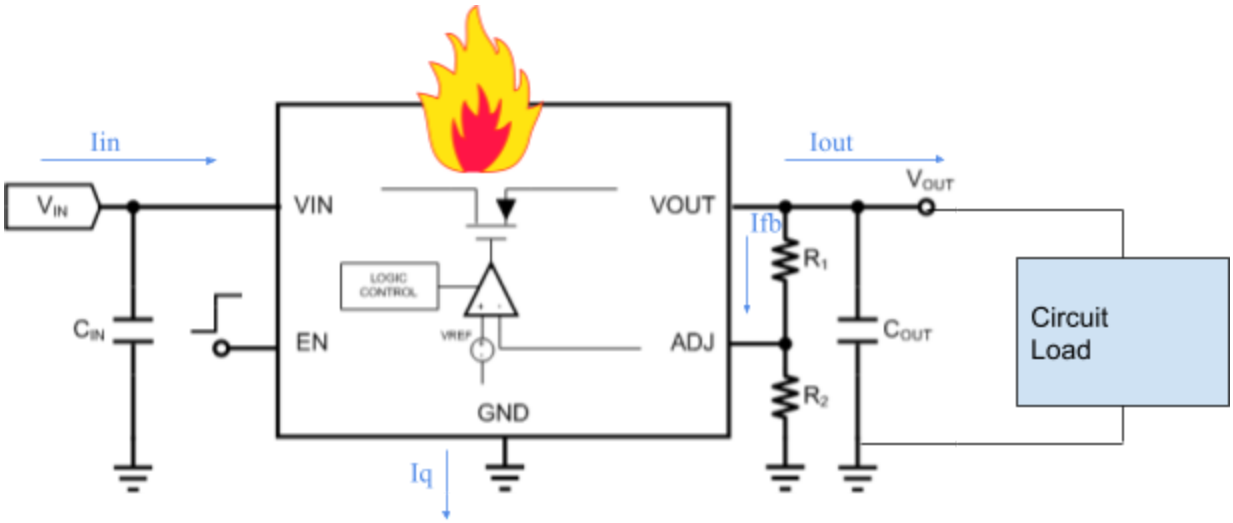
Part 2 of battery life modeling is understanding the impact of the DC/DC design architecture. The DC/DC design takes the DC battery voltage and converts it to levels required by the design. For example, a lithium battery voltage varies from ~4V (full) to ~3V (empty), whereas the embedded microcontroller may be powered from a fixed 1.8V level, regardless of battery voltage.

There are two major types of DC/DC conversion, Linear (Low Drop Out) Regulators, often referred to as "LDOs", and Switched Mode Power Supplies (SMPS). LDOs can only drop (step down) the voltage from input to output. SMPS can either be step down (buck) or step up (boost), or both. There are also "switched capacitor" converters, which are not covered in this paper, but are similar to SMPS.

This paper will show how to model load currents from the output of the DC/DC converters to the Battery. All the loads in the product need to be referred back to the battery so the model can predict the battery life.

LDOs

LDOs are the simplest form of DC/DC conversion. These parts can be as simple as a 3-terminal device. Here a 5 terminal device is shown, with enable (EN) and adjust (ADJ, sometimes labelled FB (feedback)).



The LDO function is to step down the voltage from V_{in} to V_{out}, where V_{out} must be lower than V_{in} by an amount called the "drop out" voltage (V_{do}), which is given in the LDO datasheet.

$$V_{out} \leq V_{in} - V_{do} \quad (1)$$

Without going into detail about LDO design theory, we state the following that relates all the currents,

$$I_{in} = I_q + I_{fb} + I_{out}$$

I_{fb} is the feedback pin (or adjust pin) current and it is simply V_{out} / (R_1 + R_2). This current is generally small compared to the load current (I_{out}).

I_q is called the quiescent current of the LDO. It's the current required to run the circuit that is inside the LDO. That circuit is usually a voltage reference, an op amp and other logic. The quiescent current usually affects the LDO's performance in the areas of power supply rejection ratio (PSR), transient response time to load current changes, output voltage noise, and other factors. The higher the quiescent current, generally the better the LDO performs in these areas. However, for battery powered devices, one desires low quiescent LDOs, so that the LDO quiescent current is much less than the Circuit Load current in its standby or sleep state. One must carefully read the LDO datasheet to understand the quiescent current specification.

When the product is in active mode(s) we shall assume that the load current is much greater, thus,

$$I_{out} \gg I_q,\ I_{out} \gg I_{fb}$$
$$I_{in} \approx I_{out} \qquad (2)$$

Equation (2) is an acceptable rule of thumb when modeling LDOs in the active state.

The efficiency of the LDO is the usable power at the output divided by the input power,

$$Eff = \frac{P_{out}}{P_{in}}$$
$$Eff = \frac{I_{out} \cdot V_{out}}{I_{in} \cdot V_{in}}$$

And using the relationship between input and output current (2),

$$Eff \approx \frac{V_{out}}{V_{in}}$$

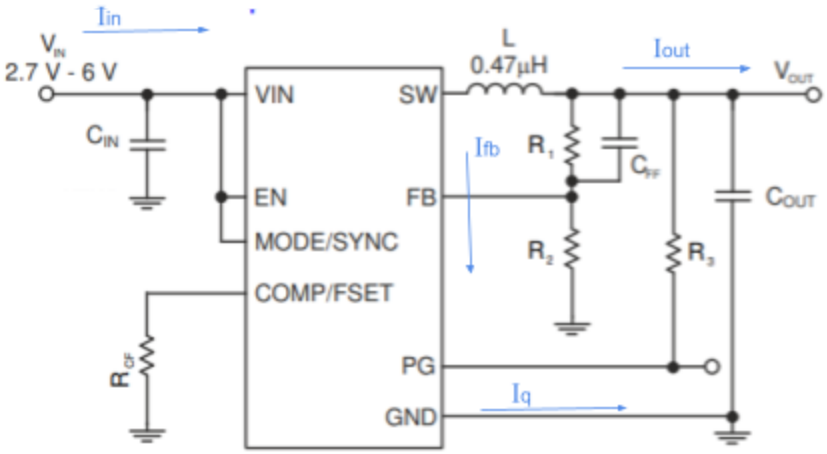
And recall V_{out} has to follow (1), which means the efficiency of the LDO is always less than 100%. The larger the ratio between V_{out} and V_{in}, the less efficient the LDO is. Where does the power go? ***Heat***. The pass transistor inside the LDO acts like a variable resistor, dropping the input voltage such that the output voltage is maintained at a constant level, as determined by the feedback (or adjust) pin. Therefore it is undesirable to drop a large voltage across an LDO, especially for a large current, because the LDO will get hot and be inefficient.

LDO Model Implications

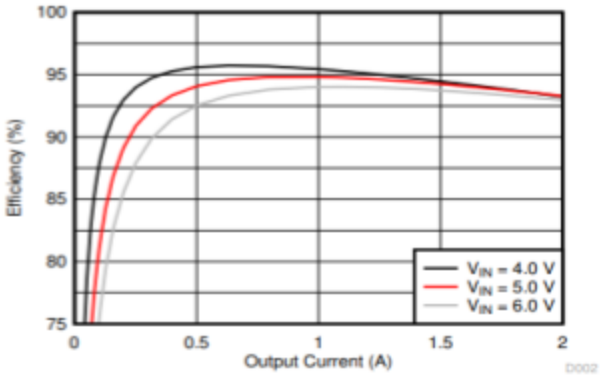
- Efficiency
  - Determined by the V_{out} / V_{in} ratio
  - For best results, drop as little voltage as possible while respecting the LDO dropout voltage
- Active Load State
  - The smaller currents can be ignored
  - $I_{in} \approx I_{out}$
- Standby State
  - LDO quiescent current should be considered
  - $I_{in} \approx I_{out} + I_q$

SMPS

The SMPS DC/DC converter is more complicated than the LDO. It also generally takes more board space, more components and costs more to implement. But the upside is high efficiency across a wider operating range of input and output voltage conditions. Below is a typical simplified schematic for a SMPS, with the same currents marked as was done for the LDO.



Simplified Schematic



Efficiency versus I_{OUT}, V_{OUT} = 3.3 V

The same starting point will be used, relating all the currents,

$$I_{in} = I_q + I_{fb} + I_{out}$$

These currents have the same meaning as for the LDO. And for the active state, we can make the same simplification,

$$I_{out} \gg I_q,\ I_{out} \gg I_{fb}$$

How the SMPS is different from the LDO, is in its efficiency, whereas we could derive the efficiency for the LDO, here the efficiency is given (see plot above), for varying load currents, and input/output voltage conditions. We are interested in an expression for the input current as a function out the load current. From the plot above, and for simplification, we will assume that the efficiency is 100% for our active current, thus,

$$Eff = \frac{I_{out} \cdot V_{out}}{I_{in} \cdot V_{in}}$$

$$1 = \frac{I_{out} \cdot V_{out}}{I_{in} \cdot V_{in}}$$

$$I_{in} = \frac{I_{out} \cdot V_{out}}{V_{in}} \quad (3)$$

Considering a SMPS stepping voltage down, equation (3) tells us that the input current will be less than the output current by the ratio of V_{out} / V_{in}. Recall from Battery Life Modelling 101 that the battery is a bucket of charge and that charge is drained by the current (rate of charge flowing). If the current is lower, then the battery will last longer! Also, because the SMPS uses a different approach than the LDO, it is far more efficient at providing output power without heating up as much as an LDO would.

What happens at low load currents? As can be seen from the Efficiency plot above, the efficiency drops off VERY quickly. What's happening is the SMPS quiescent current is starting to approach the magnitude of the load current. SMPS internal circuits are more complex than the LDO, so the quiescent current may be higher. Equation (3) becomes,

$$I_{in} = \frac{I_{out} \cdot V_{out}}{V_{in} \cdot Eff}$$

Any gains from the output to input voltage ratio are lost. The input current then looks like the LDO case,

$$I_{in} \approx I_{out} + I_q$$

Advanced SMPS integrated circuits that are specifically designed for battery powered products employ other methods for improving performance at low currents.

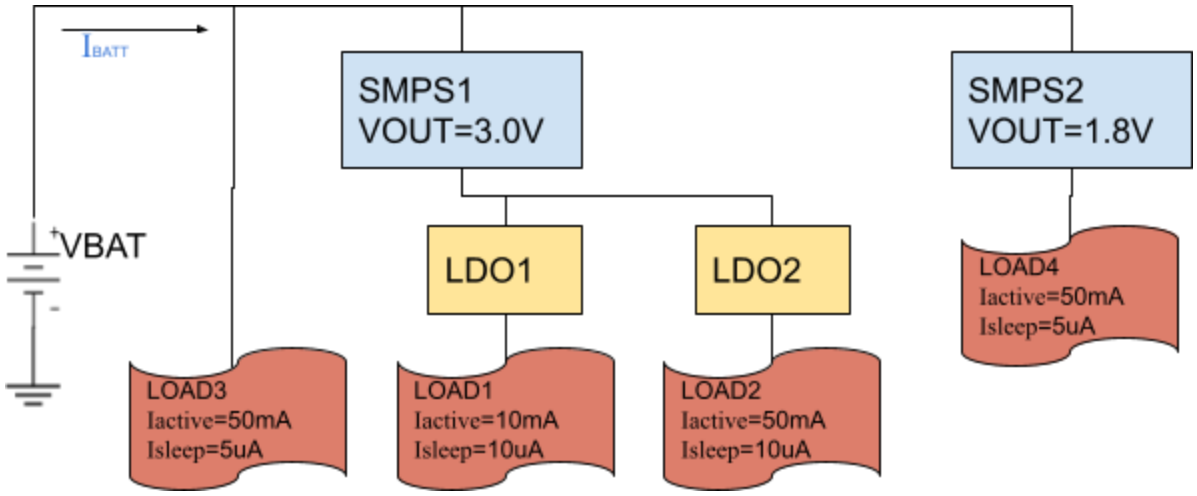
SMPS Model Implications

- Active Load State
  - The smaller currents can be ignored
  - $I_{in} = \frac{I_{out} \cdot V_{out}}{V_{in} \cdot Eff}$, $where\ Eff \approx 0.90$
- Standby State
  - LDO quiescent current should be considered
  - $I_{in} \approx I_{out} + I_q$

Modelling With LDOs and SMPSs

Let's now consider a block diagram of a theoretical product that uses LDOs and SMPSs. The goal is to refer the point of load currents back to the battery, to get Battery Referred currents, or, what the battery sees as the current. The Active time and frequency for all loads areset to the same to highlight the impact of the DC/DC design.

- LOAD2, LOAD3 & LOAD4 are all 50mA, but are in different places in the power tree, resulting in different battery referred current, and thus total coulomb impact.
- LOAD4 has the least impact on battery life because it has the highest SMPS voltage ratio.



Here is an example simple spreadsheet that highlights the impact of the DC/DC design above.

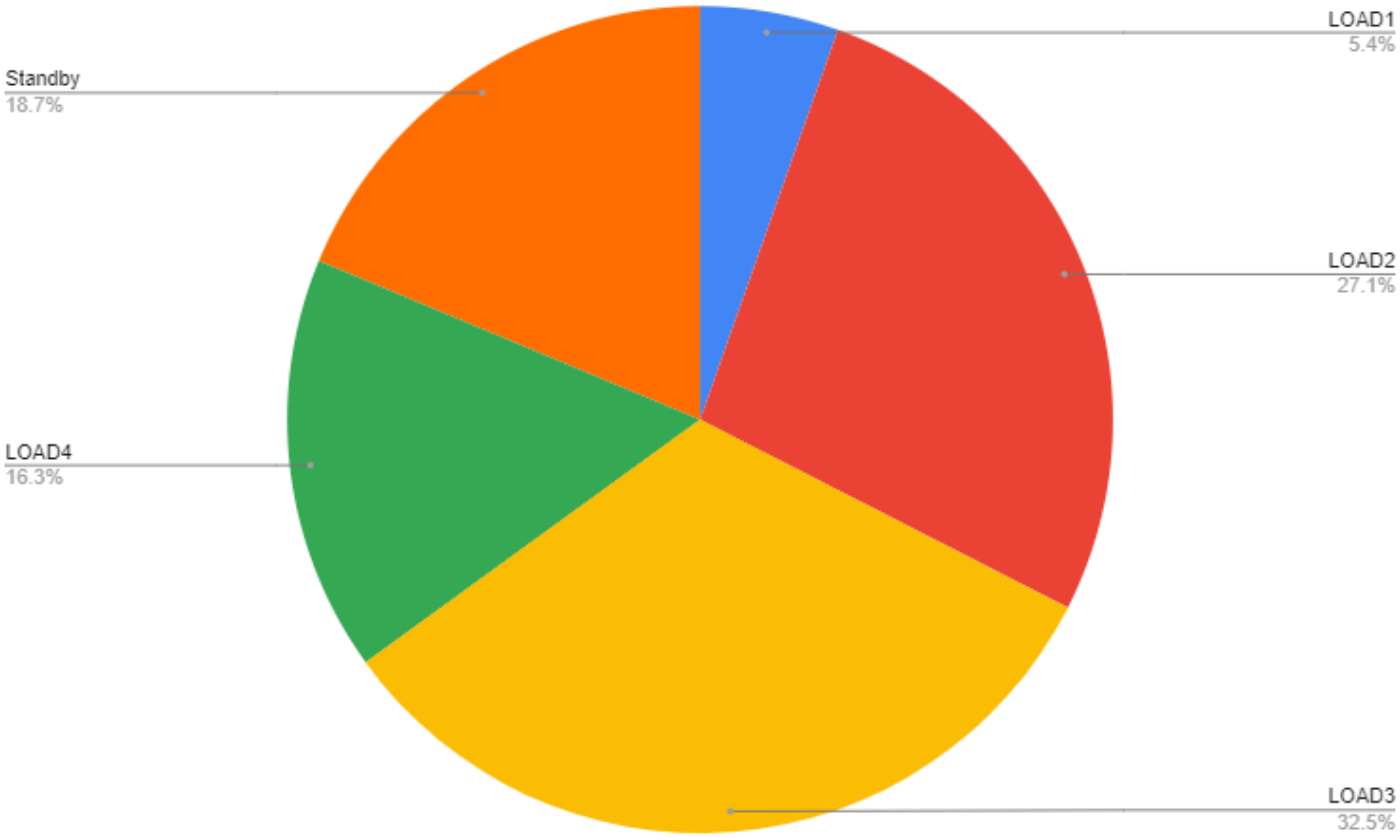
Days	98	0.27	Years
Seconds	8467200		
SMPS Vin (VBAT) (V)	4		

Active States	Current (mA)	SMPS VOUT (V)	SMPS EFF %	SMPS IIN (mA)	Battery Referred (mA)	Duration (s)	Coulombs / Activation	Activation Freq (Hz)	# Activations	Total Coulombs
LOAD1	10	3	0.9	8.33	8.33	10	0.083	0.000278	2352	196
LOAD2	50	3	0.9	41.67	41.67	10	0.417	0.000278	2352	980
LOAD3	50				50.00	10	0.500	0.000278	2352	1176
LOAD4	50	1.8	0.9	25.00	25.00	10	0.250	0.000278	2352	588
									Total Clmbs	2940

Standby States	Current (mA)	SMPS Iq (mA)		LDO Iq (mA)	Battery Referred (mA)
LOAD1	0.01	0.02		0.005	0.035
LOAD2	0.01			0.005	0.015
LOAD3	0.005				0.005
LOAD4	0.005	0.02			0.025
				Total (mA)	0.080
				Total Clmbs	677

Total Coulombs	3617	(3600 Couombs per 1000mAhr of battery)

The resulting pie chart shows the contribution of each load/mode to the battery life.



Note the contribution between LOAD3 and LOAD4, which both have the same output profile, but have a significant difference when that current is referred back to the battery because of the DC/DC design.

Summary

This short paper demonstrates how to model the product's DC/DC architecture in order to understand the impact of each load on the battery. The battery is a bucket of charge that is drained by the product load currents. The load currents at the battery are affected by the DC/DC design.

A battery usage model is very helpful in planning engineering resources to improve battery life.