

Prism Teensy Board level Test (BLT)

Refer to www.sistemi.ca for Prism/Lente Test Framework.

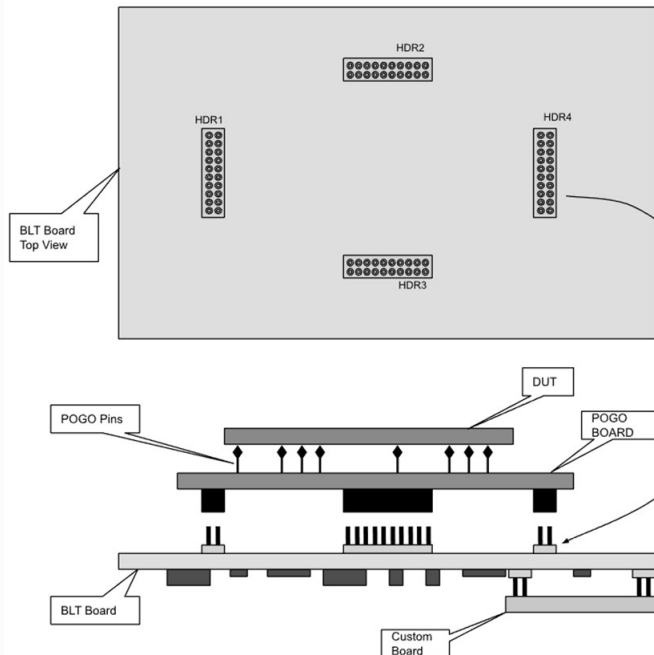
Testing Capabilities:

Each Header (1, 2, 3, 4) exposes the MAX11311 chip pins to the DUT. Each pin can be configured for either GPIO, DAC (12 bit) or ADC (12 bit), and output range of 0-2.5/5/10V.

In Addition to the MAX11311 each Header provides additional functions,

- 1] VBAT Emulator, sinking and sourcing current, with current measurement, 1-10V.
VBUS (5V) Supply with current measurement.
Additional Supply 1-5V.
UART (with level shifter)
- 2] I2C (with level shifter)
- 3] Segger JTAG (4 wire)
USB Slave to PC or Teensy
- 4] Connections to expansion Custom PCB
Custom PCB - create specific test measurement or stimulus circuits
- Connections for Power (3,3V, VBAT, VBUS, 6V)
- I2C and UART connections to Teensy

Stack Up

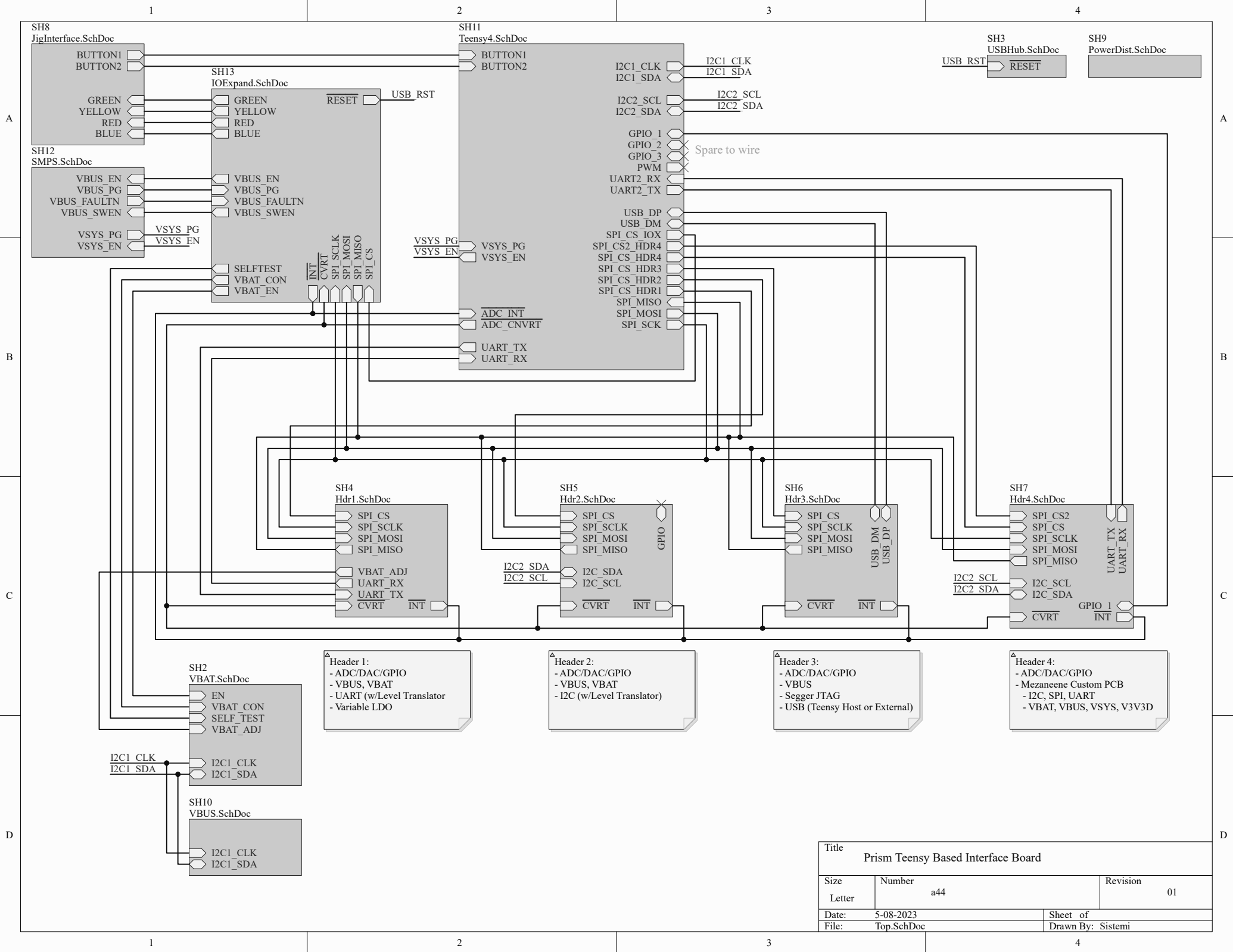


Stack Up Notes

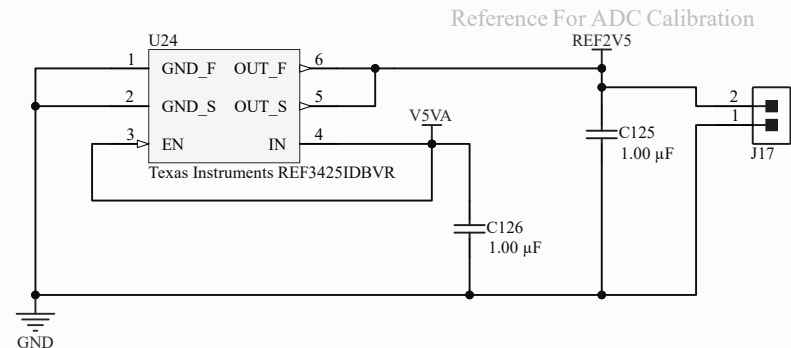
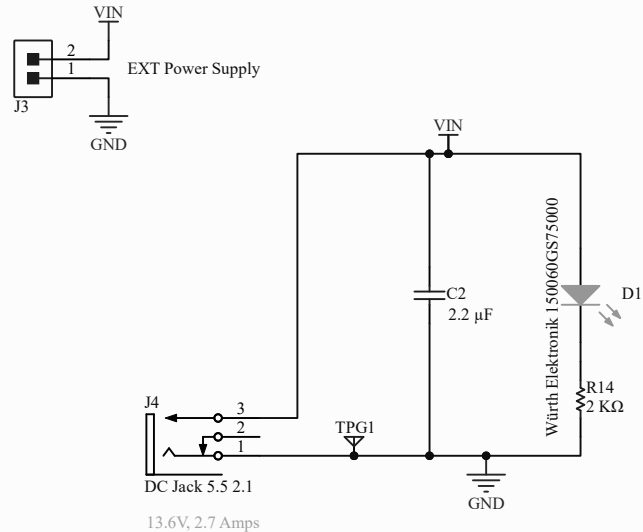
- 1) The BLT board provides test measurements and stimulus.
- 2) The Pogo Board interfaces the BLT board to the Device Under Test (DUT) via spring loaded probes.

Various DUTs can be supported by one BLT board by using different Pogo Boards.

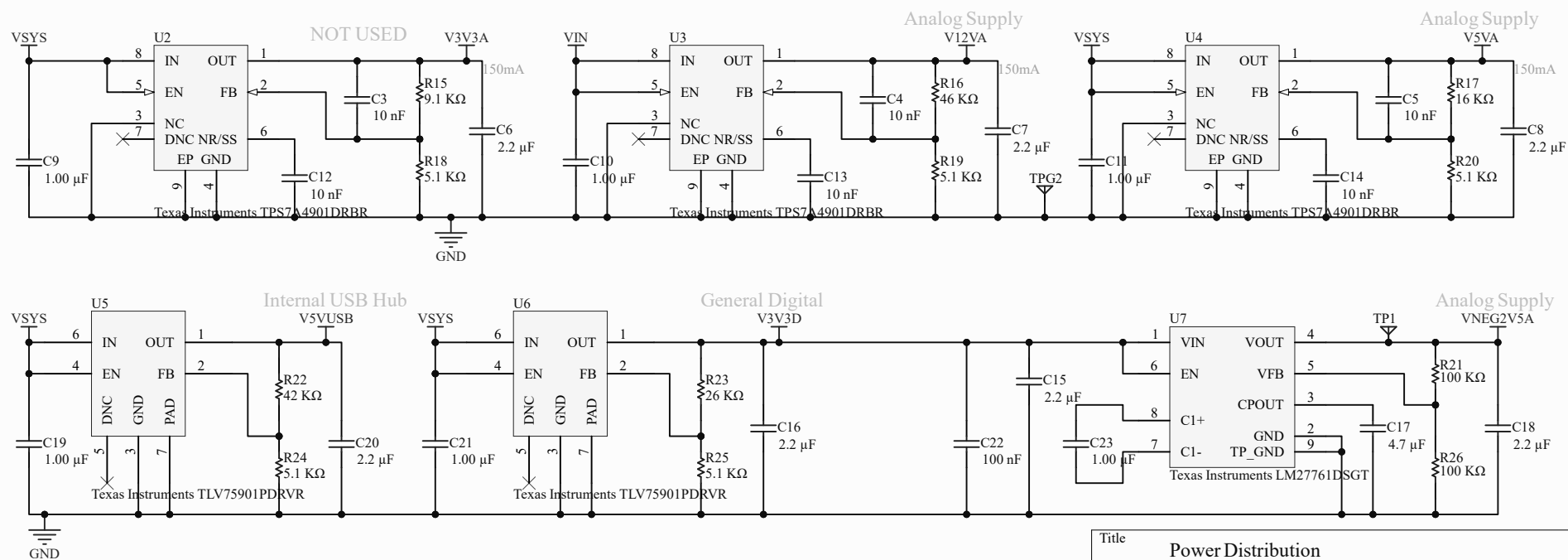
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|-------------------------|------------------|-----------|---------|
| Title | | | |
| Block Diagram and Notes | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | BlockDiag.SchDoc | Drawn By: | Sistemi |



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|---|---------------|----------------|---------|
| Title Prism Teensy Based Interface Board | | | |
| Size Letter | Number a44 | Revision 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | Top.SchDoc | Drawn By: | Sistemi |



ALL INTERNAL VOLTAGE SUPPLIES



| | | | | | | | |
|--------|--|------------------|--|--------------------|-------------------|--|--|
| Title | | | | Power Distribution | | | |
| Size | | Number | | | Revision | | |
| Letter | | a44 | | | 01 | | |
| Date: | | 5-08-2023 | | | Sheet of | | |
| File: | | PowerDist.SchDoc | | | Drawn By: Sistemi | | |

A

B

C

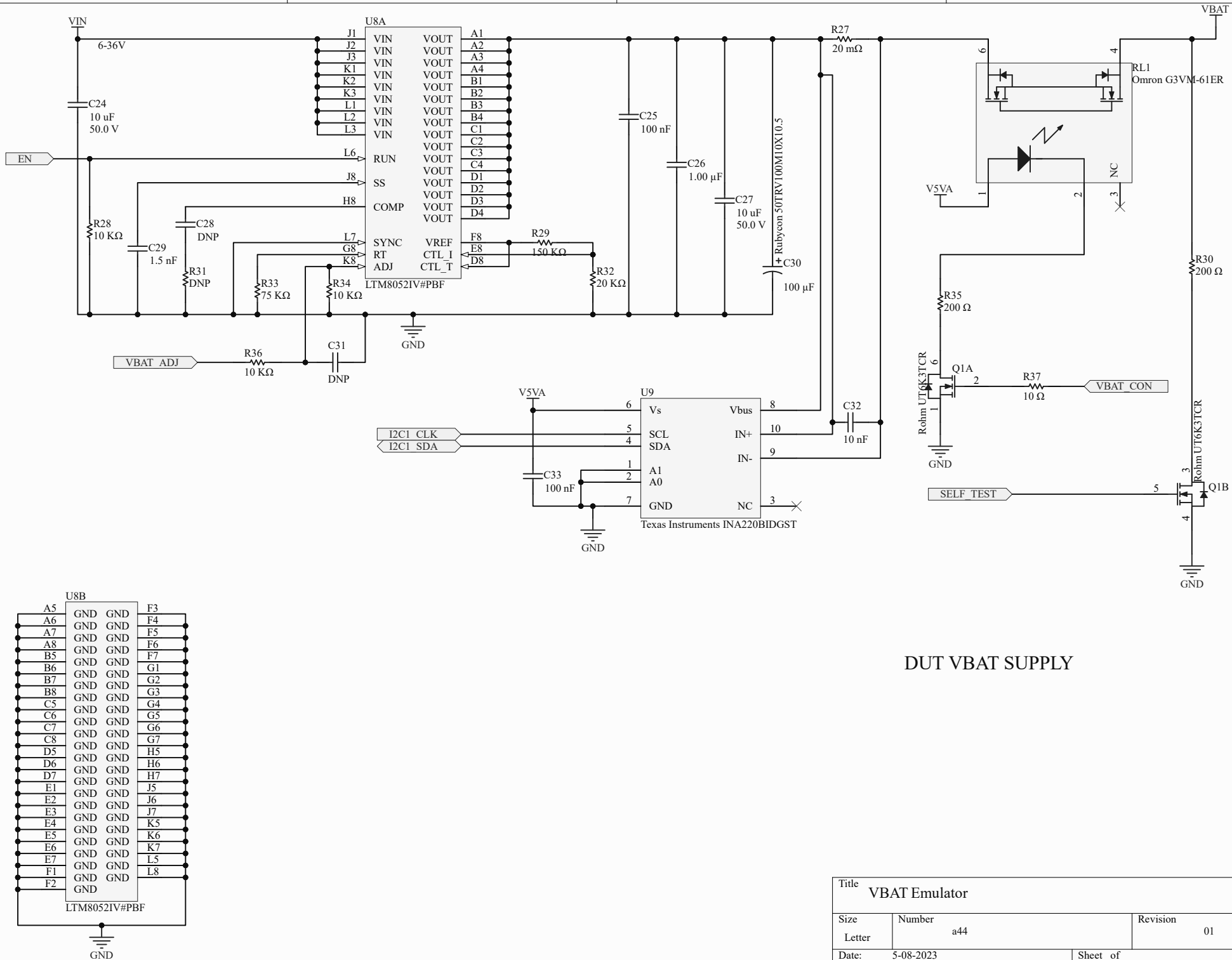
D

A

B

C

D



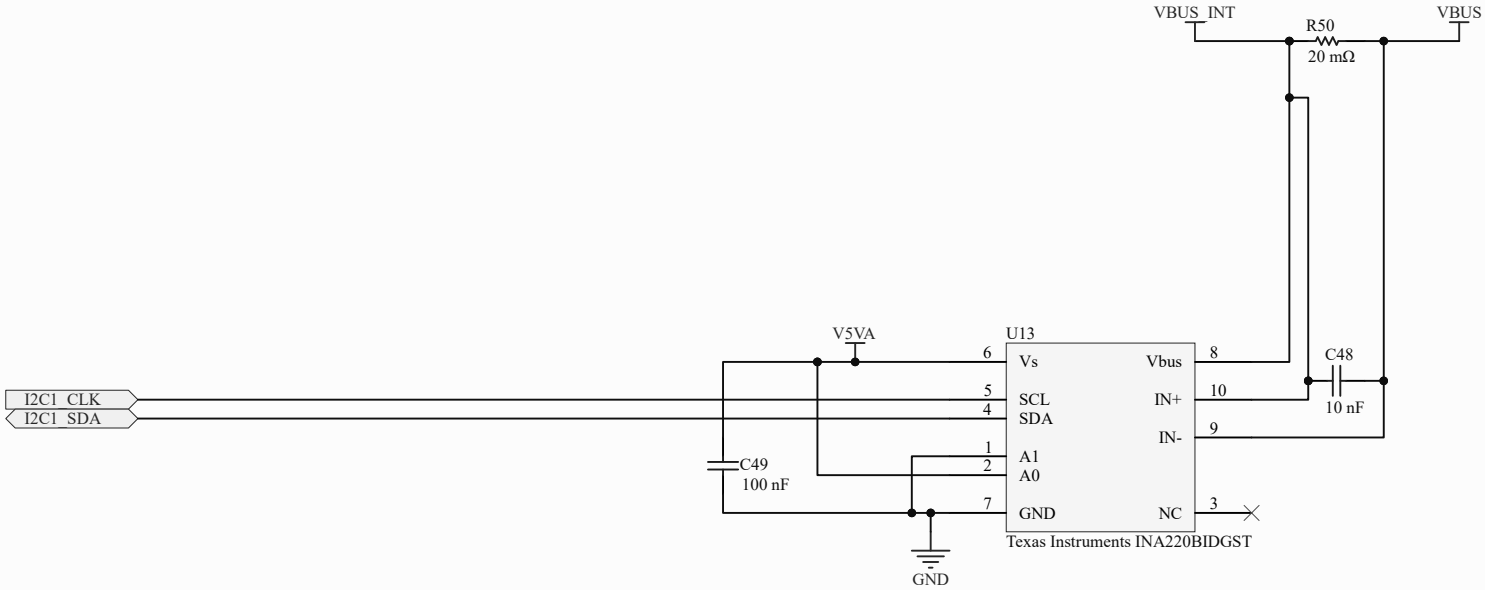
1

2

3

4

DUT VBUS SUPPLY



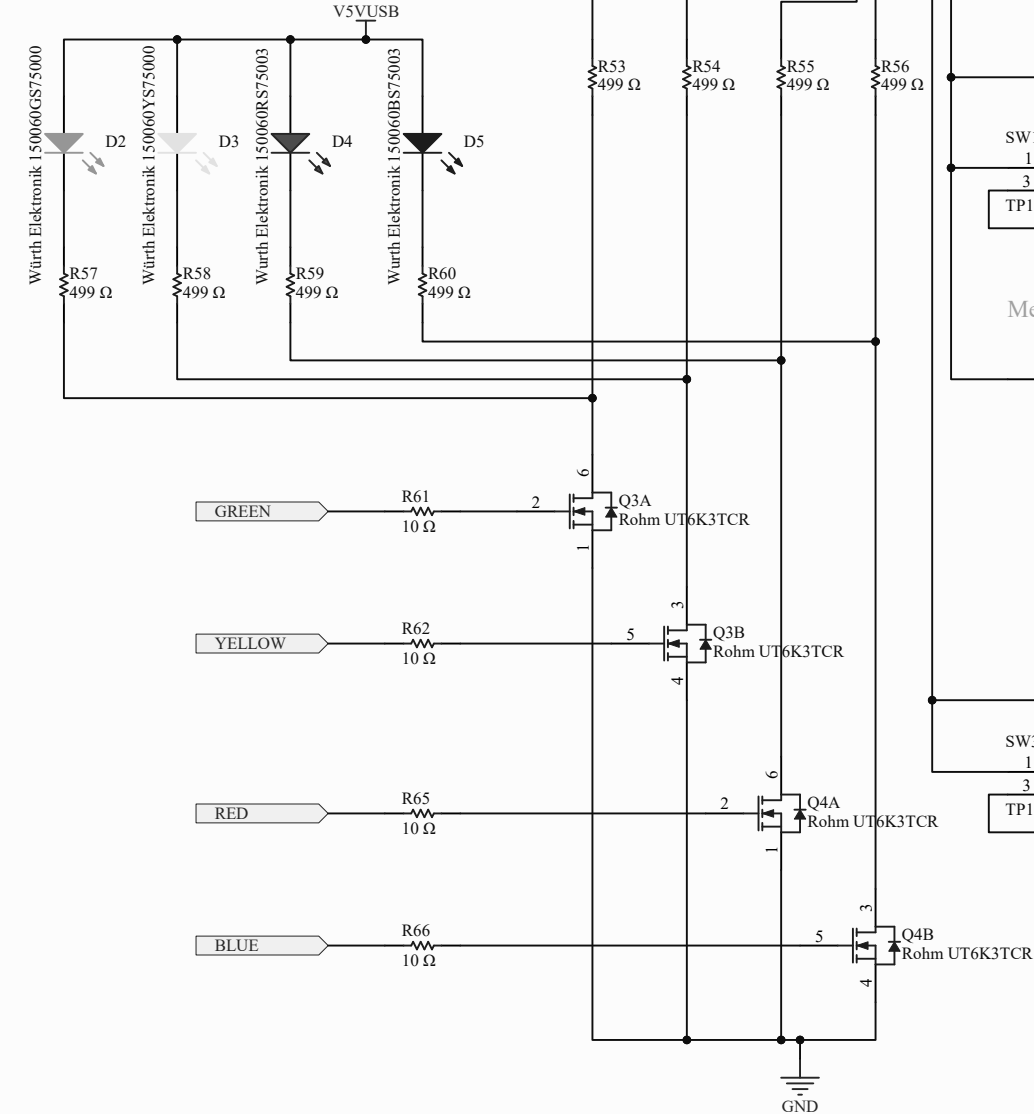
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|--------|-------------|-----------|---------|
| Title | | | |
| VBUS | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | VBUS.SchDoc | Drawn By: | Sistemi |

LED Status on-board and off-board, in parallel.

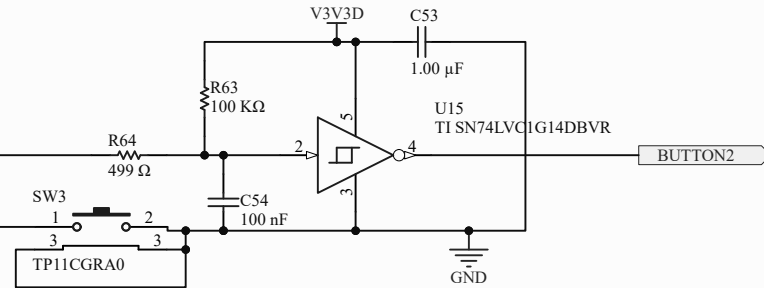
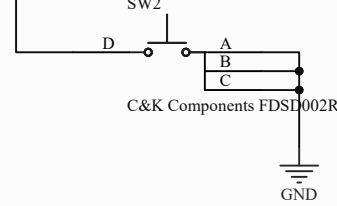
Prism Controlled:
GREEN, YELLOW, RED

User Defined: BLUE

Mounted LEDs/Switches Cable Harness



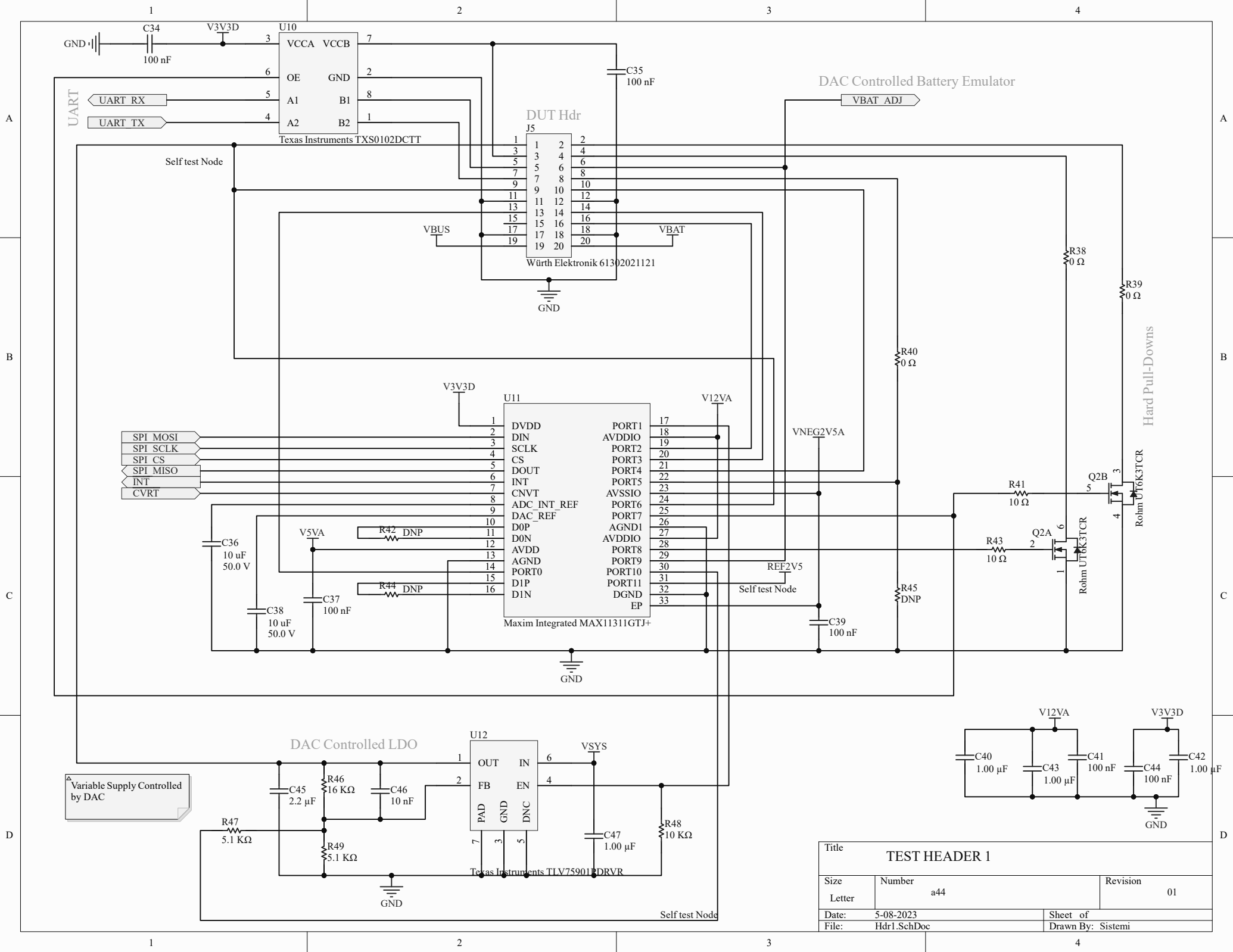
Mechanical Plunger Detect Switch



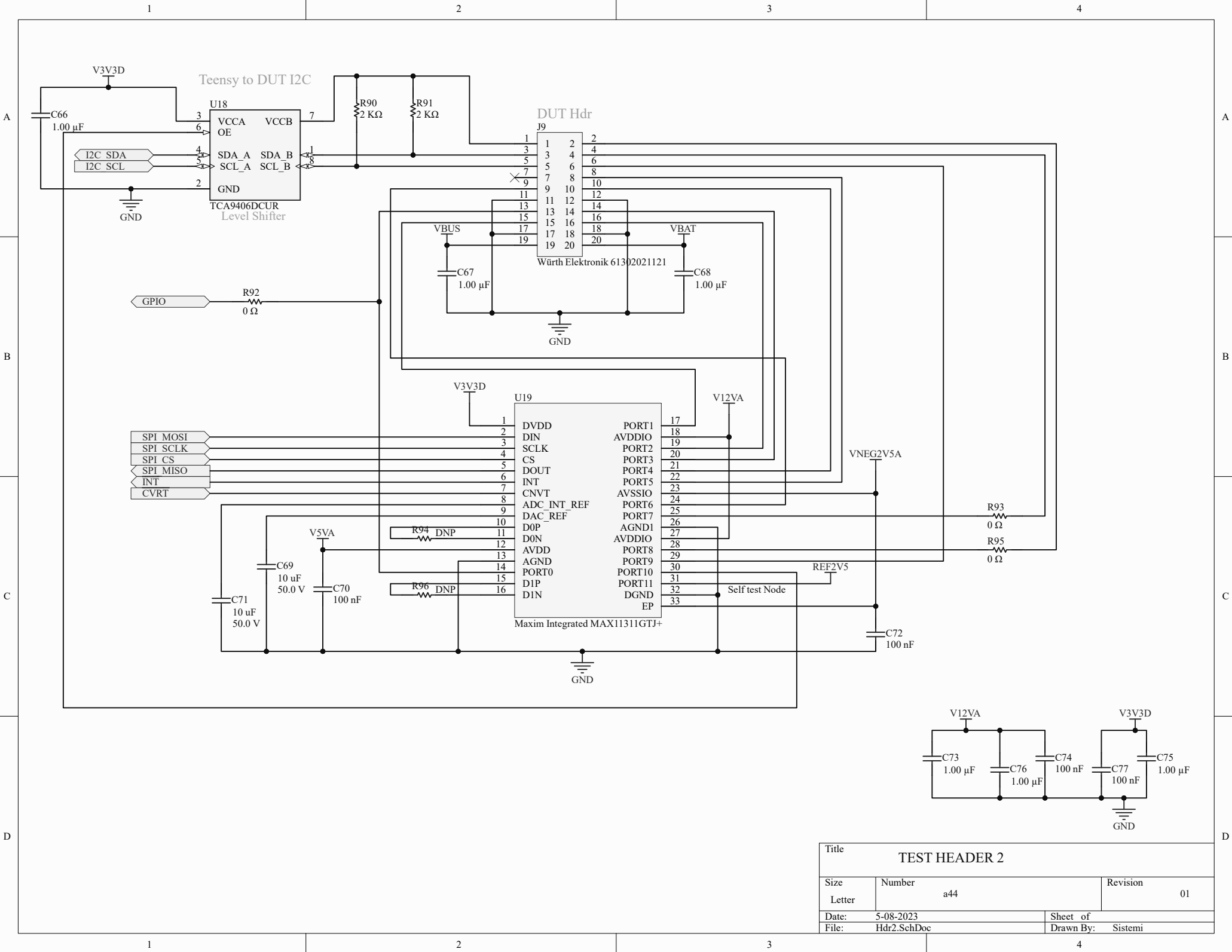
NOTES:

- 1) On board Switches (SW1/2) are for debug purposes.
- 2) Test Jig fixture will have mounted switches.
- 3) SW3 is for plunger detect via mechanical activator.

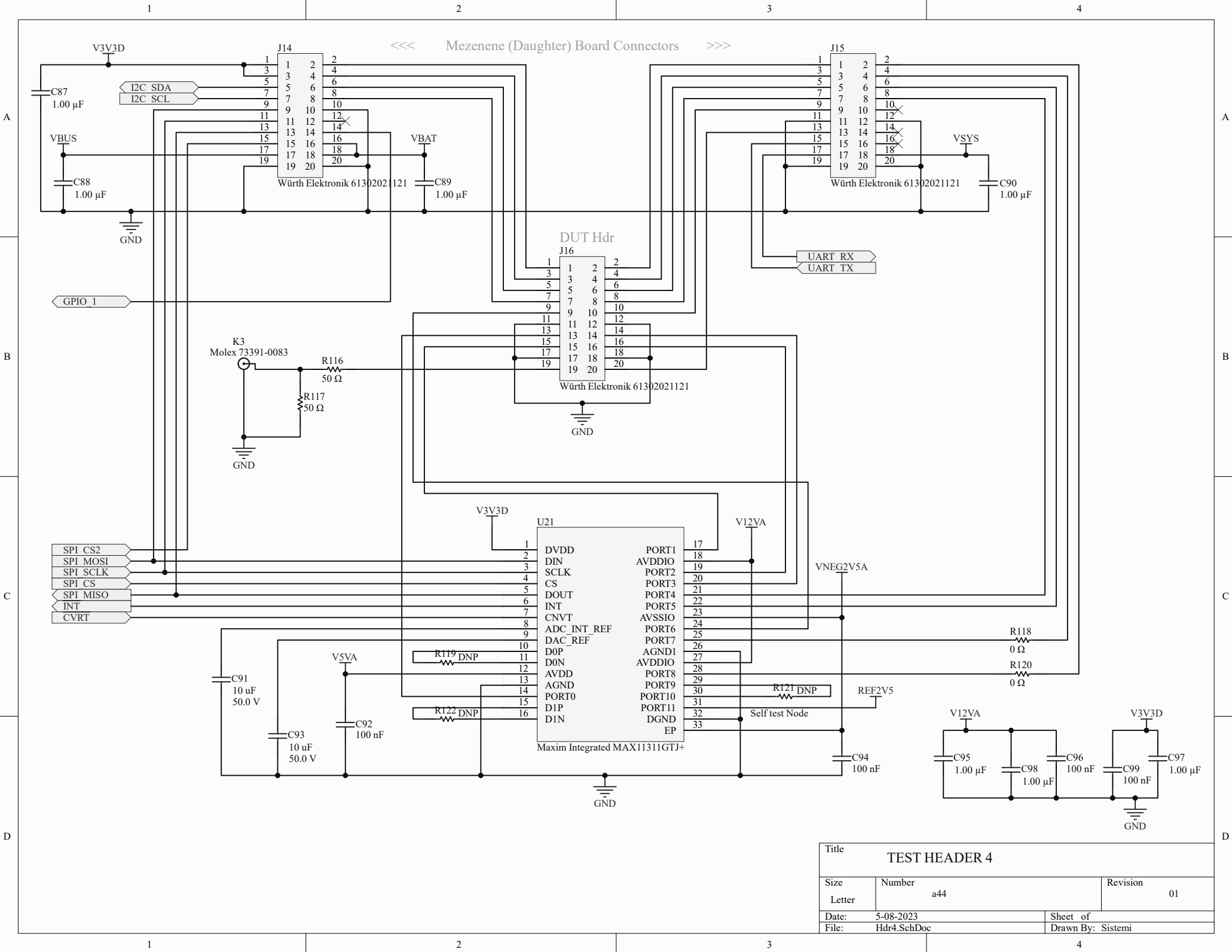
| Title | | | |
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| Jig (user) Interface | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | JigInterface.SchDoc | Drawn By: | Sistemi |



| Title | | | |
|---------------|-------------|-----------|---------|
| TEST HEADER 1 | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | Hdr1.SchDoc | Drawn By: | Sistemi |



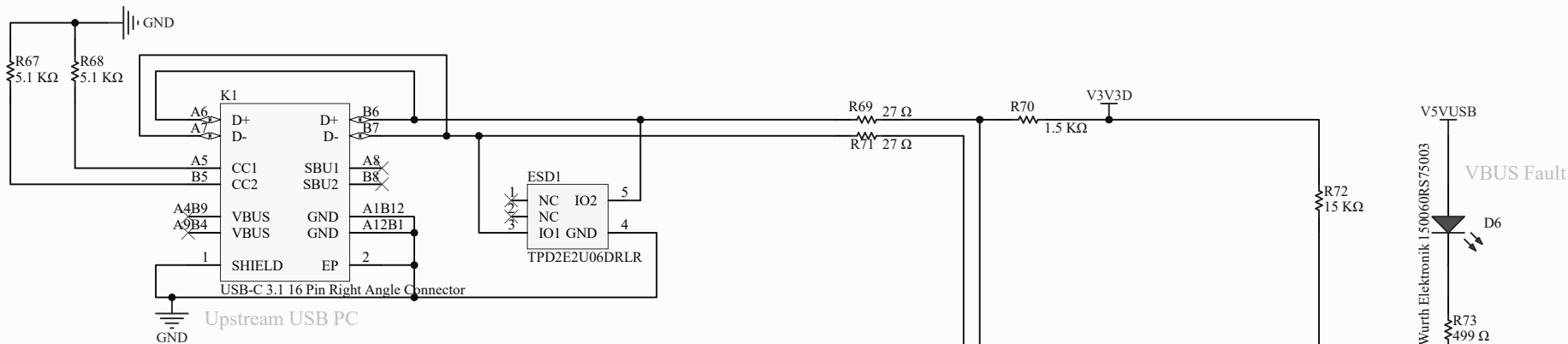
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| Title | | | |
| TEST HEADER 2 | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | Hdr2.SchDoc | Drawn By: | Sistemi |



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| Title | | | |
| TEST HEADER 4 | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | Hdr4.SchDoc | Drawn By: | Sistemi |

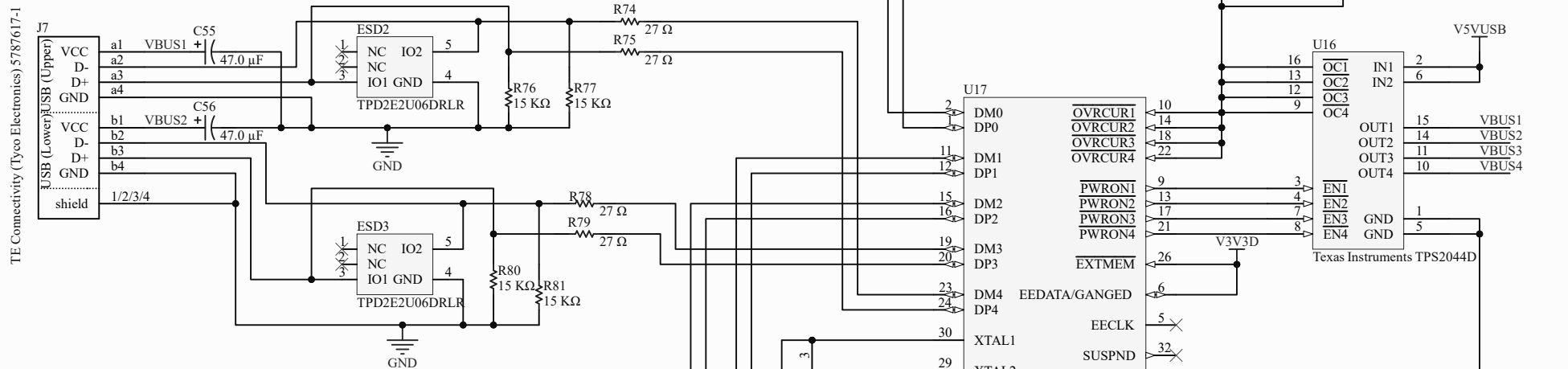
A

A



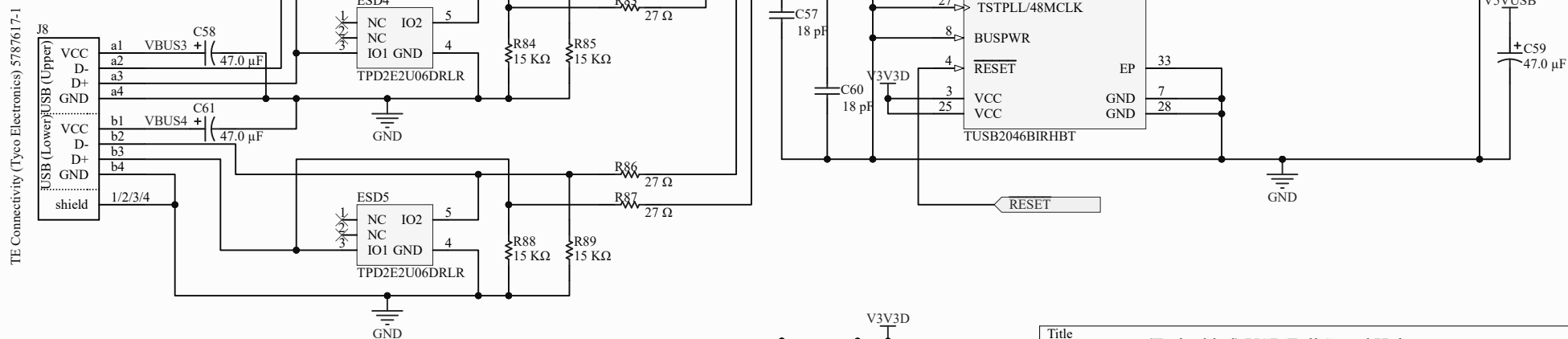
B

B



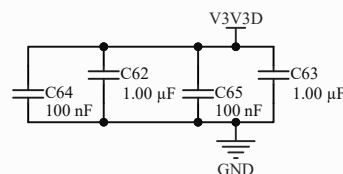
C

C

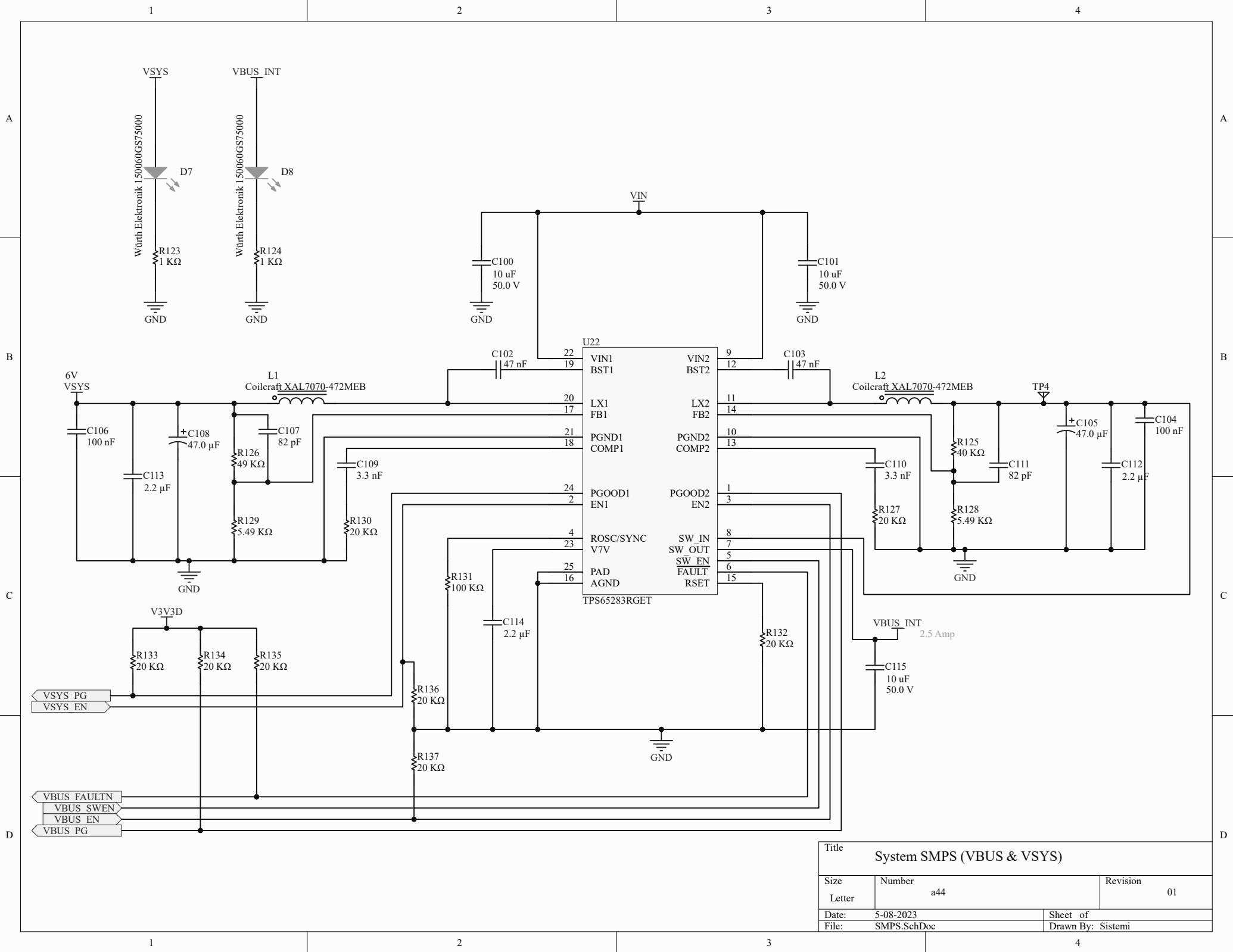


D

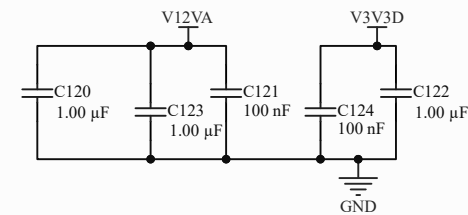
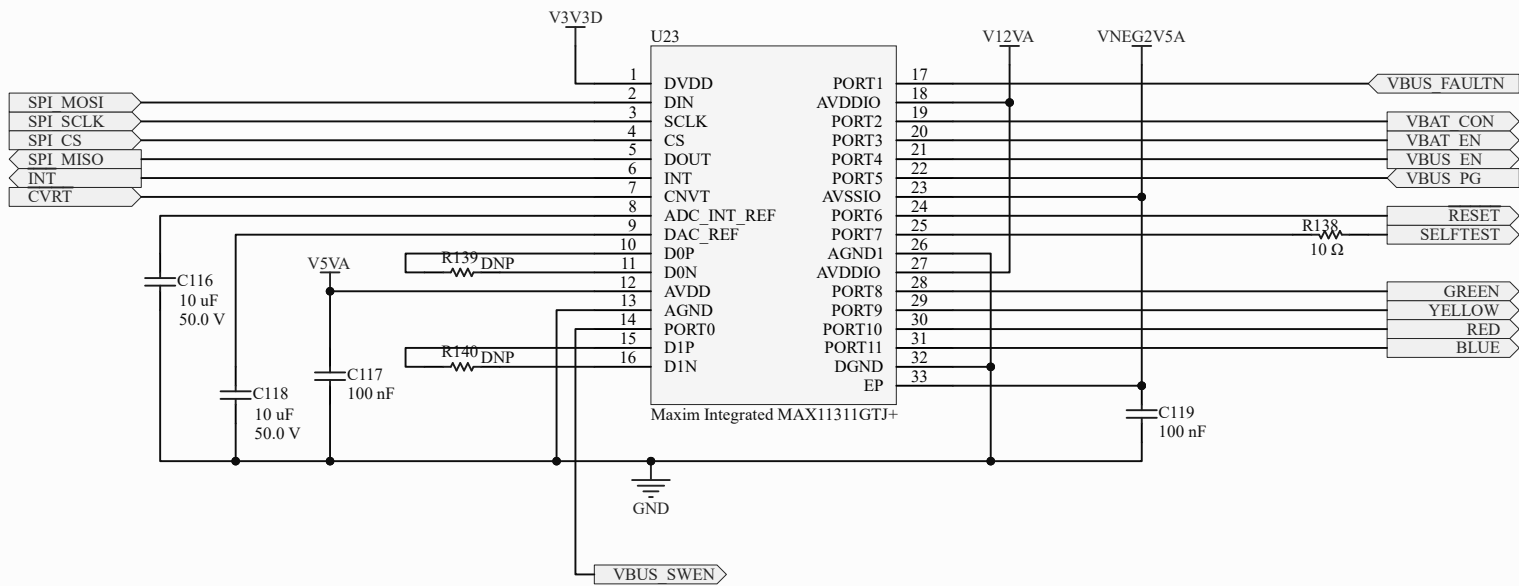
D



| Title | | | |
|-------------------------------|---------------|-----------|---------|
| (Embedded) USB Full Speed Hub | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | USBHub.SchDoc | Drawn By: | Sistemi |



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|---------------------------|-------------|-----------|---------|
| Title | | | |
| System SMPS (VBUS & VSYS) | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | SMPS.SchDoc | Drawn By: | Sistemi |



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|------------------------|-----------------|-----------|---------|
| Title | | | |
| IO Expand (for Teensy) | | | |
| Size | Number | Revision | |
| Letter | a44 | 01 | |
| Date: | 5-08-2023 | Sheet of | |
| File: | IOExpand.SchDoc | Drawn By: | Sistemi |