DIGITAL LOGIC ASSIGNMENTS

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ASSIGNMENT – 1

1. Differentiate between Analog and Digital system.
2. Convert the following decimal numbers into hexadecimal and octal number. a) 304 b) 224
3. Convert the following octal numbers to hexadecimal.
   a) 1760.46 b) 6055.263
   (C2D.598)
4. Draw a logic gates that implements the following
   a) $A = (Y_1 \oplus Y_2)(Y_3 \odot Y_4) + (Y_5 \oplus Y_6 \oplus Y_7)$
   b) $A = (X_1 \odot X_2) + (X_3 \odot X_4) + (X_4 \odot X_5) \oplus (X_6 \odot X_7)$
5. State and prove De-Morgan's theorem 1st and 2nd with logic gates and truth table.
6. Which gates can be used as inverters in addition to the NOT gate and how?
7. Represent the decimal number 8620
   a) In BCD b) in excess-3 code c) in 2,4,2,1 code and d) as a binary number
8. Convert the following hexadecimal number to decimal and octal numbers
   a) 0FFF (b) 3FFF
9. What do you mean by universal gate? Realize the following logic gates using NOR gates.
   a) OR gate (b) AND gate
10. What do you mean by Gray Code? What are its applications?
11. Write the first 20 decimal digits in base 3.
12. Convert the decimal number 250.5 to base 3, base 4, base 7, base 8 and base 16.
13. Perform subtraction with the following decimal numbers using both 9's complement and 10's complement
    a) 5250 – 321 c) 753-864
    b) 3570-2100 d) 20-1000
14. Perform the subtraction with the following binary numbers using both 1's complement and 2's complement
    a) 11010 – 1101 c) 10010 – 10011
    b) 11010 – 10000 d) 100 - 110000
15. Convert the Following:
    a) $(A08E.FA)_{16} = (?)_{10}$
    b) $(AE9.B0E)_{16} = (?)_{2}$
16. Perform $(-44)_{10} – (67)_{10}$ using 10's complement method.
17. Differentiate between weighted code and non-weighted code with examples.

18. Explain why Excess-3 code is self-complementary code with an example.
19. What is Parity bit? Explain how it is used as error detection code.
20. Explain IC Digital Logic Families with their characteristics.
21. Write Short Notes on:
    a) EBCDIC.
    b) Integrated circuit
    c) Alphanumeric codes

ASSIGNMENT – 2

22. Describe the three Variable K-map with example.
23. What is combinational logic? What are its important features?
24. Design a half adder logic using only NOR gate.
25. Draw a block diagram, truth table and logic circuit of a 16 x 1 multiplexer and explain its working principle.
26. Design the full subtractor circuit with using Decoder and explain the working principle.
27. Design the Decoder using Universal gates.
28. Design a decimal adder with logic diagram and truth table.
29. Differentiate between a MUX and DEMUX.
30. What is magnitude comparator? Design a logic circuit for a 4-bit magnitude comparator and explain it.
31. What do you mean by full adder and full subtractor? Explain.
32. Design a 3 to 8 line decoder using two 2 to 4 line decoder and explain it.
33. What is a decoder? Implement the following using decoder.
    a) F (W X Y Z) = $\sum$ (0, 1, 3, 4, 8, 9, 10)
    b) F (W X Y Z) = $\sum$ (1, 3, 5, 6, 11, 13, 14)
34. Explain the programmable logic array (PLA) and programmable Array Logic (PAL).
35. Design a multiplexer 4 x 1 using only universal gates.
36. Design a half adder logic circuit using NOR gates only.
37. Write a procedure to reduce 4 variable K- maps.
38. 1. Implement the following function $F = \sum (1, 2, 3, 4, 8)$ using

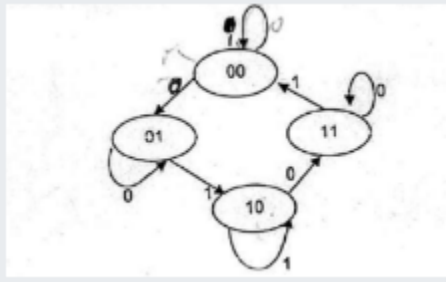
    (a) Decoder

    (b) Multiplexer

    (c) PLA

ASSIGNMENT – 3

39. Explain the 4 bit ripple counter and also draw a timing diagram.
40. Describe the clocked RS flip-flop.
41. What do you mean by triggering of flip flop?
42. What are the shift Register operations?
43. Describe the Ripple counter.
44. Design the 4 bit Synchronous up/down counter with timing diagram, logic diagram and truth table.
45. Explain the operation of Decoder.
46. What are the various types of shift registers?
47. What do you mean by synchronous counter?
48. What is JK master slave flip-flop? Design its logic circuit, truth table and explain the working principle.
49. Design a clocked sequential circuit of the following state diagram by using JK flip flop.



50. Write short notes on:
    a) Programmable logic array (PLA)
    b) Triggering at flip-flop
    c) Memory unit