ZLR964124
Reference Design User Guide for the Le9641 miSLIC™ Device

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1.0 Introduction

1.1 Overview

The *ZLR964124* is a two-channel FXS line module designed to interface with the Microsemi *Telephony Applications Platform (ZTAP)* for evaluating the *Le9641 miSLIC™ 1 FXS Device*. This user guide provides sample operating instructions, schematic, bill of materials, and layout references. Refer to the specific device data sheets for complete technical information.

1.2 Design Objectives

The *ZLR964124 Line Module* was designed to demonstrate a compact 2 FXS tracking battery solution based on the new Le9641 *miSLIC device*. It features two *Le9641 Single Channel miSLIC Devices* (48-pin QFN) with an optimized line interface circuit and independent tracking battery supplies.

The objectives of this reference design is to address the following:

- Two FXS ports with available profiles for worldwide operation
- Cadenced ringing will support up to 85 V_{PK} ringing and 3 to 5 REN ringer loads.
- Over-voltage / over-current protection for intra-building requirements.
- On-board 12 V input low cost Buck-Boost (Ch 1) and Inverting Boost (Ch 2) battery supplies.
- Power Efficient, compliant with the *EU Code of Conduct Version 5 (CoC)*, <1 W/ch off hook.
- Designed for up to 1200 Ω total loop.
- PCM / SPI interface operation at up to 8.192 MHz (with *ZTAP*).
- DC sensing is outside the protection to allow support for *VeriVoice* foreign voltage tests.
- Compact design and layout example measuring 6 cm^2 per FXS channel.
- On board Module ID ROM (MID) provides the default device profile, AC profile, DC profile, and ringing profile. A profile is defined by the *Profile Wizard* software tool for configuring Microsemi voice products.
- *ZTAP* and *Microsemi Voice Toolkit (MiToolkit)* with *VP-API-II* provides fully functional operation for complete two-channel FXS operation for extensive tests meeting the data sheet specifications.

1.3 Profiles

A profile is a file that contains all of the configuration information required to set up a *VoicePort* device. A profile is created by using the *Profile Wizard* software tool. The output from *Profile Wizard* is a ***.vpw*** file. Also a ***.h*** and a ***.c*** file can be created that can be incorporated into the users system software. The Microsemi *VP API-II* and *VP-API-II Lite* software packages use profiles to configure the device. Note that some profiles are not available with the *VP-API-II Lite* software and require that the full *VP API-II* software be licensed.

Le9641 requires VoicePath API-II™ P2.24.0, available for download from the Microsemi web site for registered customers.

Within a profile are individual data strings for configuring the different functional blocks within the device. Microsemi has profiles available for most countries and major telephony standards. 9 types of profiles are supported:

- *Device:* This profile defines PCM timing and switcher configuration
- *AC FXS:* This profile sets the AC parameters such as impedance and levels. The input for the AC profile are the coefficients generated by the *WinSLAC* software tool.
- *DC:* This profile defines the DC feed parameters such as open circuit voltage, DC feed current, hook threshold, ground key or fault thresholds.
- *Ringing:* This profile sets the ringing voltage, frequency and ring trip parameters.
- *Tone:* This profile defines call progress tone frequencies and levels.
- *Ringing Cadence:* This profile sets the cadence that is associated with ringing.
- *Tone Cadence:* This profile defines call progress tone cadences. This Profile is used in conjunction with the Tone Profile, which defines the frequencies.
- *Caller ID:* This profile sets Caller ID parameters
- *Metering*: This profile defines the frequencies and other parameters associated with subscriber pulse metering.

1.4 References

The following documents are referred to in this document and may be helpful:

1. *Le9641 Subscriber Line Interface Circuit miSLIC™ Data Sheet*, Document ID#: 148556
2. *Microsemi Telephony Applications Platform (ZTAP) User's Guide,* Document ID# 136057
3. *Profile Wizard User's Guide*, Document ID#: 127063
4. *ZL880 VP-API-II Reference Guide*, Document ID#: 143271
5. *VeriVoice Professional Test Suite Software*, Document ID#: 081516

Also referenced in this document is the Microsemi CMPG web site for file downloads.

http://www.microsemi.com/voice-line-circuits.

2.0 Quick Start Guide

2.1 Required Materials

The following materials will be required to set up the *ZLR964124* line module system:

- *Le71HK0004 Telephony Applications Platform (ZTAP) Kit* with file system P1.20 or later (available from Microsemi's web site, OPN *Le71SDKZTAP*);
- Software tools downloaded from the Microsemi web site, including *MiToolkit* (OPN *Le71SDKTK*), release P1.10.0 or later, and *Profile Wizard* (OPN *Le71SDKPRO*), release P2.7 or later;
- *ZLR964124* line module;
- Two analog telephone sets; and
- Two RJ-11 telephone cords.

Refer to Table 1 for a listing of the essential *MiToolkit* applications.

Application	Operating Functions	Description
VP-Script	*ZTAP* Control	*ZTAP* software image update; Tcl script editing and execution; console and terminal communication
Mini-PBX	Main Window / Stand-Alone Visual PBX	Discovers modules and assigns extension numbers and termination types (FXS or FXO) for each hardware port; Initializes the *Call Control* application with the profiles parameters found on the Module ID (MID) for each of the installed modules; Displays real-time status and *VP-API-II* line states for all extensions; Enables calling from any FXS into any other FXS or an FXO port.
	Profile Parameter Loading	By clicking on any extension displayed on the *Mini-PBX* main window, *Profile Wizard*-generated files may be loaded and applied to the port associated with that extension. Profiles include AC and DC coefficients, Ringing parameters, FXO / Dialing parameters, etc.
	Half Channel Setup and Testing	By clicking on any extension displayed on the *Mini-PBX* main window, the following half-channel functions are available: a) Manual line state control, b) PCM time slot assignment, and c) RX and TX gain adjustment. These functions enable AC and DC functional testing by placing the channel into one of the *VP-API-II* system states and connecting the PCM highway to the E1/T1 interface on the *ZTAP* platform.
	Line Testing	Clicking on any FXS extension displayed on the *Mini-PBX* main window and selecting the Line Testing tab provides access to *VeriVoice* tests. Tests such as line voltage, receiver off-hook, resistive faults, and ringer equivalence number (REN) may be run on that port.
	VP-API-II Line Debug	By clicking on the *Terminal* menu item, a terminal application is launched allowing the user to type commands and view *VP-API-II* run-time debug messages. The *VP-API-II* function ***VpSetOption()*** with ***VP_OPTION_ID_DEBUG_SELECT*** is used to enable debug messages.

Table 1 - Essential MiToolkit Applications

2.2 Getting Started

The Microsemi *ZLR964124* line module is designed to mate with the *SM2* receptacle found on the *ZTAP* platform and is configurable by the *MiToolkit* software.

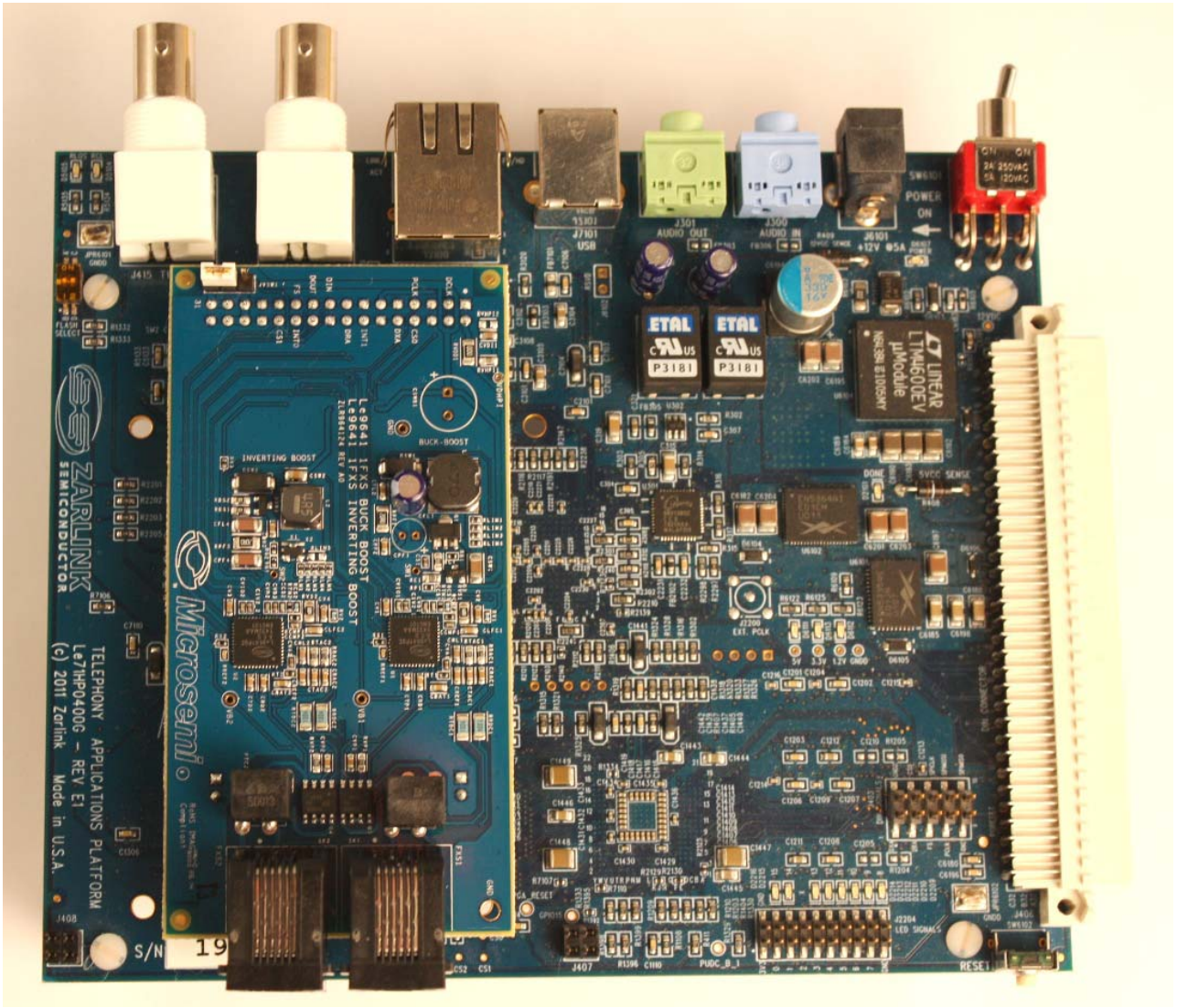


Figure 1 - ZTAP and ZLR964124 Line Module Setup

The *ZTAP* platform can accommodate one to eight telephone interfaces for the *SM* or DIN receptacle and up to four interfaces for the *SM2* receptacle (depending on line module capability). Note that *SM* and *SM2* receptacles overlap so only one type may be inserted at a time. An additional line module (*SM* or *SM2*) can be supported via an *Le71HR0411G* adapter board that connects to the *ZTAP* DIN receptacle. The *ZTAP Kit* is supplied with an external power supply adapter and accepts an optional high voltage power supply and ringer source module (for external unbalanced ringing applications). The *Mini-PBX* application is contained within the *MiToolkit* software package that configures the attached devices based on the Line Module MID. A USB cable is used to communicate with a PC running *MiToolkit*.

The *ZLR964124* module features two FXS ports accessible through its RJ-11 telephone jacks.

Quick start steps:

1. Assemble the components as shown in Figure 1 and connect a USB cable between the *ZTAP*'s USB port (J7101) and a PC.
2. Plug the supplied 12V AC/DC adapter into the *ZTAP*'s +12 V input jack J6101.
3. Apply power to the *ZTAP* and installed line module by switching *SW6101* to the left. The system will boot up within about 20 seconds, initialize the installed line module, and automatically run the call control application. This allows pulse- and DTMF-dialed calls to be made between the telephony ports even without a PC attached.
4. Start the *MiToolkit* application.
5. When *MiToolkit* starts up, it will display a list of applications. Run the *Mini-PBX* application.
6. When *Mini-PBX* starts, it will prompt for which serial port to use. If *VP-Script* is already running, *Mini-PBX* will know what port is being used. Note that the *ZTAP Support Package* software installation includes a Virtual COM Port Driver to support USB-to-serial UART interface on the *ZTAP* board.
7. When *Mini-PBX* starts, it will identify the module plugged on the *ZTAP* and initialize it to the appropriate Idle state. The extension number, line type, and line state will also be displayed.
8. Refer to the *Microsemi Telephony Applications Platform User's Guide* for additional installation and operation details.

2.3 Making Test Calls

This arrangement for the two-channel line modules is as a single PBX network. The setup requires that the *ZLR964124* line module be installed on the *SM2* receptacle on the *ZTAP* platform.

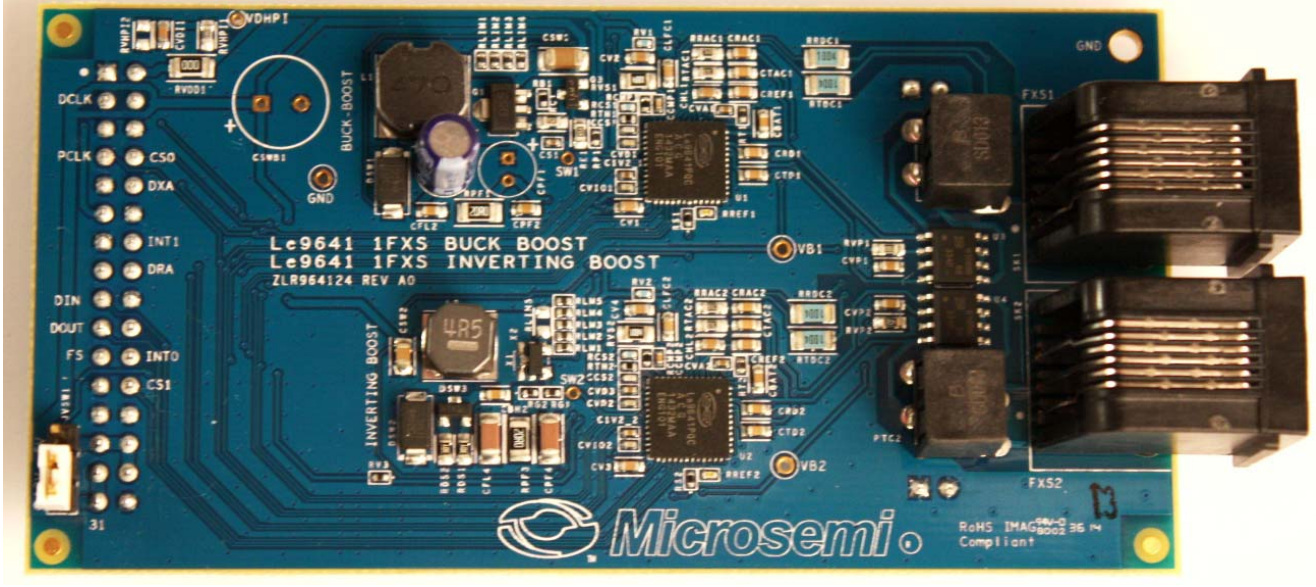


Figure 2 - ZLR964124 Line Module

The *ZLR964124* line module is equipped with two FXS ports. *Mini-PBX* assigns extension numbers to each port, which are typically 100 and 101 for the FXS ports.

- To make an FXS to FXS call, connect two telephone sets to the two FXS ports on the line module and go off-hook on one of them.
- *Mini-PBX* detects the telephone set going off-hook and provides a dial tone. It also shows which extension has gone off-hook. Let us assume that it is extension 100 in this example. To call the second FXS port, dial 7101 (i.e. 7 followed by the extension number 101).

- *Mini-PBX* will route the call to extension 101 and initiate cadenced ringing. Default ringing is defined within the MID.
- The *Mini-PBX* will provide an audible ringback tone to the calling extension 100.
- Please note that *Mini-PBX* will generate Caller ID information to extension 101, indicating extension 100 is calling.
- When extension 101 is placed off-hook, ring trip will automatically occur and a voice path will be set up between extensions 100 and 101.
- *Mini-PBX* will reflect the current line state for all lines.

3.0 System Description

3.1 Module Features

The *ZLR964124* line module features two *Le9641 Single Channel miSLIC Devices*, a programmable tracking switching regulator circuits and line interface and protection components. The *Le9641* combines SLIC and SLAC functionality into a thermally-enhanced 48-QFN 7x7 mm package. The module communicates with the *ZTAP* board using the *SM2* interface.

3.2 System Features

The *ZLR964124* line module includes an onboard EEPROM programmed with a Module ID ROM (MID) that provides a default set of *VP-API-II* profiles for use with the board and which are automatically accessed by *ZTAP*. The two FXS lines are configured for FXS_LOW_PWR termination types and the individual profiles used in the MIDs on the *ZLR964124* were created using *Profile Wizard* 2.7 and are available from Microsemi in the following files:

- ZLR964124L_SM2_LITE_Rev2_9.VPW

Those files contains the following profiles:

- *Device Profile* for Microsemi *ZTAP* demonstration platform and configured for a Buck-Boost (FXS 1) and Inverting Boost (FXS 2).
- AC Profile providing narrow band 600 Ω AC transmission with -6 dBr receive and 0 dBr transmit levels.
- DC Profile with feed coefficients set for a calibrated 25 mA active mode loop current limit (ILA), and 48 V open circuit voltage (VOC).
- Ringing Profiles configured for sinusoidal ringing at 70.7 V_{PK} with FXS 1 being fixed mode and FXS 2 being full tracking mode.

3.3 Additional Le9641 Device Features

- Complete BORSCHT function for a single FXS telephone channel.
- Option for narrowband, 300 Hz - 3.4 kHz or wideband 50 Hz - 7 kHz operation, selectable on a per-channel basis.
- Integrated power management using on-chip switching regulator controller.
- Internal balanced ringing up to 85 V_{PK} capable of supporting up to 5 REN loads.
- Capable of sinusoidal or trapezoidal ringing.
- Selectable PCM/SPI or ZSI digital interfaces (ZLR964124 is PCM/SPI only).
- Supervision ADC for advanced power optimization and testing.
- Worldwide programmability.
- G.711 a-law / µ-law, or 16-bit linear coding.
- Powerful signal generators with support for worldwide call progress tones, howler, and caller ID.
- Subscriber loop test/self-test support with *VeriVoice* test suite software.

4.0 Circuit Design

4.1 Overview

The *ZLR964124 Line Module* consists of two *Le9641 Single Channel miSLIC* devices, line interface circuit, dedicated tracking VBAT supplies, and a host interface circuit for communication with the Microsemi *ZTAP* platform. This chapter highlights some of the design considerations including component selection and options.

4.2 Le9641 Device

The *Le9641* is a member of the new *miSLIC*^{TM} family of devices from Microsemi. It builds the heritage of *Legerity* and *Zarlink* of developing programmable SLIC and SLAC devices for the worldwide markets. The *Le9641* provides complete BORSCHT functions for a single FXS port. It features enhanced functionality, lower BOM cost, and greater power efficiency while maintaining software compatibility with the *VE880 Series*. Device-level enhancements include the following:

- Direct MOSFET Driver
- Low Power Idle Mode (LPIM) with < 60 mW typical power consumption when FXS_LOW_PWR termination type is used
- Added SPI Mode 0 and 3 support with no inter byte $\overline{CS}$ off time. Also supports the legacy MPI interface
- Added ZSI Mode support for a smaller number of interface signals and less expensive isolation. This mode is supported by many residential gateway SoCs.
- New Supervision ADC for advanced testing, improved calibration and adaptive power management

The *VP-API-II* takes advantage of these and other enhancements in the *Le9641* and offers greater programmability and more efficient operation.

Please refer to the *Le9641 Single Channel miSLIC Device Data Sheet* for more details about this device.

Figure 29, “ZLR964124L Line Module Schematic” on page 42 shows the *Le9641* and associated components. The designer should note the following changes from previous *VE880*-based designs:

- *Le9641* does not have separate ground pins. All ground is routed through the metal ePAD, which is also used for thermal heat dissipation
- $RREF_1$ must be a precision 0.5% 25ppm resistor (75.0 KΩ) in order to meet the data sheet specifications. A 1% resistor maybe be used, but some device parameters may not meet the data sheet specifications. Some parameters that would be affected would be VBAT, VOC, ILA,VeriVoice Accuracy etc.
- Note that a pull-up or pull-down at pin 16 ($\overline{ZSI}$) is used to select the mode of communication with the host processor, PCM/SPI or ZSI. The ZLR964124 module does not support ZSI mode. This design uses PCM/SPI mode, ZSI pulled up. If ZSI mode is desired, the ZSI pin should be pulled to ground with a 10Kohm resistor. Only a single device is supported when in ZSI mode.

4.3 Line Interface Circuit

Figure 3 below shows the *ZLR964124's* line interface circuit. The complete circuit is shown in Figure 29 on page 42.

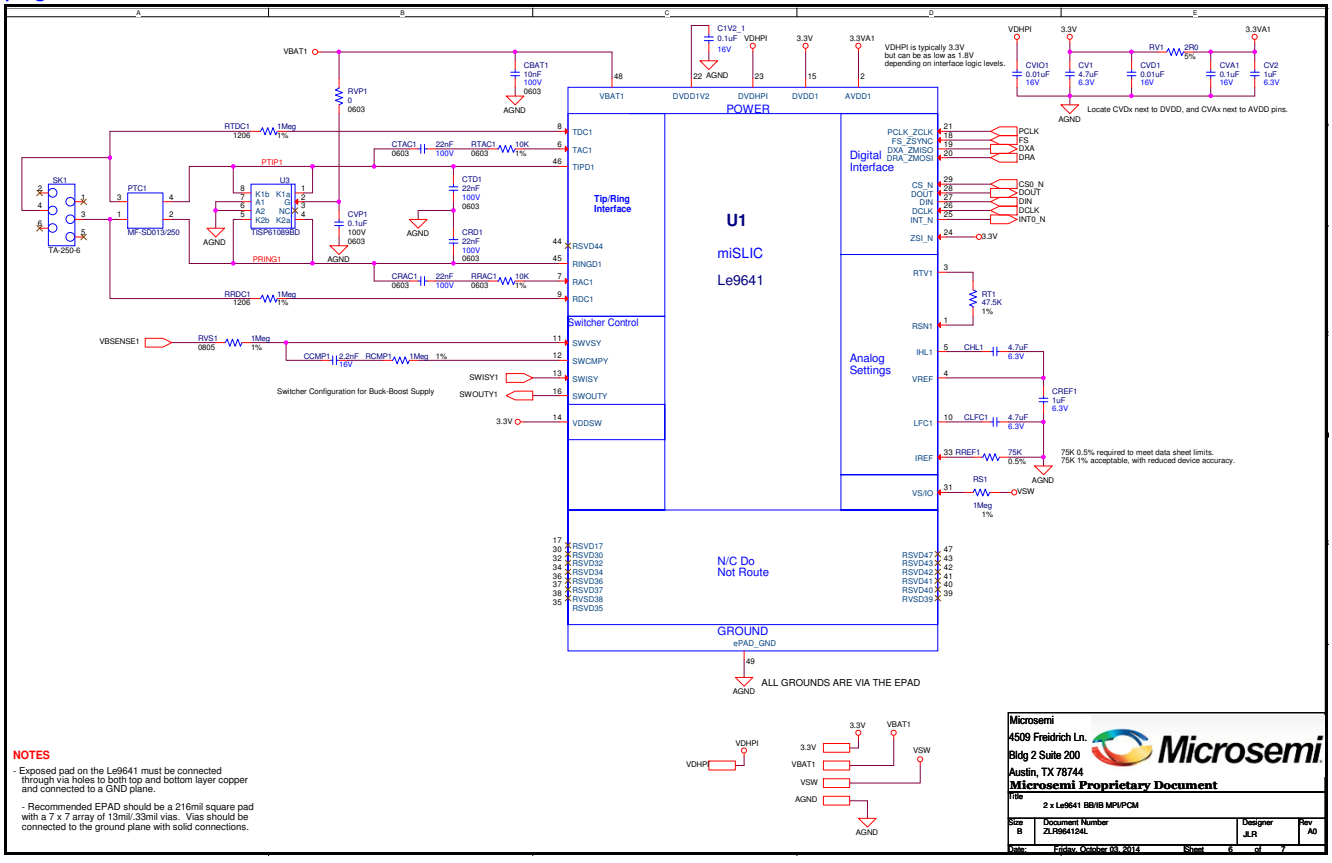


Figure 3 - ZLR964124 Line Interface Circuit

Please note the following changes from *VE880* designs:

- The AC sense capacitors $CTAC_{1,2}$ and $CRAC_{1,2}$ are now 0.022uF (whereas *VE880* designs required them to be 0.068uF, a less common and potentially more expensive value). Note that the values of the $RTAC_{1,2}$ and $RRAC_{1,2}$ resistors have changed to 10 K.
- The DC sense resistors such as $RTDCA_x$ are now 1.0 MΩ per leg as compared to 400 KΩ on the *VE880*. This reduces the leakage current in the Low Power Idle Mode.
- No external high-voltage (*BAS21*) diodes are needed to protect the SLIC against positive surges.

4.3.1 Surge Protection

The *ZLR964124 Line Module* design has series current limiting and shunt voltage limiting for lightning and surge protection as shown in "ZLR964124 Line Interface Circuit" on page 13. This protection design uses Positive Temperature Coefficient (PTC) thermistor devices to limit surge current. The purpose of the PTC is to provide overcurrent protection during a power cross event. During a typical transient surge (i.e. due to a lighting strike), the PTC simply acts like a low-value resistor limiting the surge current to a manageable level. In the event of a power cross, the PTC behaves like a fuse. Since a power cross is a long term event, the PTC will heat up and transition

from a low resistance to a high resistance. After the event has been cleared, the PTC will return to a low resistance value once again, assuming the ratings of the PTC have not been exceeded.

Voltage limiting is provided by *Bourns TISP61089BDR* SLIC Programmable Overvoltage Protector or equivalent. This device provides a voltage clamp that is triggered by voltages slightly more negative than V_{BATH}. This protection scheme protects both the Tip and Ring leads of the surged channel, limiting the voltage applied to either the TIPD or RINGD pins of the device.

Overcurrent protection is provided by the *Bourns MF-SD013/250* dual PTC devices (or equivalent) which ramp to a high impedance value once the threshold current has been exceeded. Below this threshold current, the devices act as nominal 7 Ω resistors. The hold current at 23°C is 0.13 A. The *MF-SD013/250* is a dual PTC that uses a polymer technology. Other PTC options are available such as single polymer PTCs and single or dual ceramic PTCs with nominal resistance of up to 50 ohms. Be aware that the effective resistance of ceramic PTCs is considerably less in the presence of fast-edged transients. Also, note that higher values PTCs will limit the maximum available ringing voltage. AC coefficients should take the PTC resistances into account or performance may not be as expected. Microsemi has standard coefficients available for various PTC values.

The protection solution provided by the Microsemi reference design is suitable for environments with relatively low surge activity such as intra-building applications defined in *Telcordia GR-1089-CORE*. This design is also suitable for *ITU-T K.21* requirements. Contact Microsemi Customer Applications if higher protection levels such as *Telcordia GR-1089-CORE* inter-building protection is required.

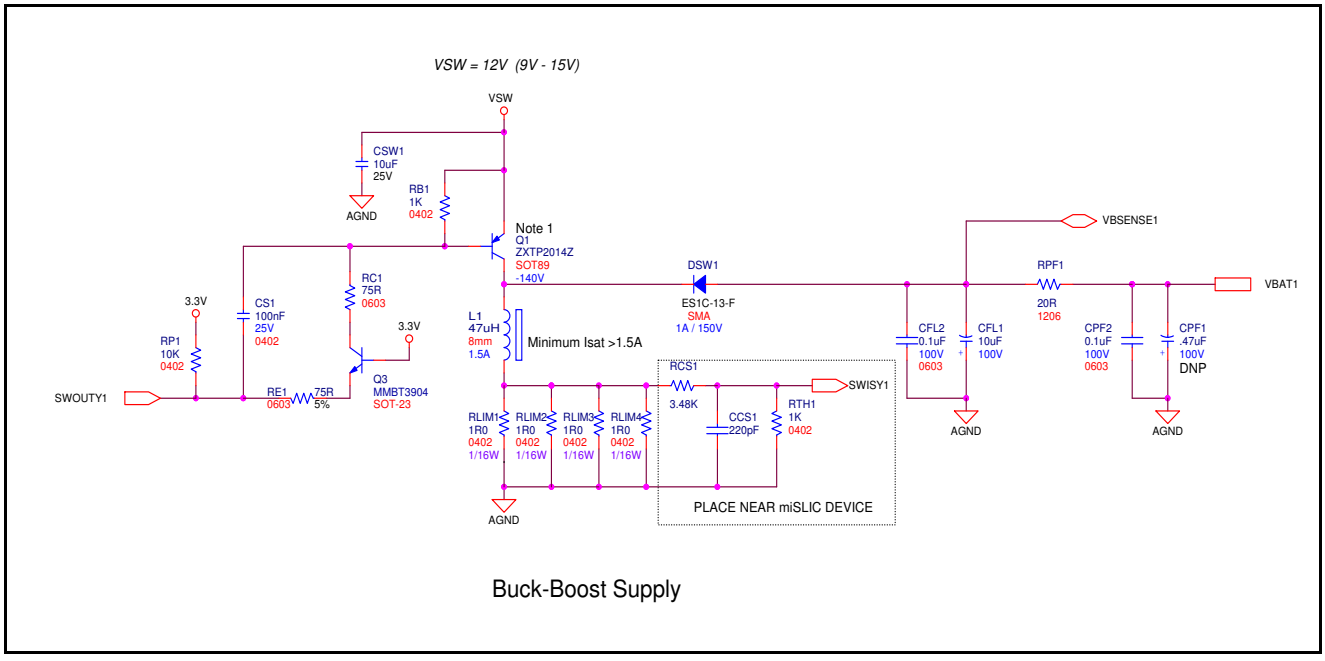
4.4 Buck-Boost Power Supply

The Buck-Boost switching power supply for the *Le9641* device produces a single tracking battery voltage. Unlike other full tracking designs though, the Buck-Boost is referred to as fixed tracking, as it does not track ringing. Refer to Figure 4 for the schematic of the Buck-Boost switcher on the *ZLR964124*.

The line module is designed to operate from 12 V (9 to 15 V) nominal input. The design can be modified to support a 5V (3.7 to 6 V) nominal input. Ringing capability is reduced to 3REN when operating from 5 V, and 1REN when operating from 3.7 V. Operation down to 3.7 V is intended for litium ion battery backed Wireless Local Loop (WLL) systems. Additionally, the 12 V design can operate down to 6 V, supporting 3REN ringing loads, with only a profile change. The 12V design cannot effectively operate below 6V without circuit changes.

The 12V Buck-Boost uses a low Vce saturation PNP transistor (FZT955 type) as the primary power switch for the supply. The PNP is switched at 24kHz when in the idle state to maximize power efficiency. When in the off hook or ringing states, the switching frequency is changed to 128kHz to increase power capability.

The Buck-Boost design for the Le9641 measures only 0.49 sq^2 (3.15 cm^2) on a two layer PCB with all components on the top side. This provides for an ultra small footprint while still fully supporting customer requirements. The design makes use of a smaller SOT89 PNP and 8mm inductor footprints.



Buck-Boost Supply

Figure 4 - ZLR964124 Buck-Boost Switching Regulator

4.4.1 Capacitor/Filter Requirements

The Buck-Boost power supply uses a 10 uF 100 V electrolytic capacitor for output filtering. An electrolytic is used because higher capacitance is required for good filtering due to the lower operating frequency of the supply. A supplemental 0.1 uF ceramic capacitor is used to remove high frequency noise. The electrolytic capacitor should have a ripple current rating of >150 ma at 100kHz. Resistor RPF1 and capacitors CPF1 and CPF2 provide an additional low pass filter. For many applications CPF1 may not be required. It is recommended that a footprint be provided on the PCB for CPF1 in case it is needed. CPF1 is show as a 0.47 uF 100 V general purpose electrolytic. A 0.47 uF 100 V X5R/X7R ceramic capacitor could also be used. CPF2 is a 0.1 uF 100 V X5R/X7R ceramic capacitor.

4.4.2 High Voltage PNP

The Buck-Boost power supply uses a 140 V PNP power transistor as the main power switch. This transistor is designed for applications where low Vce saturation voltage is important. When the transistor is turned on the collector current can go as high as 1.5 A. The thermal tab (collector tab) of the transistor should have a thermal pad of at least 0.25 cm^2. Microsemi Buck-Boost designs are validated using Diodes ZXTP2014/ZX5T955/FZT955 family devices. Substitution of any other device besides the devices listed below is not recommended. Use of other devices can result in transistor failure. The PNP transistor requirements for the buck-boost switcher are shown below

- Type: PNP, Vce= 140 V, Low Vce sat, Diodes/Zetex ZXTP2014 or equivalent.
- Suitable Packages: SOT-223, SOT89, or equivalent
- Sources: Diodes/Zetex ZXTP2014/ZX5T955/FZT955, Central Semiconductor CZT955.

4.4.3 Inductor Requirements

The Buck-Boost power supply has been designed to make use of low cost unshielded/semi-shielded inductors. The inductor should not be placed in close proximity to noise sensitive circuits. See the later section on xDSL compatibility. The ZLR964124 line module has been designed to support 8mm size 47 uH inductors. 47 uH

inductors with saturation current rating of 1.5 A and greater are acceptable. Inductance should not be degraded more than 30% at rated current.

Example Inductors for 12 V applications:

- Bourns SRN8040-470M, Isat=1.5 A
- Taiyo Yuden NR8040T 470M, Isat=1.5 A

It should be noted the not all inductors are suitable for switching power supplies. This particularly applies to toroid style choke inductors that are intended for filtering applications. These types of inductors have high core losses that can result in excessive heating of the core. This results in poor supply efficiency and over time can result in catastrophic failure of the inductor.

4.4.4 PNP Transistor Driver

The Le9641 has an integrated high current driver, SWOUT, which is capable of directly driving N-ch MOSFETs. A minimal amount of additional circuity is required to drive the PNP power transistor, Q1. The driver includes two paths for base current. Capacitor CS1, 0.1uF X7R, is directly connected between the SWOUT pin and the base of Q1. This provides high instantaneous currents to facilitate fast PNP turn on and turn off times. Additionally, there is a small signal NPN transistor, MMBT3904, that functions as a level shifter and base current limiter. In Buck-Boost designs the SWOUT signal is a 3.3V level. The VDDSW power pin (pin 14) is connected to 3.3V. The base of the NPN is connected to, DVDD (3.3V), and the emitter of the transistor is driven. Resistor RE1 is in series with the emitter and sets the maximum DC base current limit to about 35ma. Resistor RC1 is in series with the collector of the NPN and serves to provide some voltage drop so that the NPN does not dissipate too much power. Both resistors are 75ohm 0603. It is not recommended to change the value of these resistors. For designs operating at less than 6V input, RC1 must be changed 0ohms. Without this change the NPN will become saturated which will result in the emitter current flowing from the NPN base instead of the collector, reducing PNP base current. Please consult with Microsemi Applications if a single design is required to operating from less than 6V to 12V or greater.

4.4.5 Current Sense, RLIM

Resistors $RLIM_{1,2,3,4}$ implement a low cost 0.25ohm current sense resistor. The resistors are 1ohm 5% 0402 type. The combination of $RLIM_{1,2,3,4}$, RCS1, and RTH1 set the cycle-by-cycle current limit threshold for the SWIS pin. In this case, the threshold is set to a value just above the current rating of the inductor, 1.8A. If peak inductor current reaches 1.8A the current switcher cycle is terminated preventing the inductor for becoming saturated and protecting the power transistor. It is not recommended to change the values of the resistors. Capacitor CCS1 is used to filter excess noise from reaching the SWIS pin. High noise in the SWIS path can result in poor switcher stability. Components RCS1, CCS1, and RTH1 should be placed near the device SWIS pin.

4.4.6 Buck-Boost Compatibility with xDSL

Switching power supplies are inherently noisy and the Buck-Boost switching regulator is no exception. The collector node of the PNP will have high dv/dt signals with a voltage swing in excess of 100 V at a frequency of up to 128 kHz. Placing the switcher in close proximity of a DSL AFE can and most likely will cause degraded performance of the DSL interface. It is therefore extremely important that the PNP, inductor, and associated circuitry be placed at least one inch (2.5 cm) away from any DSL AFE signals. On two layer PCBs it is important to pay attention to ground continuity and ground return paths for the high peak currents of the power supply. These currents should not flow though the same ground that is also being used to shield DSL AFE signals.

4.4.7 Low Input Voltage Option, 3.7V to 6V

The Buck-Boost supply can support operation from nominal 5V supplies. The supply can support up to 3REN loads from a 4.75V input or 1 REN from 3.7V. Referring to Figure 4, circuit changes are required for the Buck-Boost supply to operate at low input voltage. A modified device profile is also required.

- Inductor L1 changes to 22uH 1.8A

- Resistor RC1 changes to 0 ohms

Consult with Microsemi Applications if the same design is required to operate from less than 6V to 12V or greater.

4.5 Inverting Boost Power Supply

The Inverting Boost topology is basically a boost converter power stage with a charge pump inverter on the output. The Inverting Boost battery supply for Le9641 has been optimized for the lowest possible cost while maintaining good efficiency and power capability. On a 2 layer PCB with all components on the top side, the supply only requires 0.38 sq^2/2.4 cm^2.

Inverting Boost uses an N-channel MOSFET switching at up to 512kHz to produce battery voltages up to -90V. The device has an internal clamp that will not allow battery voltage to exceed the allowed limit. This is intended to protect the MOSFET from overvoltage. The Nch MOSFET is specified as a logic level 100V rated device in a small SOT23 or SOT6 package. Larger packages such as SOT223 or SO8 can be used but are not necessary for typical commercial applications.

The supply operate in three configurable power modes to optimize efficiency and power capability. When in the *Low Power Idle* state the supply operates at 24kHz. When in the *Active* state the supply frequency changes to a duty cycle limited 512kHz. *Ringing* state is also 512kHz but with duty cycle maximized to allow maximum power capability.

Inverting Boost can be used with input voltages as low as 4.5V. An alternate device profile is required to optimize the supply for the lower input voltage.

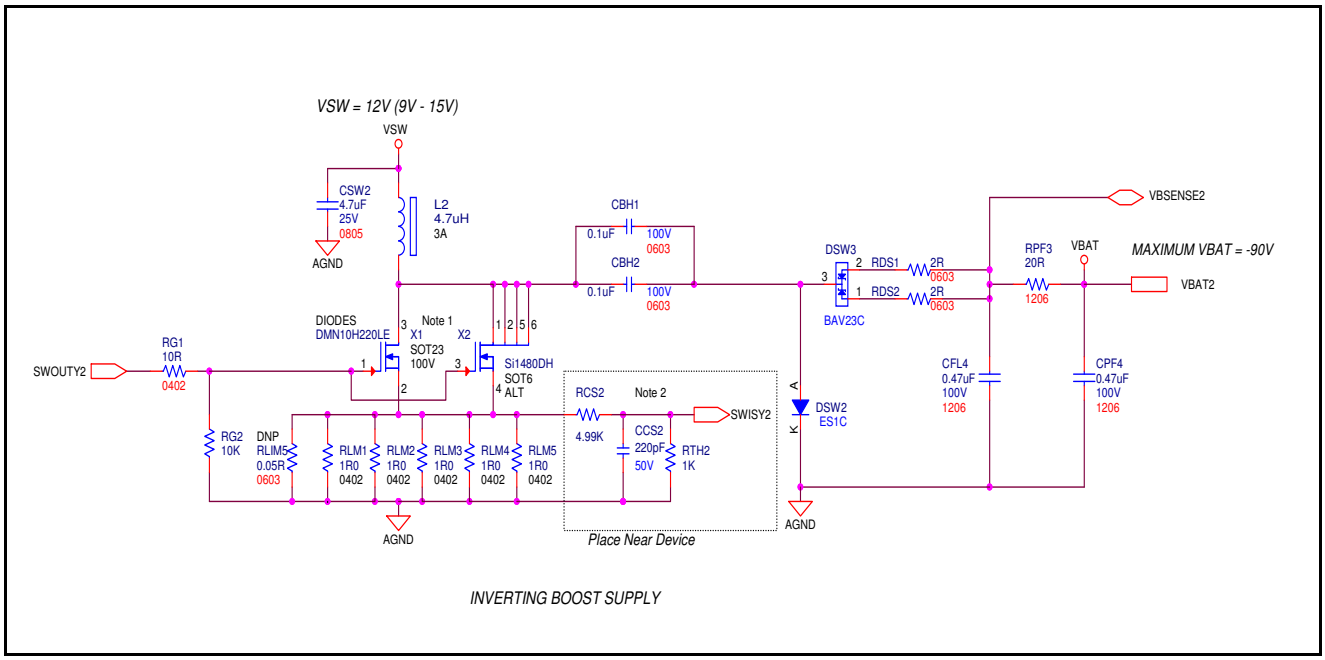


Figure 5 - ZLR964124 Inverting Boost Switching Regulator

4.5.1 Capacitor/Filter Requirement

The Inverting Boost uses a simple PI type output filter, CFL4, RPF3, ad CPF4. The primary output filter capacitor, CFL4, is a single 0.47uF 100V X5R/X7R 1206 ceramic type. An additional RC post filter is used where RPF3 is 20ohms and CPF4 is another 0.47uF ceramic.

4.5.2 MOSFET Requirements

The MOSFET requirements for the Le9641 Inverting Boost switcher design are:

- Type: N-Channel, Logic Level (V_{GS}: 4.5 V) MOSFET
- Drain-Source Voltage Rating, V_{DSS}: 100 V
- Static Drain-Source On-Resistance, $R_{DS(on)}$: <250 mΩ recommended
- Total Gate Charge $Q_{G(total)}$ at V_{GS} = 4.5 V: <8 nC recommended
- Suitable Packages: SOT-23, SOT23-6

Please note that $R_{DS(on)}$ (MOSFET on state drain to source resistance) and gate charge impact overall supply efficiency. Higher $R_{DS(on)}$ will result in higher power dissipation while the MOSFET is conducting. Gate charge is the measure of how much current vs time that is needed to turn the MOSFET on. A higher gate charge MOSFET will take longer to turn on/off for the same amount of driver current. Therefore gate charge losses are noticed during the on and off transition of the MOSFET. These losses become higher with increased switching frequency. Typically there is a trade off between $R_{DS(on)}$ and Q_G. Higher $R_{DS(on)}$ devices will have lower gate charge and vise versa, although newer devices have been successful at reducing both. Recommended SOT23 devices include the *Diodes DMN10H220L, International Rectifier IRLML0100TRPbF,* and *Vishay Si2392DS.* The power numbers included in Chapter 6 were taken using the *International Rectifier IRLML0100TRPbF*. Use of a different MOSFET may result in different overall efficiency numbers. Higher $R_{DS(on)}$ MOSFETs up to 500 mΩ may be used, but ringing limitations should be expected due to the limitation of SOT23 thermal capacity as well as efficiency reduction.

The ZLR964124 layout supports both SOT23 and SOT6/SOT23-6/SOT363 MOSFETpackages.

For designs requiring 85Vpk ringing, 100V MOSFETs should be avalanche rated or a 150V MOSFET should be used. At this time, there are no sutable 150V logic level rated MOSFETs in SOT23 or SOT6 packages.

4.5.3 MOSFET Driver

The Le9641 SWOUT pin is capable of directly driving a Logic Level Nch MOSFET. The VDDSW, pin 14, is the power pin for the driver circuit. For MOSFET based power supplies, VDDSW requires a 5V (5.5V Absolute Maximum) power source. The 5V current requirement is very low, typically less than 2ma. The current can be estimated by multiplying the MOSFET total gate charge (at 4.5V Vgs) times the switching frequency. For example, the MOSFET used on the Inverting Boost circuit has a typical Qg of 2.5nC. The Inverting Boost maximum switching frequency is 512Khz. There is also some current due to the 10K gate pull down resistor.

$$I_{VDDSW} = ((2.5 \times 10^{-9}) \times 512000) + (5V/10K \times D)$$; where D is duty cycle which is load dependant.

I_{VDDSW} = 1.53mA, assuming a 50% duty cycle.

Systems that do not have a 5V supply available can use one of the following low cost circuits to create a 5V supply from a 12V input. The 5V supply does not have to be accurate, +/-10%. It should be greater than 4.5V with an absolute maximum of 5.5V.

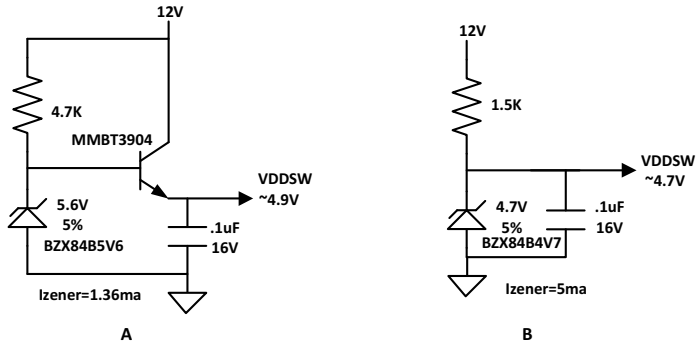


Figure 6 - VDDSW Regulator Circuits

Circuit option A uses less power, only requiring 1.36ma to bias the zener diode. Circuit option B does not require an extra transistor, but does require higher zener diode current, 5ma, since the resistor must also pass the VDDSW pin current. For good voltage control, zener diodes that are specified at 5ma (Diodes BZX84B5V6 or equiv.) are preferred. If 1N52xx type diodes are used, zener bias current may need to be increased since these are usually specified at 20ma.

Circuit A could potentially power multiple devices. Circuit B can only support a single Le9641 device with a low gate change MOSFET.

4.5.4 Inductor Requirements

For typical applications, a 4.7 uH inductor with a 3 A saturation rating is recommended. If power requirements are lower, such as 3 REN ringing then a 2.5 A inductor may be suitable. Note that the current sense threshold should be appropriate to the inductor.

Example Inductors for 12V applications:

- Bourns SRN6045-4R7M, Isat=4 A
- Taiyo Yuden NR6045T 4R5M, 4.5 uH, Isat=4 A

It should be noted the not all inductors are suitable for switching power supplies. This particularly applies to toroid style choke inductors that are intended for filtering applications. These types of inductors have high core losses that can result in excessive heating of the core. This results in poor supply efficiency and over time can result in catastrophic failure of the inductor.

4.5.5 Output Rectifier

The minimize costs, output rectifier DSW3 has been chosen to be a BAV23C. BAV23C (common cathode) is a 200V dual small signal diode in a SOT23 package. 2 ohm 0603 resistors, RS1 and RS2, are placed in series with each diode to help the diodes evenly share current and also to limit peak currents to acceptable levels. This configuration does not require any more PCB space than a typical ES1C SMA rectifier that would have normally been used. A BAV23A common anode version can also be used as long as it is insured that the diode direction is kept the same, anode toward the output. The BAV23 was specifically chosen for its high surge current ratings relative to other small signal diodes. Devices used in this application must have a repetitive peak current rating of >600 ma per diode. DSW3 can also be an ES1C/ES1D if desired. In this case RS1 and RS2 are not required.

Rectifier DSW2 must be an ES1C/ES1D type ultra-fast recovery rectifier. Peak currents for this device are too high to allow use of a small signal substitute. DSW3 can also be an ES1C.

4.5.6 Current Sense, RLIM

Resistors $RLM_{1,2,3,4,5}$ implement a low cost 0.2 ohm current sense resistor. The resistors are 1 ohm 5% 0402 type. The combination of $RLIM_{1,2,3,4,5}$, RCS1, and RTH1 set the cycle-by-cycle current limit threshold for the SWIS pin. In this case, the threshold is set to a value just near the current rating of the inductor, 3 A. If peak inductor current reaches 3 A the current switcher cycle is terminated preventing the inductor for becoming saturated and protecting the MOSFET. It is not recommended to change the values of the resistors. Capacitor CCS1 is used to filter excess noise from reaching the SWIS pin. High noise in the SWIS path can result in poor switcher stability. Components RCS1, CCS1, and RTH1 should be placed near the device SWIS pin.

The low cost option does result in reduction of power supply efficiency, particularly at higher power levels. An alternate option is to use a 0.05 ohm 2% 0603 resistor (RLIM5). This type of resistor is usually more expensive but power supply efficiency is improved. If the 0.05 ohm resistor is used, then resistor RCS1 must be changed to 1 K ohms and RTH1 is changed to 2 K ohms. This is required to maintain the same 3 A current sense threshold.

The current limit threshold is defined by the equation:

$$I_{LIM} = 0.1\ V*(R_{CS}+R_{TH}/R_{TH}*R_{LIM})$$

The parallel (thevenin) value of RCS and RTH should be close to 1 Kohm to maintain good high frequency filtering with CCS, which is typically 220 pF.

4.5.7 Pump Capacitor, CBHx

Capacitors CBH1 and CBH2 are critical to good supply performance. These capacitors should have good capacitance stability with voltage bias. For lower voltage ringing designs, 50Vrms, only a single .1uF 0603 capacitor is necessary for CBHx. For greater than 50Vrms ringing both CBH1 and CBH2, 2 x .1uF 100V 0603 ceramic, is required. Alternately, a single .22uF 100V 0805 ceramic can be used. It is not recommended to use smaller body size capacitors for CBHx than what is recommended.

When using a single .1uF 0603 100V capacitor, it is also necessary to use an 80V max device profile. Attempting to use a single .1uF 0603 capacitor for CBH with a >50Vrms ringing profile can result in excessive voltages on the MOSFET.

4.5.8 Compatibility with xDSL

Switching power supplies are inherently noisy. The drain node of the MOSFET will have high dv/dt signals with a voltage swing up to 90 V at a frequency of up to 512 kHz. Placing the switcher in close proximity of a DSL AFE can and most likely will cause degraded performance of the DSL interface. It is therefore extremely important that the MOSFET, inductor, and associated circuitry be placed at least one inch (2.5 cm) away from any DSL AFE signals. On two layer PCBs it is important to pay attention to ground continuity and ground return paths for the high peak currents of the power supply. These currents should not flow though the same ground that is also being used to shield DSL AFE signals.

Relative to the Buck-Boost design, the Inverting Boost would be considered more xDSL friendly since any noise interference would only affect frequency bins at 512Khz and harmonics versus 128Khz.

4.6 Adaptive Ringing and Power Limiting

Buck-Boost designs support an optional Adaptive Ringing feature. This feature is useful for designs that desire to limit the maximum amount of current drawn from the VSW supply. The feature would generally be used with a power limited device profile. A power limited profile limits the headroom of the Buck-Boost power supply to prevent unwanted high current surges during normal operation. The VP-API II option command below is an example:

api so 100 -d VP_DEVICE_OPTION_ID_ADAPTIVE_RINGING 40 83 VP_ADAPT_RING_SINGLE_BB_TRACKER

Using a power limited device profile and applying the adaptive ringing option above, a Buck-Boost design can support 60Vrms ringing for ringing loads up to 3REN, then fall back to 50Vrms for ringing loads up to 5REN.

Absolute VSW current is limited to no more than 350ma in this case. Note that the 12V input supply should be well regulated in this case and should not vary more than +/-1V.

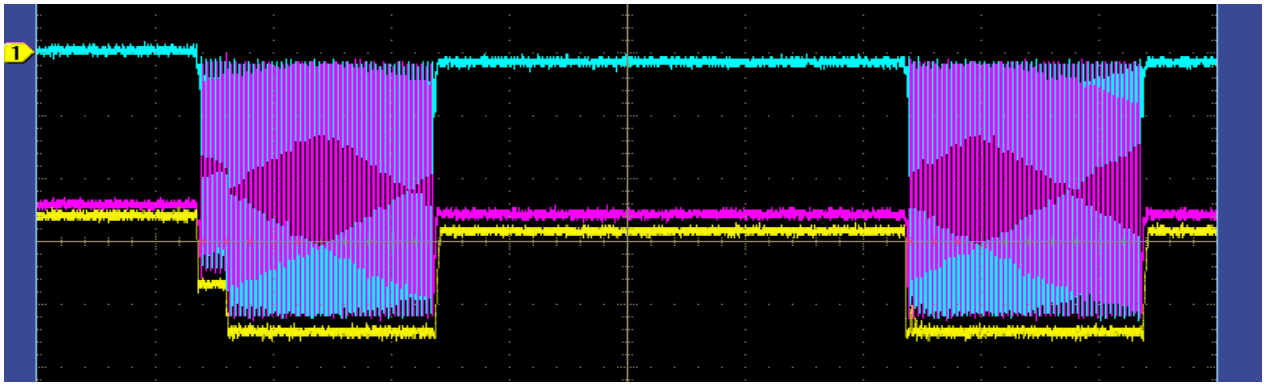


Figure 7 - Adaptive Ringing

4.7 Voltage Sense, Switcher Optimization and Power Measurement

The *Le9641* has the ability of measuring the switcher input voltage VSW. A 1.0 MΩ, 1% resistor is connected to between VSW and the pin I/O/VS which can be configured as an analog sense input. This allows the designer to monitor VSW and make switcher optimizations based on its level. This can be valuable in case a back-up battery is used. Furthermore, using VSW and the switching frequency and ON Time, real-time power usage may be calculated.

5.0 Module Configuration

5.1 Introduction

The *ZLR964124 Line Module* is programmed through the *VoicePath Application Program Interface (VP-API-II)*. This API hides the complexity of the device and its internal registers and provides a much simpler interface to the software engineer. The *VP-API-II* software requires *Profiles* to initialize the AC, DC, signaling, supervision, host interface, and switcher settings. Default *Profile* values are stored on Module ID ROM (MID) memory devices on the line modules to enable “out-of-the box” operation. Most profiles can be easily modified using the *Profile Wizard* software tool.

5.2 Module ID ROM (MID) Default Profiles

The MID on the *ZLR964124L* uses the same *AC, Tone, Cadence*, and *Caller ID Profiles for both devices*. They have different *Device*, *DC*, and *Ringing Profiles*, due to the different switcher topologies for each channel.

5.2.1 Device Profile

The *Device Profile* sets the PCM clock (PCLK or ZCLK) frequency, PCM transmit edge, transmit and receive clock slots, and interrupt types and GPIO/sense pins. The device profile also selects the choice of 3.3V or 5V for the VDDSW supply. Buck-boost uses 3.3V for the VDDSW pin supply, while Inverting Boost requires a 5V supply.

Channel 2, Inverting Boost, uses a 90V limited device profile. See Chapter 4 for design options and limitations.

5.2.2 AC Profile

Used for programming the transmission characteristics of the system, the AC Profile holds the programmable gain and filter coefficient data.

The default *AC Profile* provides a 600 Ω input and balance impedance with -6 dBr receive level and 0 dBr transmit. It also takes into account the nominal 7 Ω PTC series resistance per leg.

5.2.3 DC Profile

The *DC Profile* contains the parameters for the *ZLR964124 Line Module* to control supervision thresholds, DC feed, and other switcher settings. It is not compatible with the *DC Profiles* that were used for the *VE880 and VE890* due to new features in the *miSLIC* devices.

The MID settings for the *DC Profile* include an Open Circuit Voltage (VOC) of 48 V, an Active Mode Current Limit (I_{LA}) of 25 mA . The loop hook detection thresholds are 11 mA for the *Active* state and 22 V for the *Low Power Idle Mode* state. The hook debounce time is 12 ms. The Ground Key detection threshold is 18 mA with 16 ms debounce.

5.2.4 Ringing Profile

The *Ringing Profile* is set in the *ZLR964124L* MID to generate a 70.7 V_{PK} (50 V_{RMS}) with no DC offset at 25 Hz. Ring trip is set to integrate over half-wave (AC only) with a ring trip threshold (R_{TTH}) of 21 mA. The ringing current limit (I_{LR}) set to 54 mA.

The *Ringing Profile* for the Buck-Boost uses fixed mode ringing where VBAT1 is fixed at 80V during ringing. Inverting Boost uses a tracking mode ringing.

5.2.5 Tone Profile

The MID does not include any *Tone Profiles*.

5.2.6 Ringing Cadence Profile

The *Ringing Cadence Profile* sets the cadence that is associated with ringing. The default *Mini-PBX* ringing cadence configuration is 2 second ON and 4 seconds OFF.

5.2.7 Tone Cadence Profile

The *Tone Cadence Profile* sets the cadence that is associated with call progress tones. These tones normally include dial tone, ring back, busy, congestion and call waiting tones.The MID does not include any *Tone Profiles*.

5.2.8 Caller ID Profile

The *Caller ID Profile* sets the signaling that is used for on-hook and off-hook Caller ID. The MID does not include any *Caller ID Profiles*.

5.3 Profiles Generated with Profile Wizard

As an alternative to using the default profiles that are provided on the MID, the user can create new ones or edit the following profiles that are provided with the standard *Profile Wizard* distribution:

- ZLR964124L_SM2_LITE_REV2_9.VPW

These files contain *Device, AC, DC, and Ringing Profiles* and are available for use with the *VP-API-II* Lite software.

Customers who execute a Software License Agreement (SLA) for the *VP-API-II* software will have access to the following additional files as a part of the full *VP-API-II* license:

- ZLR964124L_SM2_FULL_REV2_9.VPW

These files contain *Device, AC, DC, Ringing, Tone, Cadence,* and *Caller ID* for over 44 countries.

5.3.1 Profile Wizard Menu

Figure 8 below shows the Main Menu of the Profile Wizard application with the *ZLR964124L* project file loaded. Please note that the *Tone, Cadence and Caller ID* require a license to the *VP-API-II* and are not available with the *VP-API-II Lite* version.

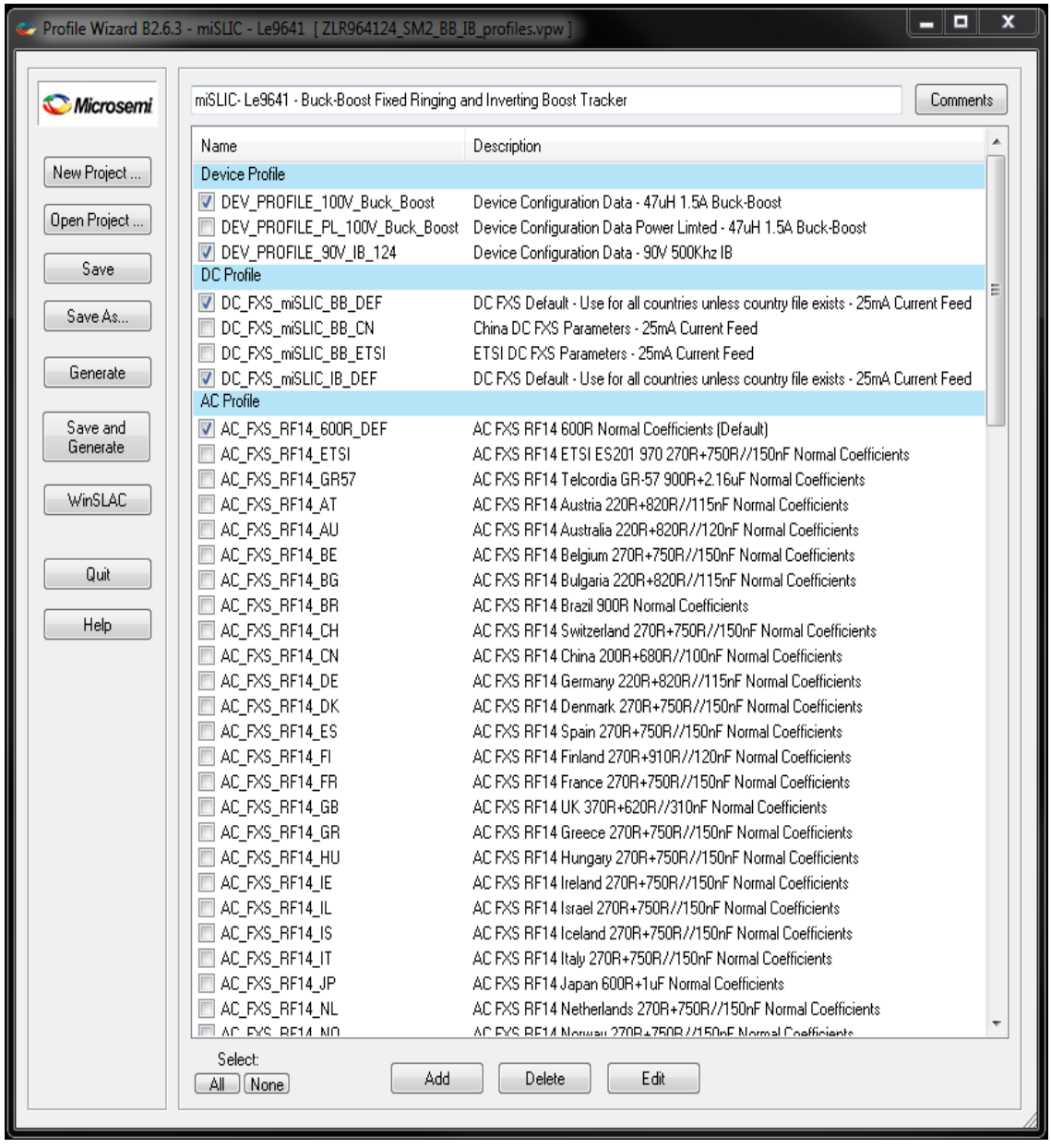


Figure 8 - Profile Wizard Main Menu - ZLR964124L Project File

Please refer to the *Le9641* data sheet for more information about the settings of the various profiles. Note that Microsemi has Profile examples for many countries.

5.3.2 Reviewing and Editing Profile Entries

The user can edit any of the profiles by clicking on the corresponding item and can check the ones that he or she needs for the project. As an example, Figure 9 shows the contents of the Ringing Profile. The user can change any of the values, such as the ringing frequency, amplitude, DC bias, by simply typing them in the corresponding boxes and pressing the “OK” button on the bottom.

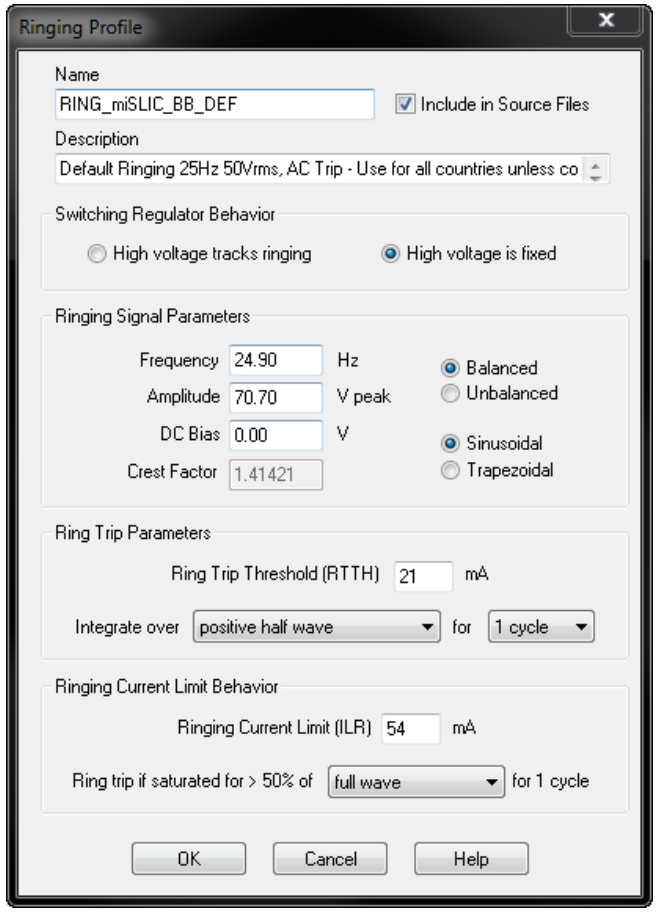


Figure 9 - Ringing Profile Configuration Example

After saving the Profile data, the user should press the “Save and Generate” button on the left panel of the Main Menu (Figure 8). This will generate new ***.c*** file with the selected profiles in the directory that is selected.

5.3.3 Running New Profiles

After completing the changes to Profile Wizard, the user should follow the following steps:

1. Start the *MiToolkit* application.
2. When *MiToolkit* starts up, it will display a list of applications. Run the *Mini-PBX* application.
3. When *Mini-PBX* starts, it will prompt for which serial port to use. If *VP-Script* is already running, *Mini-PBX* will know what port is being used. Note that the *ZTAP Support Package* software installation includes a Virtual COM Port Driver to support USB-to-serial UART interface on the *ZTAP* board.

4. Double click on the location of the line module. It is DIN CS0 or CS1 on the example shown in Figure 10 below.

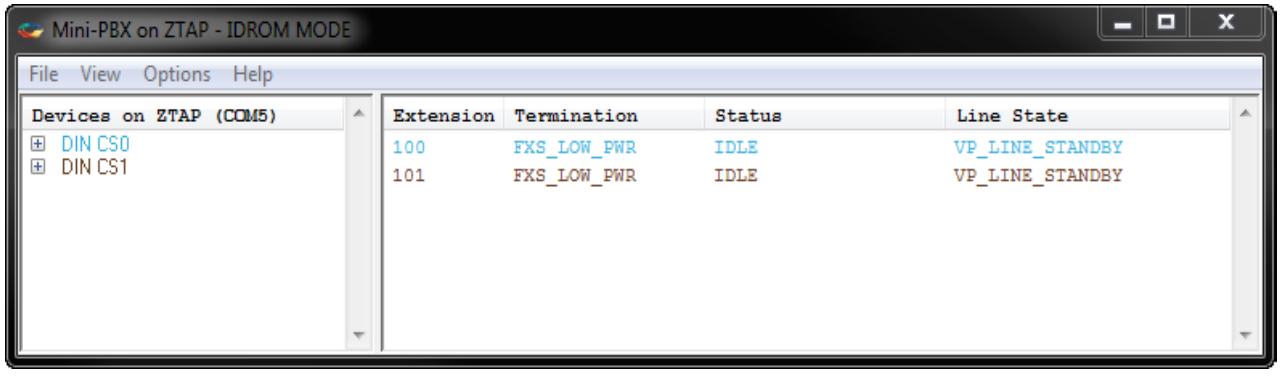


Figure 10 - Mini-PBX - Configuration Mode

5. After double clicking on the line module location, a new window will open as shown in Figure 11. The user should click the “Browse” button and select the newly created ***.c*** *Profile Wizard* file.

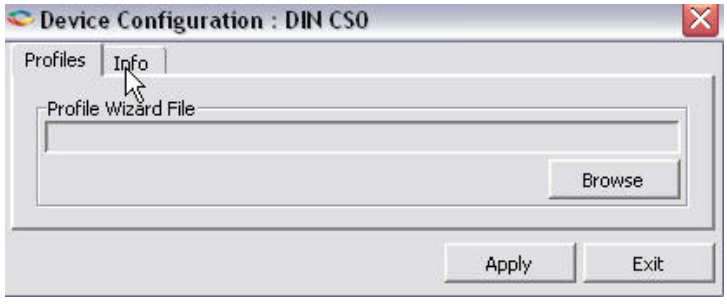


Figure 11 - Mini-PBX - Device Configuration

After *Mini-PBX* loads the new profiles, it will use its values. For example, new ringing values created in Section 5.3.2, *Reviewing and Editing Profile Entries*, on page 25 will now take effect.

6.0 Performance

6.1 Coefficients and WinSLAC

Coefficient files were generated from the Microsemi *WinSLAC* software and used to program filters and to set gains.

6.1.1 Schematic Used for Coefficient Generation

The following schematic was used to generate FXS coefficients for all Microsemi *miSLIC*™ devices. AC coefficients are compatible with older Ve880 and ZL880 VoicePort devices.

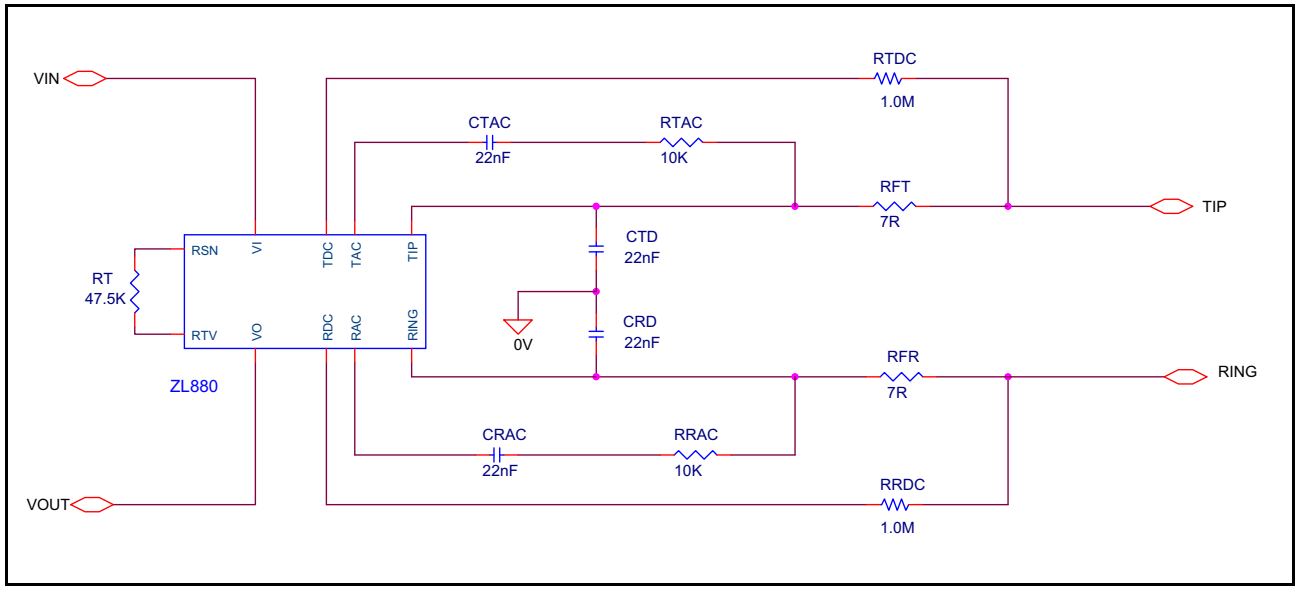


Figure 12 - WinSLAC Software Model for the Le9641 Schematic

Coefficients were generated as follows:

- 600 Ω termination
- Receive relative level = -6 dBr
- Transmit relative level = 0 dBr
- A-Law encoding (or µ-Law)

6.2 Narrowband Transmission Performance

The following graphs illustrate the narrowband (300 - 3400 Hz) transmission performance using a *W&G PCM-4*.

6.2.1 Return Loss

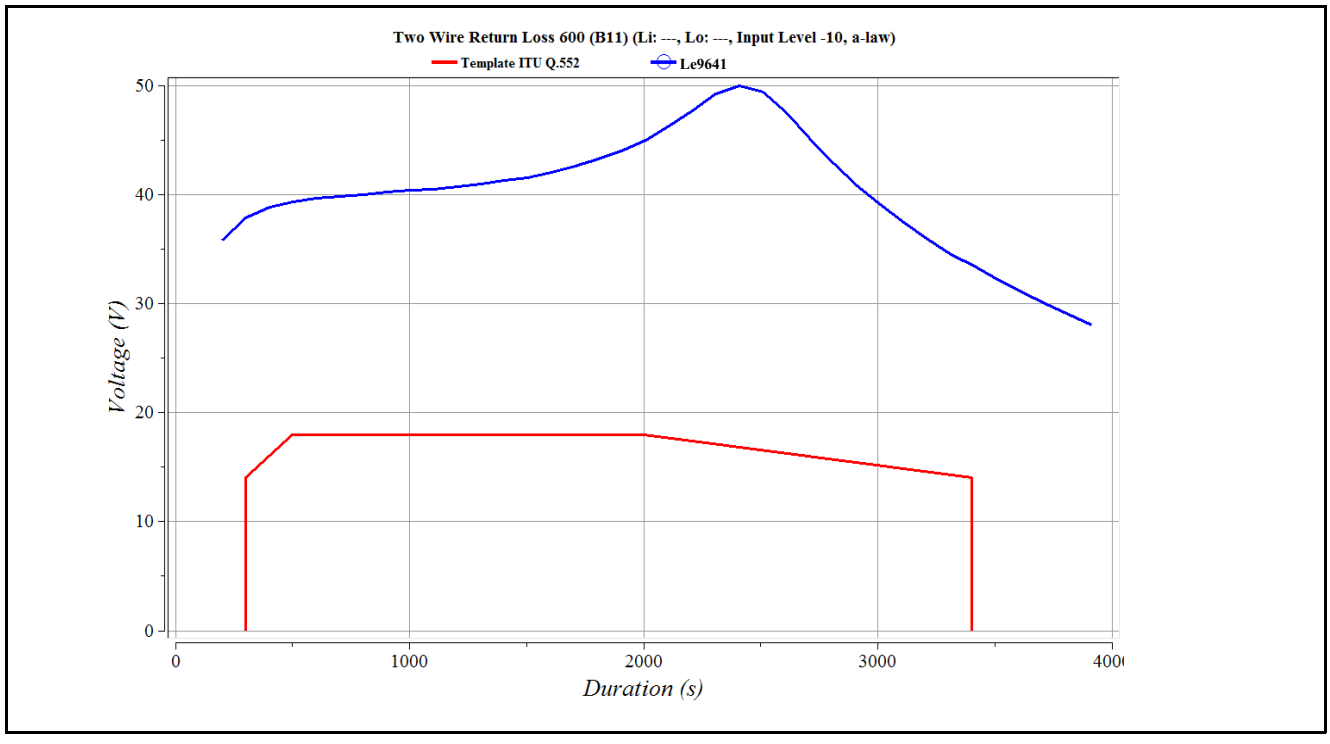


Figure 13 - Two-Wire Return Loss (Narrowband)

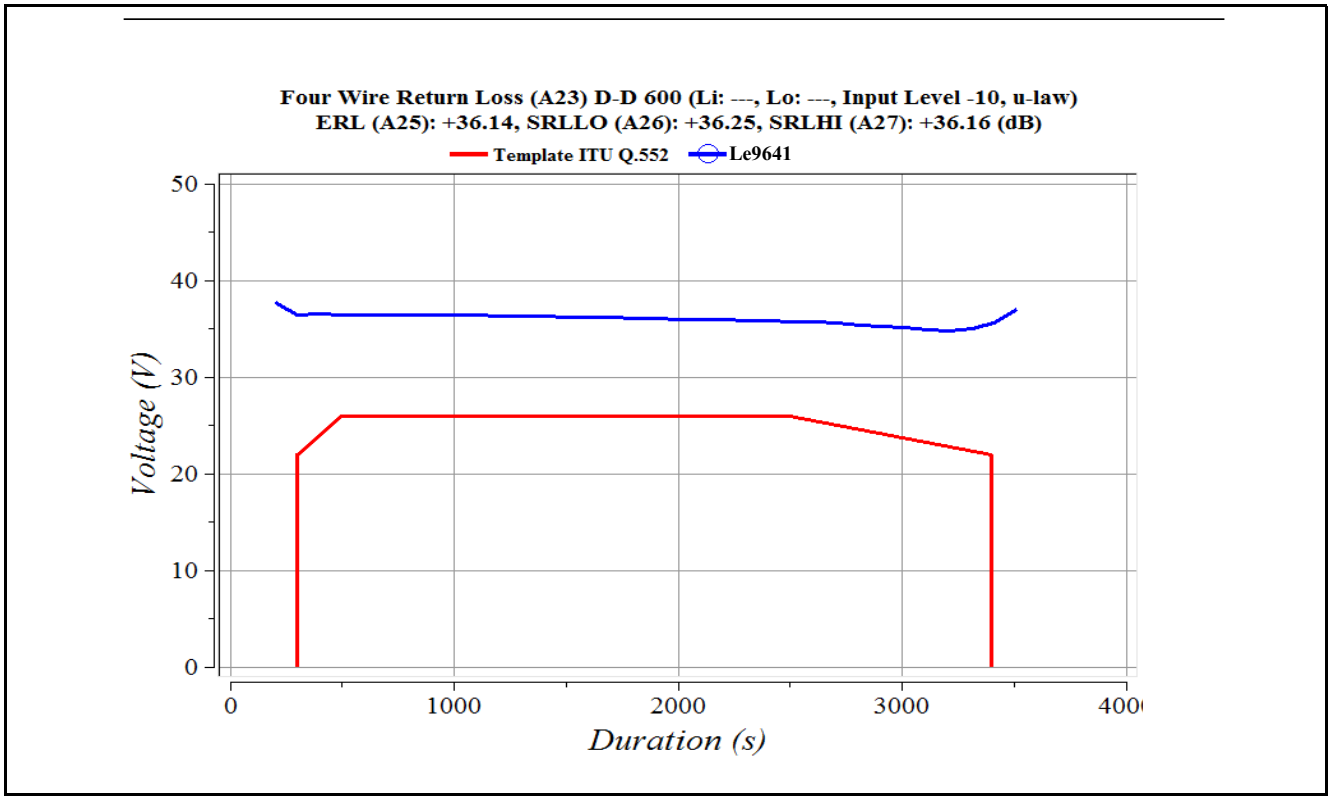


Figure 14 - Four-Wire Return Loss (Narrowband)

6.2.2 Attenuation Distortion and Gain

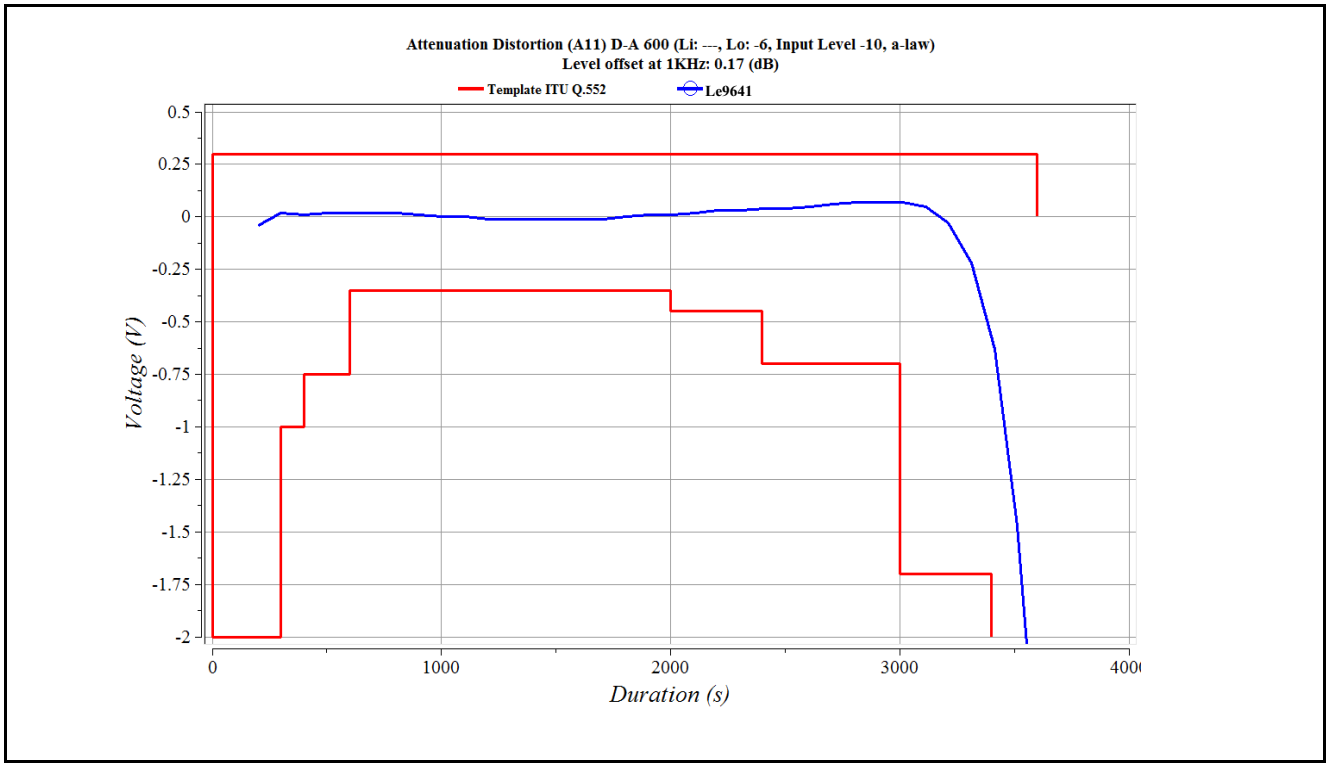


Figure 15 - Receive Path (D to A) Attenuation Distortion (Narrowband)

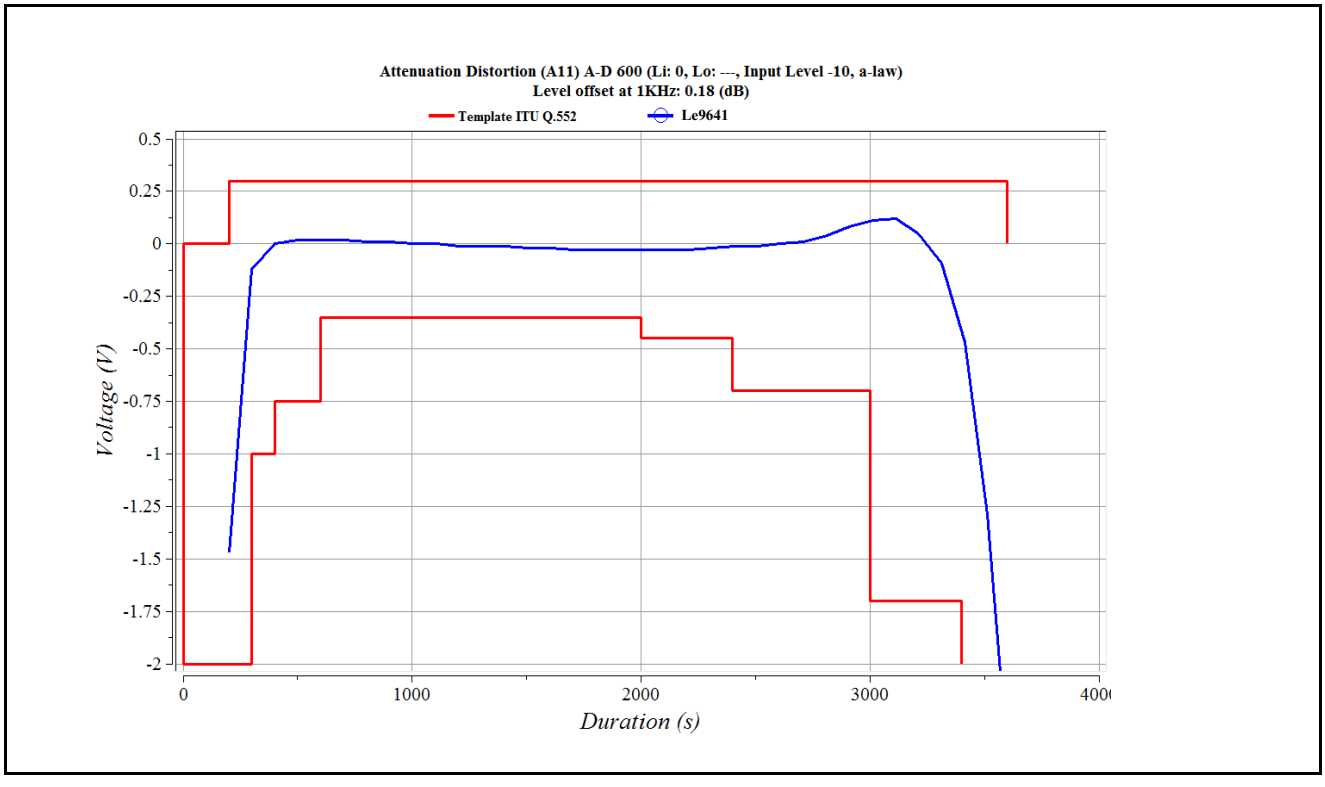


Figure 16 - Transmit Path (A to D) Attenuation Distortion (Narrowband)

6.2.3 Gain Tracking and Noise

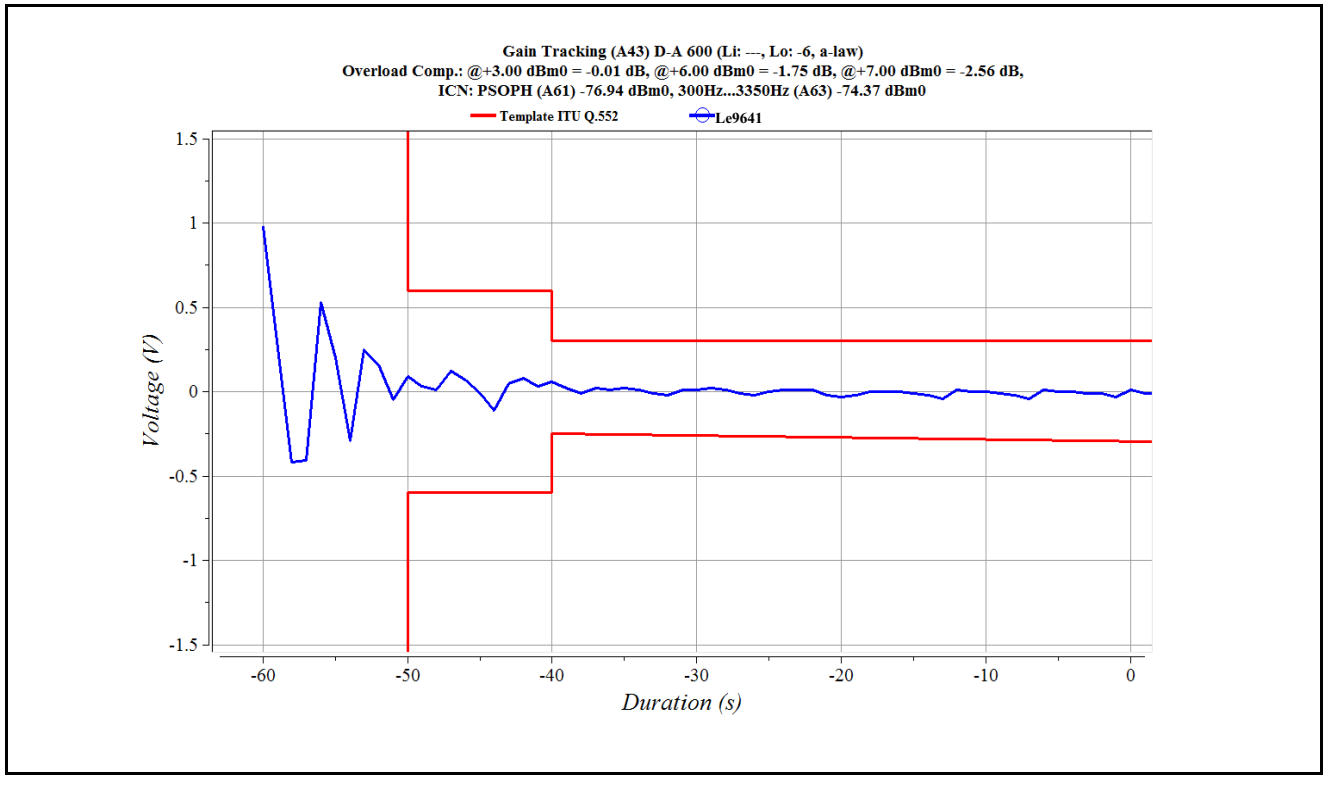


Figure 17 - Receive Path (D to A) Gain Tracking (Narrowband)

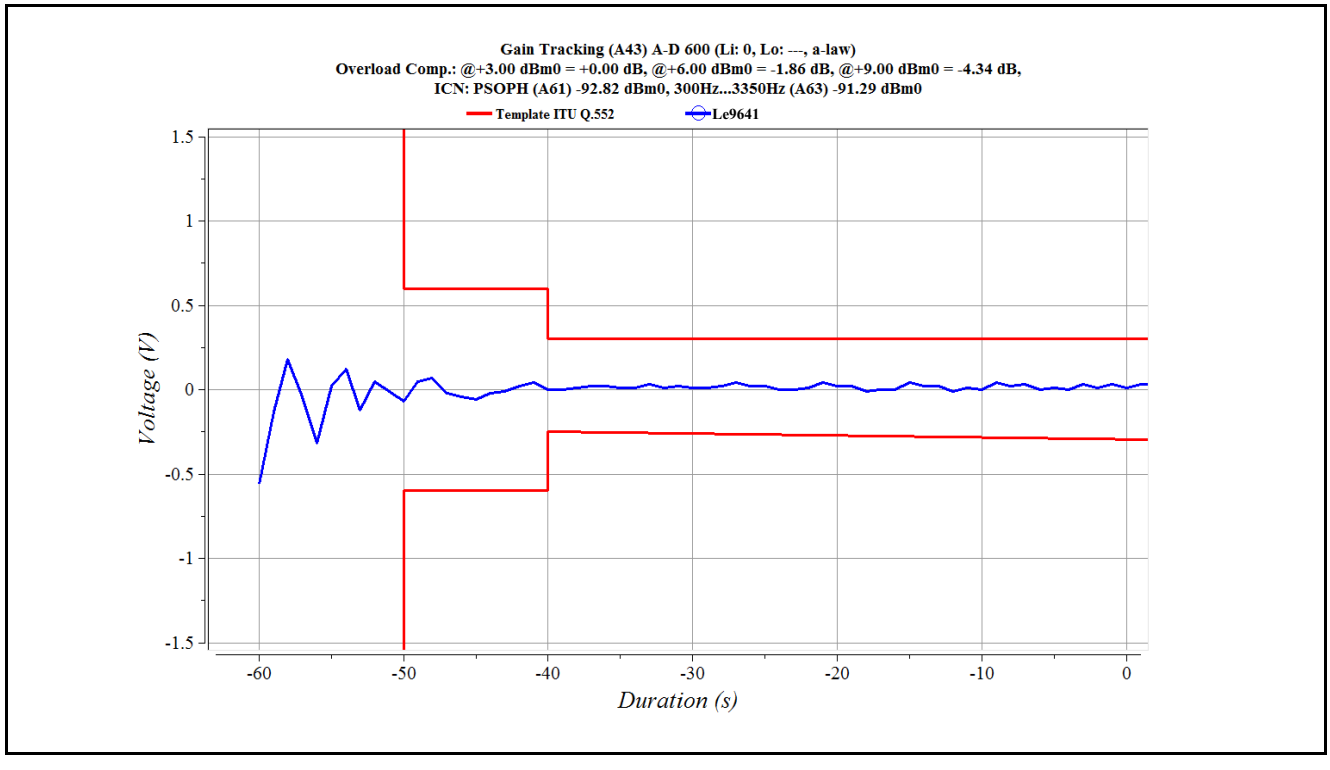


Figure 18 - Transmit Path (A to D) Gain Tracking (Narrowband)

6.2.4 Total Distortion and Harmonic Distortion

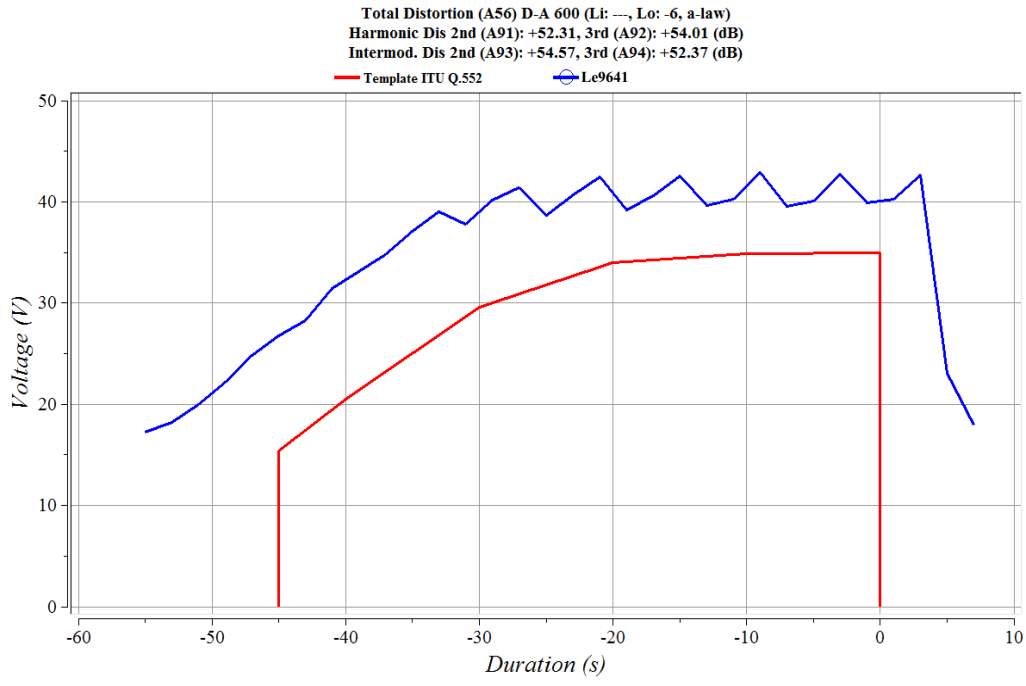


Figure 19 - Receive Path (D to A) Total Distortion (Narrowband)

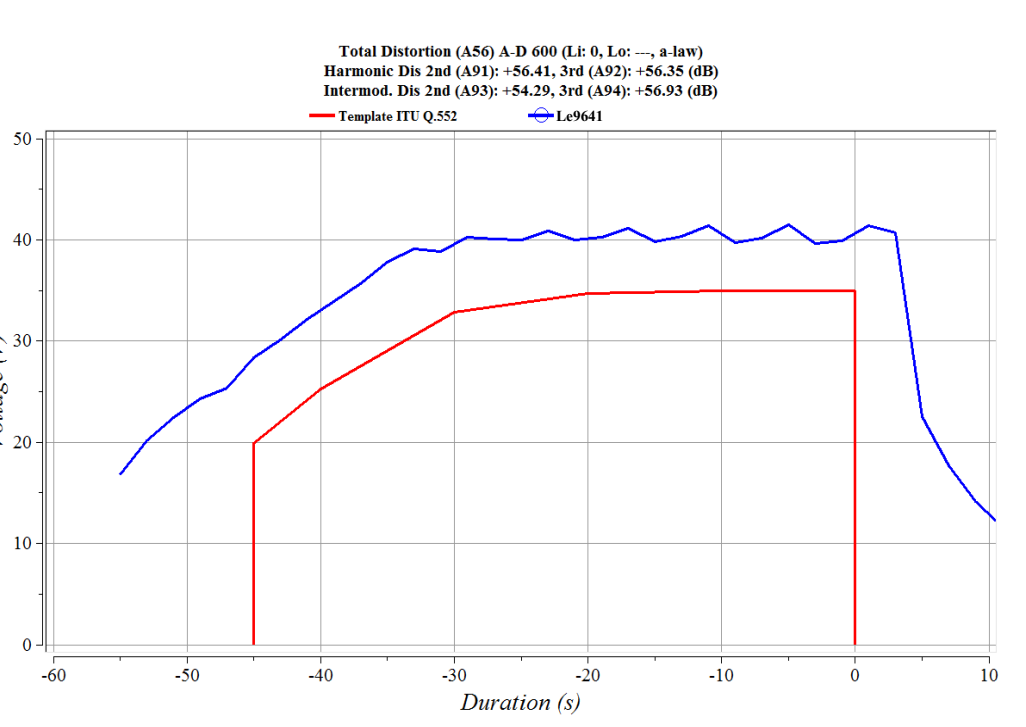


Figure 20 - Transmit Path (A to D) Total Distortion (Narrowband)

6.3 Wideband Transmission Performance

The following graphs illustrate the wideband (150 - 6800 Hz) transmission performance using a *W&G PCM-4*. Note that the *ZL88601/602* device supports per-channel wideband mode.

6.3.1 Return Loss

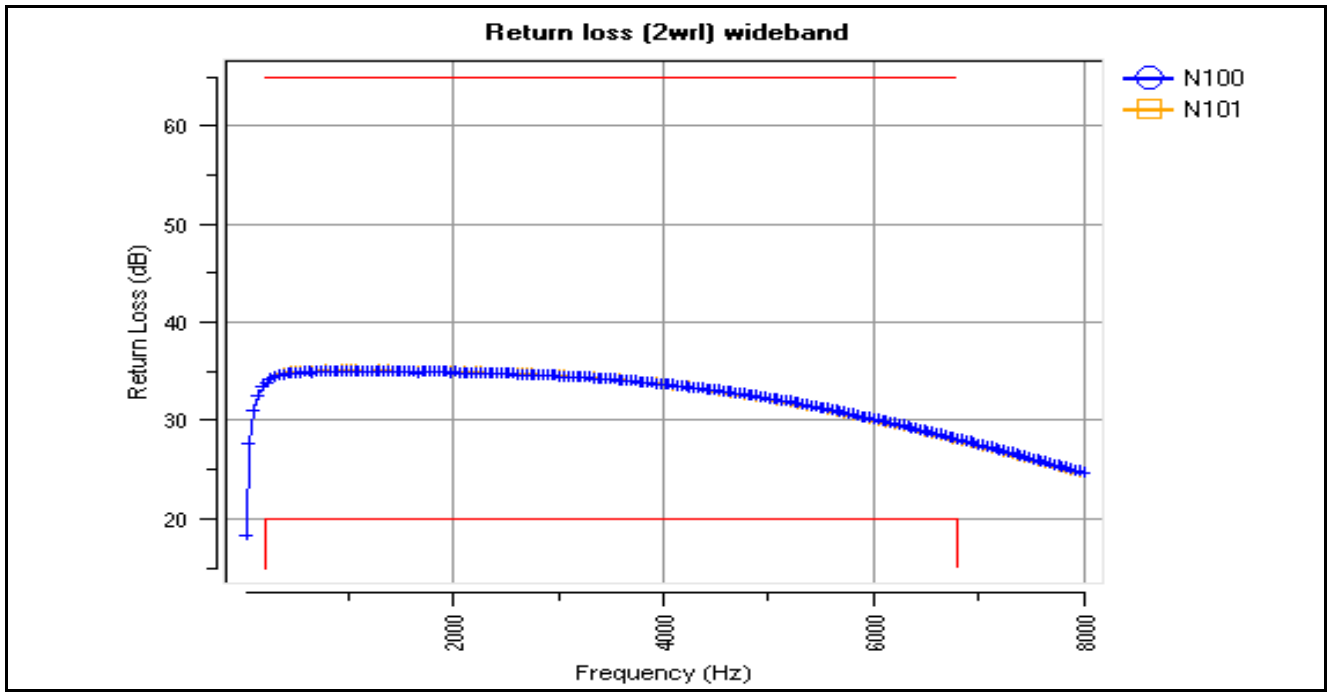


Figure 21 - Two-Wire Return Loss (Wideband)

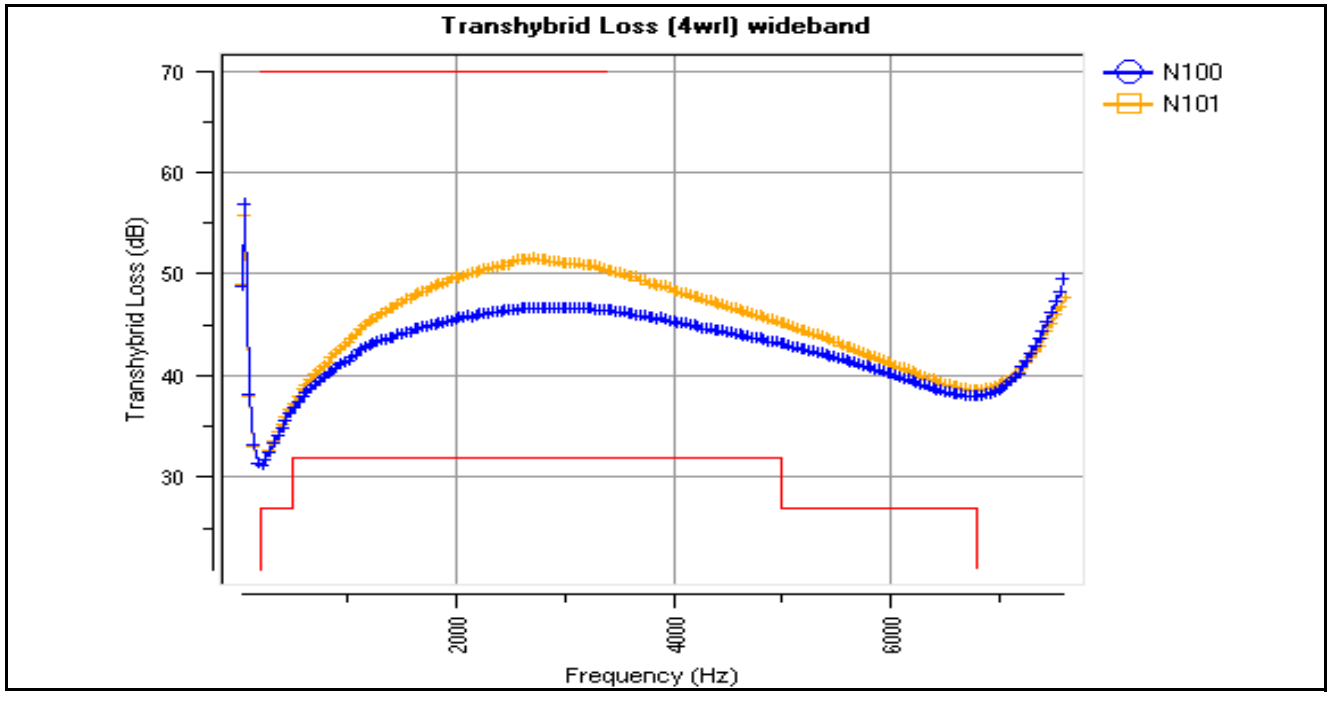


Figure 22 - Four-Wire Return Loss (Wideband)

6.3.2 Attenuation Distortion and Gain

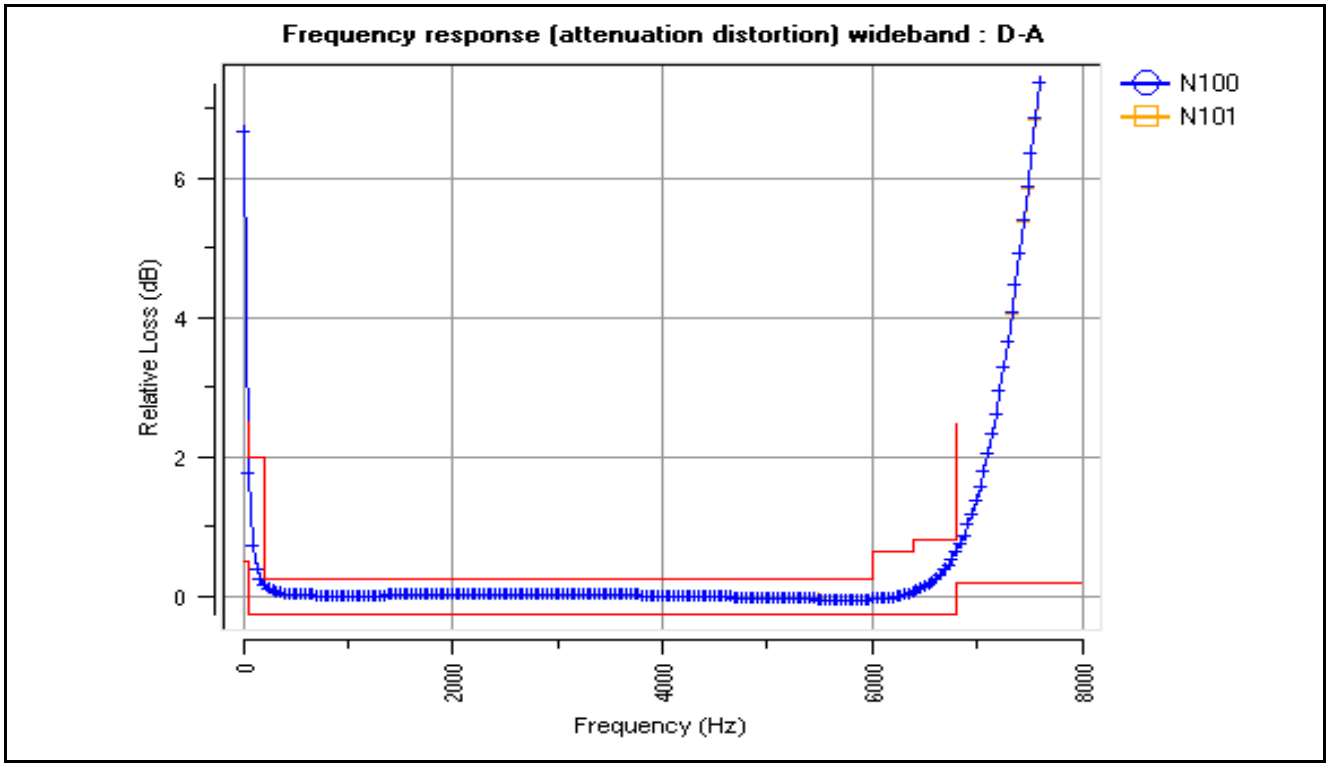


Figure 23 - Receive Path (D to A) Attenuation Distortion (Wideband)

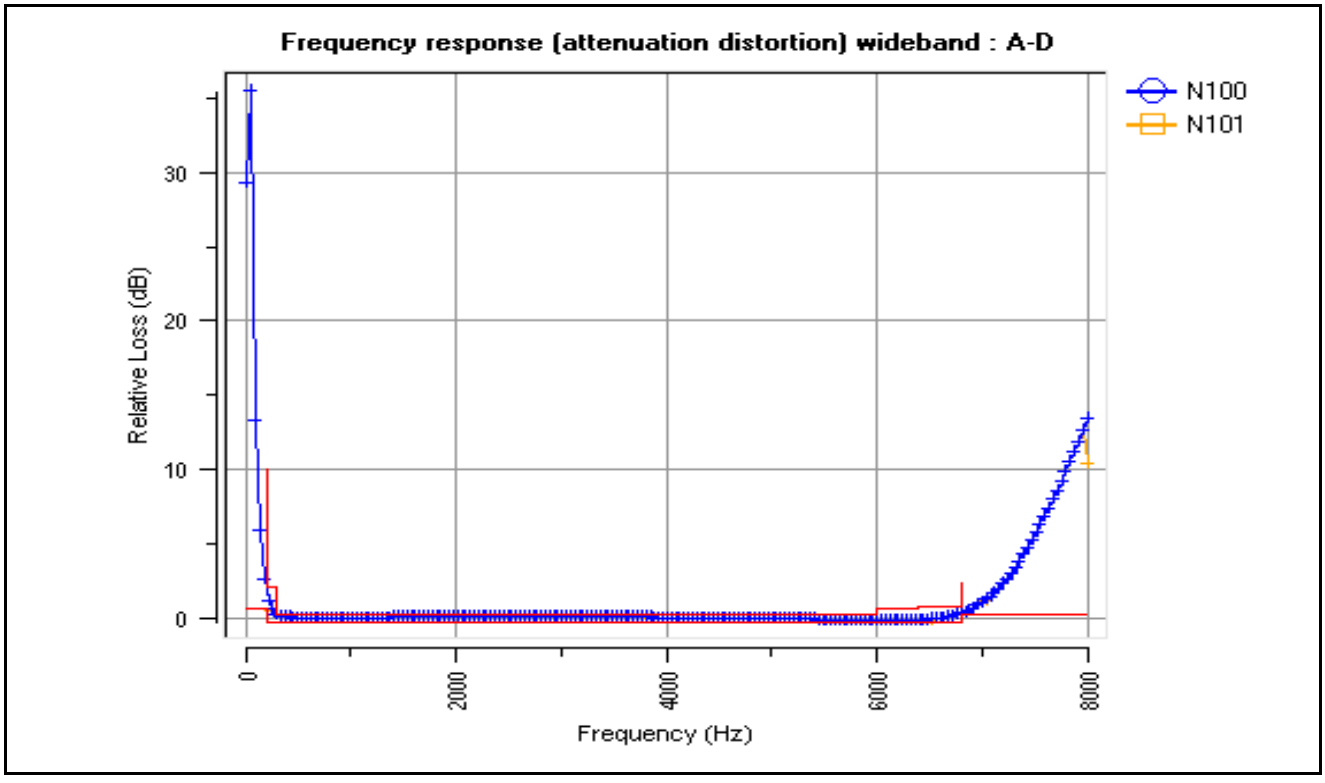


Figure 24 - Transmit Path (A to D) Attenuation Distortion (Wideband)

6.3.3 Gain Tracking and Noise

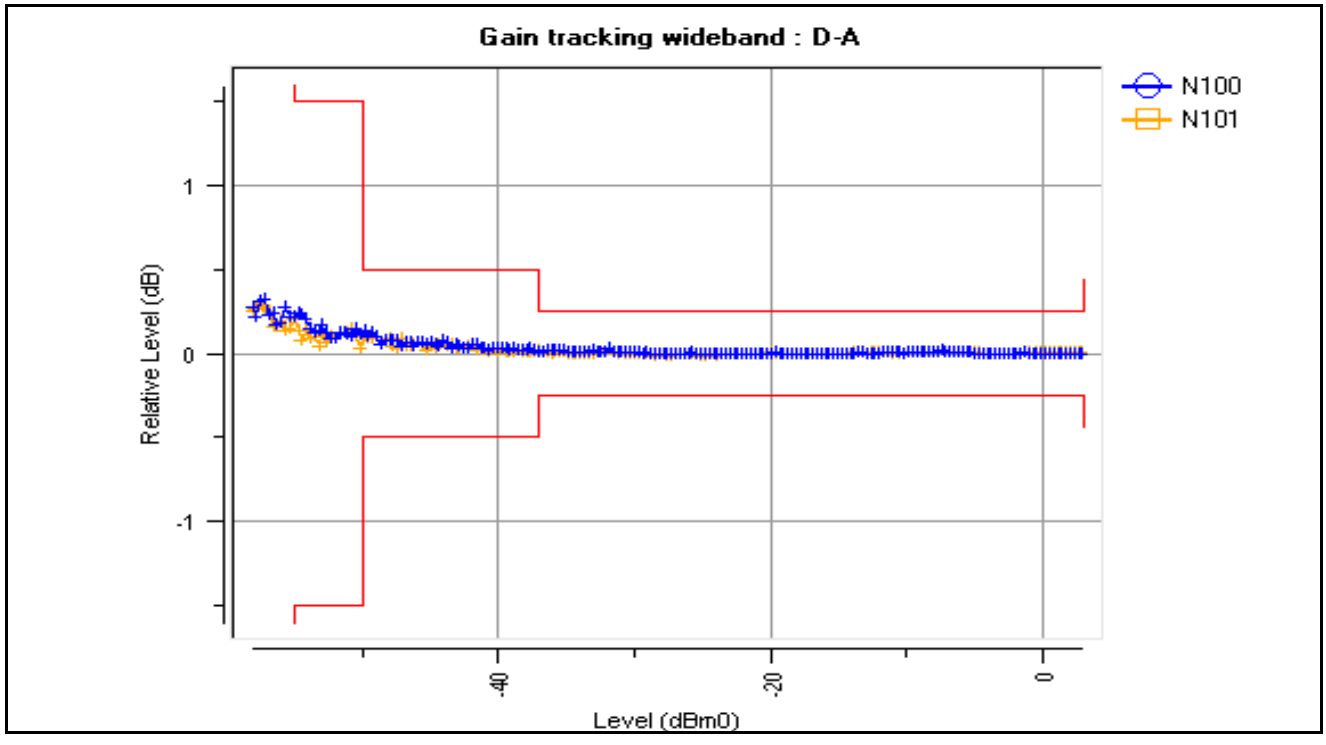


Figure 25 - Receive Path (D to A) Gain Tracking (Wideband)

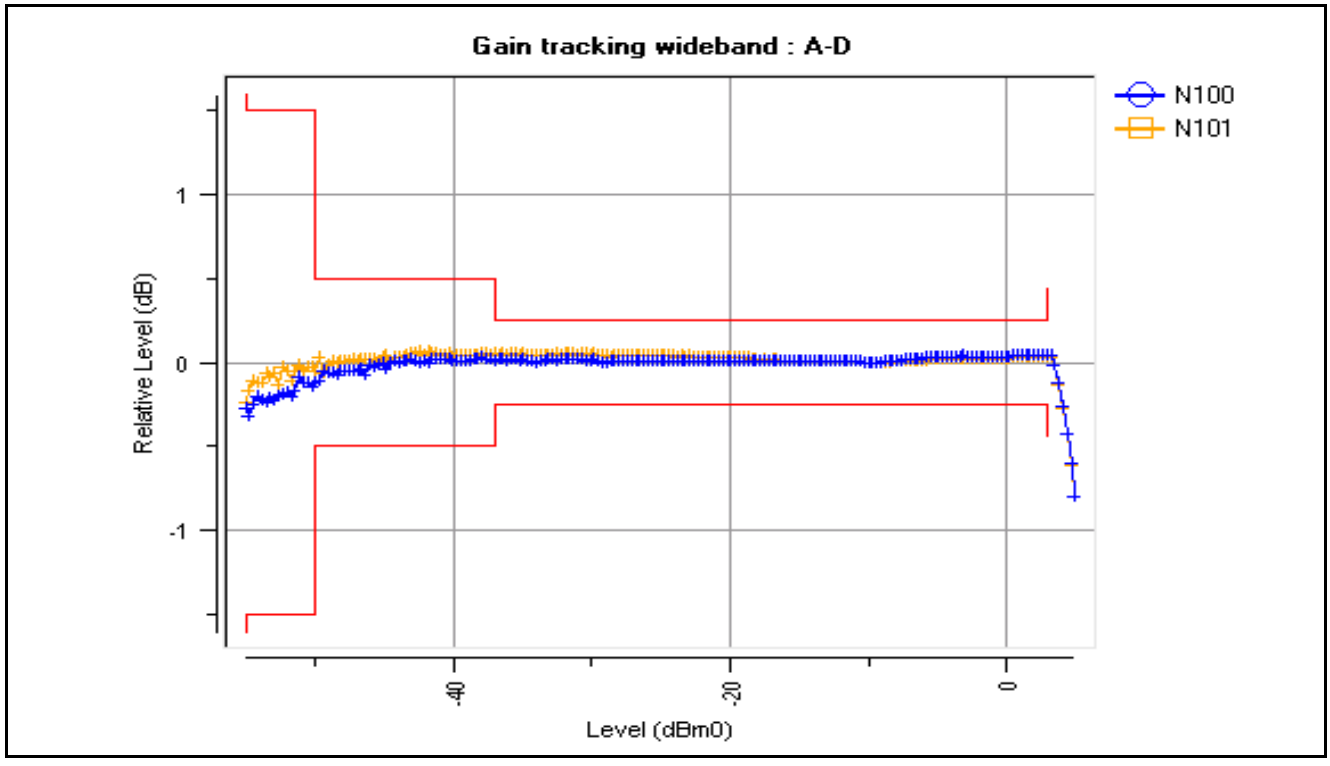


Figure 26 - Transmit Path (A to D) Gain Tracking (Wideband)

6.3.4 Total Distortion and Harmonic Distortion

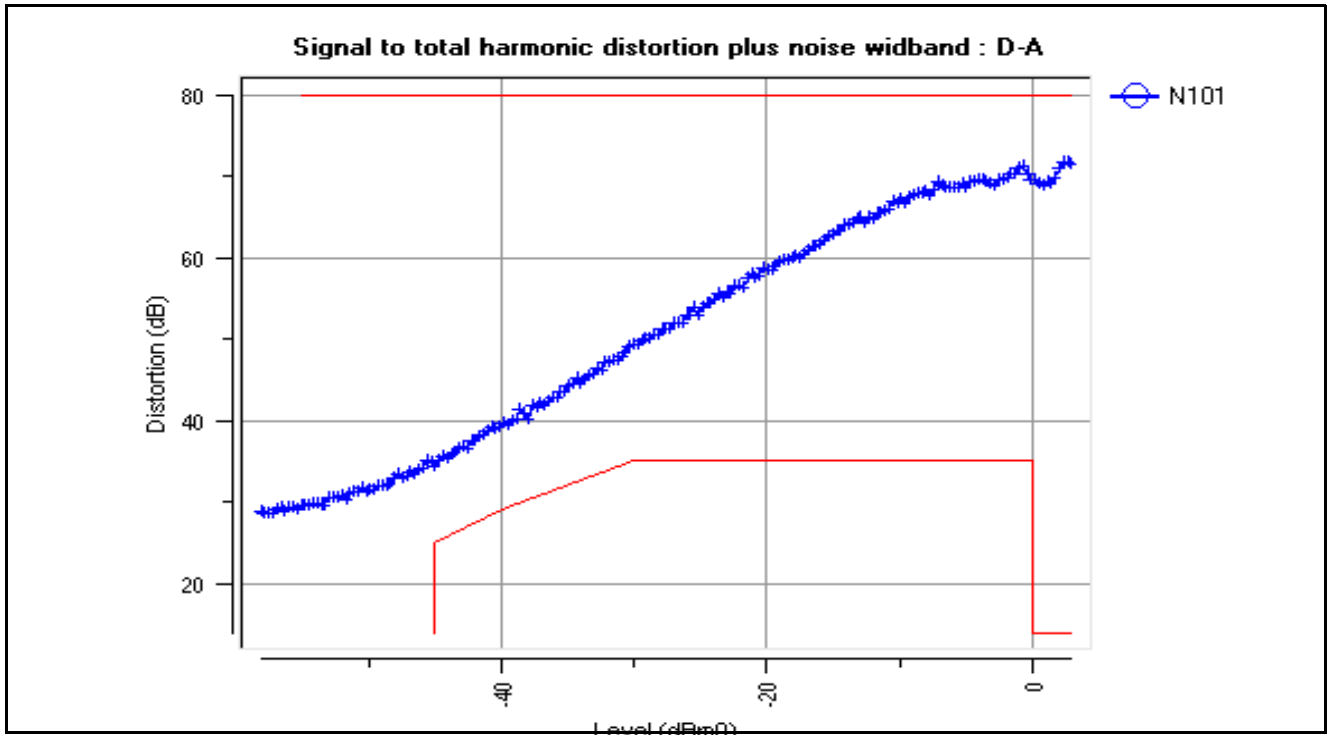


Figure 27 - Receive Path (D to A) Total Distortion (Wideband)

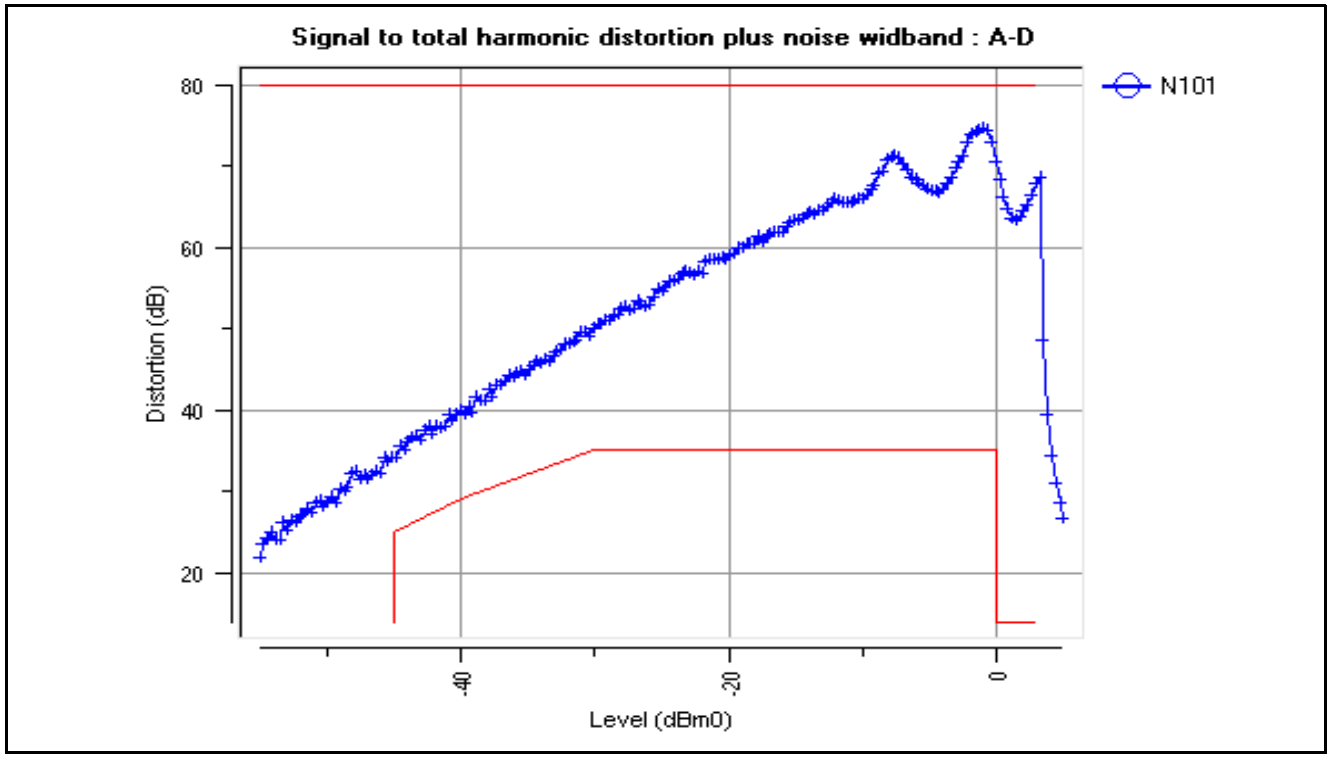


Figure 28 - Transmit Path (A to D) Total Distortion (Wideband)

6.4 Power Consumption with Buck-Boost supply

The following parameters are used to calculate DC feed and Ringing power consumption:

DC Feed Power Consumption

1. On- and off- hook states: (see *Le9641* data sheet conditions)
2. Off-Hook Load 300 Ω
3. V_{DD} = 3.3 V, V_{DSW} = 3.3 V, V_{SW} = 12.0 V.
4. V_{OC} = 48V, I_{LA} = 25 mA, V_{FLOOR}=-20 V
5. Fixed mode ringing C1 and C2, VBAT = -75 V,
6. Fixed mode ringing C3 and C4, VBAT = -90 V

Ringing Power Consumption

Ringing tests have two conditions: C1 and C2 with ILR = 54 mA and RTTH = 21 mA (AC only), C3 and C4 with ILR = 76 mA and RTTH = 30 mA (AC only).

1. C1 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load
2. C2 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 5 REN (1386 Ω + 40-µF) load
3. C3 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load
4. C4 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 5 REN (1386 Ω + 40-µF) load

Operational State	Condition	I_{DD} mA *(Note 1)*	I_{VSW} mA	System Power mW
		Typ	Typ	Typ
Shutdown	Disconnect, switcher off	1.7	0	8.5
Disconnect		5.9	1.1	33
Low Power Idle		10.8	1.6	55
Idle	On-Hook	15.1	6.1	123
Active (normal or reverse polarity)	On-Hook Transmission	25.5	17.6	295
	Off-Hook, 300 Ω	24.1	69.2	910
Ringing *(2)*	C1	26	205	1262
	C2	25.9	301	3697
	C3	25.9	273	3361
	C4	25.7	399	4872

Table 2 - Buck-Boost Power Consumption

Notes:

1. *I_{DD} supply current is the sum of I_{AVDD} , I_{DVDD} , and I_{VDSW} for the device*
2. *Ringing tests were cadenced to produce an average power that can be handled by the device.*
3. *Note that power efficiency is dependent on power supply components. Use of different components, particularly MOSFET, PNP and inductor, may result in different total system power.*

6.5 Power Consumption with Inverting Boost supply

The following parameters are used to calculate DC feed and Ringing power consumption:

DC Feed Power Consumption

1. On- and off- hook states: (see *Le9641* data sheet conditions)
2. Off-Hook Load 300 Ω
3. V_{DD} = 3.3 V, V_{DSW} = 5.0 V, V_{SW} = 12.0 V.
4. V_{OC} = 48V, I_{LA} = 25 mA, V_{FLOOR} = -15 V

Ringing Power Consumption

Ringing tests have two conditions: C1 and C2 with ILR = 54 mA and RTTH = 21 mA (AC only), C3 and C4 with ILR = 76 mA and RTTH = 30 mA (AC only).

1. C1 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load
2. C2 programmed ringing 70.7 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 5 REN (1386 Ω + 40-µF) load
3. C3 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load
4. C4 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 5 REN (1386 Ω + 40-µF) load

Operational State	Condition	I_{DD} mA *(Note 1)*	I_{VSW} mA	I_{VDSW}mA	System Power mW
		Typ	Typ	Typ	Typ
Shutdown	Disconnect, switcher off	1.7	0	0	6.4
Disconnect		6.4	0.08	0.16	23
Low Power Idle		9.8	1.2	0.26	48
Idle	On-Hook	13.4	4.2	0.26	96
Active (normal or reverse polarity)	On-Hook Transmission	18.3	13.1	1.24	225
	Off-Hook, 300 Ω	18.3	53.8	1.24	712
Ringing *(2)*	C1	21	135	1.28	1695
	C2	21.2	204	1.3	2525
	C3	21.3	196	1.30	2429
	C4	21.4	290	1.32	3557

Table 3 - Inverting Boost Power Consumption

Notes:

1. *I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the device*
2. *Ringing tests were cadenced to produce an average power that can be handled by the device.*
3. *Note that power efficiency is dependent on power supply components. Use of different components, particularly MOSFET, PNP and inductor, may result in different total system power.*

6.6 12V Buck-Boost Switching Regulator Performance

Input Range:	9 to 15 V_{DC}
Supply Efficiency:	The efficiency will vary with load and with input voltage. For a nominal 12 V_{DC} input, the efficiency range is typically 50% to 75%
Maximum Output	-95 V_{DC} (Limited by 100V capacitors)
Ringing Voltage	Up to 85 V_{PK}
Ringing Drive	5 REN maximum, subject to the device thermal dissipation not exceeding 1.5 W
Output Regulation:	1.0 % with 12 V_{DC} input and -90 V_{DC} output load varied from 0 to 30 mA
Output Accuracy:	-4 V_{DC} to +4 V_{DC} from the fixed ringing voltage setting
Operating Frequency:	Disconnect, Low Power Standby, and Standby (On-Hook Idle): 24 kHz On-Hook Transmission, Talk (Off-Hook), and Ringing: 128 kHz

6.7 12V Inverting Boost Switching Regulator Performance

Input Range:	9 to 15 V_{DC}
Supply Efficiency:	The efficiency will vary with load and with input voltage. For a nominal 12 V_{DC} input, the efficiency range is typically 50% to 80%
Maximum Output	-90 V_{DC} (Limited by 100V MOSFET)
Ringing Voltage	Up to 85 V_{PK}
Ringing Drive	5 REN maximum, subject to the device thermal dissipation not exceeding 1.5 W
Output Regulation:	1.0 % with 12 V_{DC} input and -90 V_{DC} output load varied from 0 to 30 mA
Output Accuracy:	-4 V_{DC} to +4 V_{DC} from the fixed ringing voltage setting
Operating Frequency:	Disconnect, Low Power Standby, and Standby (On-Hook Idle): 24 kHz On-Hook Transmission, Talk (Off-Hook), and Ringing: 512 kHz

6.8 Thermal Performance

The *Le9641* device has a thermal ePAD which must be soldered to a large copper area for heat dissipation and tied to the ground plane. For best thermal performance, a four layer PCB is recommended. Even with multi-layer boards it is recommended that multiple copper pours be used for thermal relief. Microsemi voice telephony modules pour ground on both inner layers and bring the ePAD to the bottom of the PCB. All layers should be connected with a generous array of vias that have solid connections to the ground pours.

The *Le9641* has a recommended maximum operating junction temperature of 145°C. The device will indicate a thermal fault at a junction temperature of 165°C. Depending on the setting of the VP_DEVICE_OPTION_ID_CRITICAL_FLT function in the *VP-API-II*, the device may either go to the Disconnect state or temporarily shut down the tip and ring drivers and turn them back on when the die temp is reduced. Note that the device will alternately cycle in and out of the temporary shutdown condition if a high power dissipation condition is present.

Le9641 θ_{JA}= 29°C/W - using a 4-layer PCB with ground pours on both inner layers. Via array is a 7x7 array of 0.33 mm/13 mil vias.

Le9641 θ_{JA}= 35°C/W - using a 2-layer PCB with ground pours on both inner layers. Via array is a 7x7 array of 0.33 mm/13 mil vias.

Actual device thermal performance is dependent on factors such as copper area, ePAD solder coverage, proximity of other heat producing devices, airflow, etc. Refer to Chapter 7 for PCB layout references and to the *Le9641 Single Channel Device Data Sheet* for footprint recommendations.

7.0 Printed Circuit Board Documentation

7.1 Revision Information

ZLR964124L Revision A0: Initial Release

ZLR964124L Revision A1: Change to IB supply and notes

ZLR964124L Revision A2: Correct ZSI pull up/down options

7.2 Parts Placement Strategy

The *ZLR94124 Line Module* is designed using a two layer PCB to demonstrate a low cost and compact design. The design features two *Le9641 Single Channel miSLIC™ Devices*, *Telcordia*-compliant intra-building protection, and Buck-Boost and Inverting Boost tracking power supplies. The switcher is optimized for +12 V input. PCB thermal pads for the Microsemi *Le9641* are required for grounding and heat dissipation. This module measures 3.95" x 2.0" (10 x 5.1 cm). This board is designed to be plugged into the *SM2* expansion receptacle on the Microsemi *ZTAP (Le71HP0400)* platform.

The switching power supply tends to be the most common place for design and layout mistakes. For best performance, all sense input nets should be kept as short as possible with their associated components placed close to the *Le9641* device. These include the following: TDC_x, RDC_x, TAC_x, RAC_x, RSN, SWISY, and SWVSZ. Also, the VREF net should be routed as directly as possible between the CHL_1 capacitors, and $CREF_1$ should be placed near the VREF pin. Avoid routing the VREF net near any digital signals. It is also recommended that $CREF_1$, and CHL_1 be ceramic capacitors with X5R/X7R dielectric. If a design is expected to operate above 70°C then X7R capacitors are recommended. Use of Y5V and Z5U type capacitors is not recommended. There are no Y5V or Z5U type capacitors used in this design.

Switcher feedback components RVS_1, $RCMP_1$ and $CCMP_1$ should be placed as close to pins SWCMPY and SWVSY as possible. The SWVSY node is a summing node for the error amplifier and should be treated as such. Avoid routing any digital signals or other sources of noise near this node. Noise on SWCMPY can upset the operation and efficiency of the switching power supply. $CCMP_x$ should also be high quality capacitors with stable characteristics. NPO/C0G dielectric is preferable especially if the design will experience wide temperature extremes. X7R types are acceptable for most applications. The SWISY current sense node is also very sensitive to noise. Avoid routing the net parallel to SWOUTY, the switching transistor driver signal, or near the drain node of the power MOSFET or collector nose of the PNP. SWISY should tap right off of the current sense resistor, $RLIM_x$, and route directly to the current sense filter components CCS_1, RCS_1, and RTH_1 which should be placed near the pin SWISY. It is also recommended to shield SWISY with ground if possible. The threshold for SWISY is only 100 mV which makes it very sensitive to noise. Poor routing of SWISY is one of the most common mistakes. A noisy SWISY signal WILL cause the supply to run poorly. The current limit sense resistor, $RLIM_1$, should terminate to ground with multiple vias and minimal trace length from the resistor to ground.

High current nets should be kept short and routed with 50 mil/1.25 mm nets minimum. The 12 V net should also be routed with heavy copper to minimize losses. When the power transistor switches on, the current is sourced primarily from CSW_1. In the case of the Inverting Boost, the loop from CSW_1 through the inductor, MOSFET, and RLIM to ground should be as tight as possible. For Buck-Boost the positions of the transistor and inductor are reversed relative to Inverting Boost. The ground return from RLIM to CSW should be as short as possible.

Following the recommendations above will help achieve best performance and also best EMI/EMC performance. Additional recommendations for EMI/EMC performance are proper supply decoupling/filtering and good digital design techniques. DVDD pins should have 0.01 uF decoupling caps and AVDD pins should have 0.1 µF decoupling caps for each supply pin of the device. An additional bulk decoupling cap such as a 4.7 µF ceramic or tantalum near the device is also recommended. There is also a filter between DVDD and AVDD that is required. A 2ohm resistor is placed between DVDD and AVDD and a 1uF ceramic cap is connected from AVDD to ground. The value of the resistor should not be increased or AVDD may have too much voltage drop.

One common source of EMI is exceedingly fast edge rates on digital signals. Modern CMOS processes result in digital edge rates that have no problem achieving 1 ns rise/fall times. This results in spectral components that are well into the GHz range. This is completely unnecessary for proper *miSLIC* device operation. Even with careful design and layout, significant overshoots on clock edges are present that can result in noise in the device and even EMI failure due to this noise creeping out the tip and ring pair. In many cases, placing a 100 Ω series termination resistor at the source will slow the edges down to 5 ns, which is still well within the rise time requirements of *miSLIC* devices. What this achieves is that the rise/fall time is slow enough that transmission line effects are no longer a factor in many cases. This has been shown to result in very nice square clocks with little or no overshoot. As long as the rise time is 10 ns or less, it will work.

For best thermal performance of the QFN-48 package, the *Le9641* thermal pad must be soldered to a thermal PCB pad under the device. If the board is a two-layer design, the thermal pad should also be on the back side of the PCB with an array of vias connecting both sides. The more copper the better. If the design incorporates a ground plane, the thermal pad should tie into the ground plane with a 7x7 array of 13 mil/0.33 mm vias on a 5.4x5.4 mm area. The vias should be hard tied into the ground plane. Thermal (wagon wheel) vias should not be used. The thermal pad should still be brought to the back side of the PCB. Note that ALL ground connections for this device are through the ePAD, therefore the ePAD MUST be grounded for both electrical and thermal reasons.

For two layer designs, all components should be placed on the top side of the PCB with minimal routing on the back side. The intent is to maintain as much ground pour as possible. Digital signals such as the SPI/PCM bus should be interleaved with ground traces that have vias to the back side copper.

7.3 ZLR964124L Line Module Schematics

The schematics of the *ZLR964124 Line Module* are provided below in Figure 29, *ZLR964124L Line Module Schematic*, on page 42. Please refer to the *ZLR964124L Bill of Materials*, on page 48 for more details about component selections.

The module schematic is available in *Cadence OrCAD (Allegro Design Entry CIS)* format upon request.

Figure 29 - ZLR964124L Line Module Schematic

REV	DESCRIPTION	DATE
A0	INITIAL RELEASE	8/8/14
A1	Change to IB supply and notes	1/14/15
A2	ZSI pullup/down corrections	1/29/15

ZLR964124L 2 FXS miSLIC™ Reference Design

Le9641 QFN48 1 FXS Buck-Boost with PCM/MPI Interaface

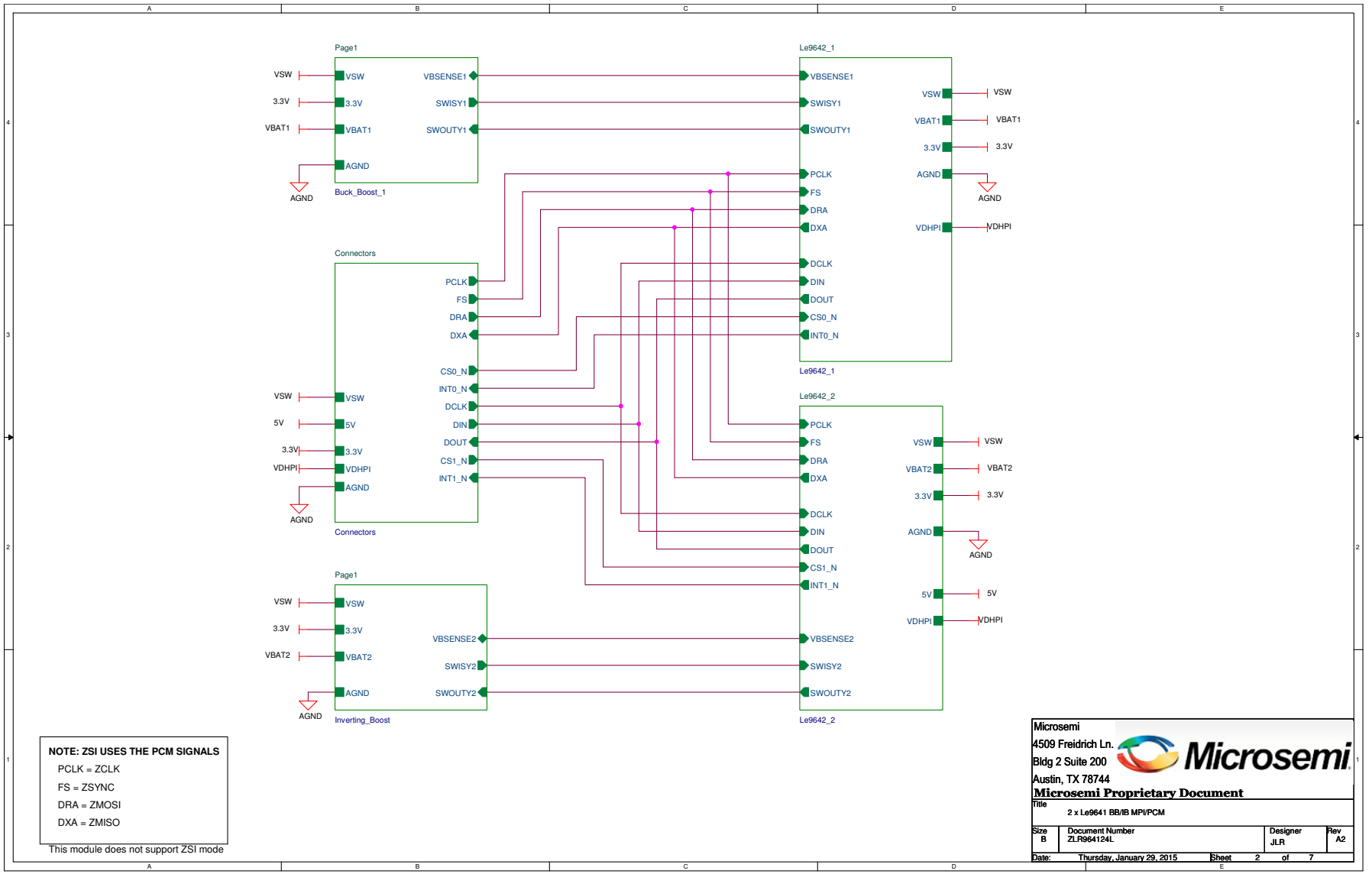
Le9641 QFN48 1 FXS Inverting Boost with PCM/MPI Interaface

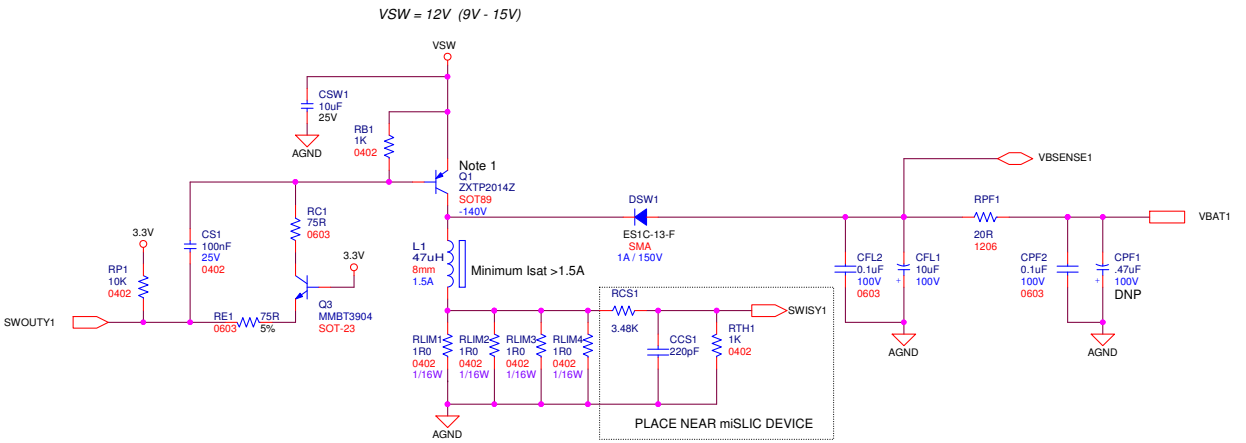
Description:
This reference design provides a 2FXS solution.

Page1 - Title Page
Page2 - Hierarchy
Page3 - Buck-Boost Supply - Ch1
Page4 - Inverting Boost Supply - Ch2
Page5 - Connectors
Page6 - Ch1 Le9641 QFN48
Page7 - Ch2 Le9641 QFN48

Microsemi
4509 Freidrich Ln.
Bldg 2 Suite 200
Austin, TX 78744

Title: 2 x Le9641 BB/IB MPI/PCM			
Size: B	Document Number: ZLR964124L	Designer: JLR	Rev: A2
Date: Thursday, January 29, 2015	Sheet 1 of 7		





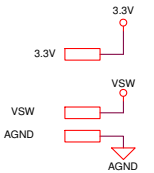
Buck-Boost Supply

Q1 PNP Requirement	
Ringing 50Vrms	Diodes Inc. ZXTP2013/ZX5T953/FZT953 (Vce=100V)
Ringing 60Vrms	Diodes Inc. ZXTP2014/ZX5T955/FZT955 (Vce=140V)

SOT223 (G) or SOT89 (Z) packages acceptable

NOTES:

1) Q1 should have a collector thermal pad of at least .5cm x .5cm



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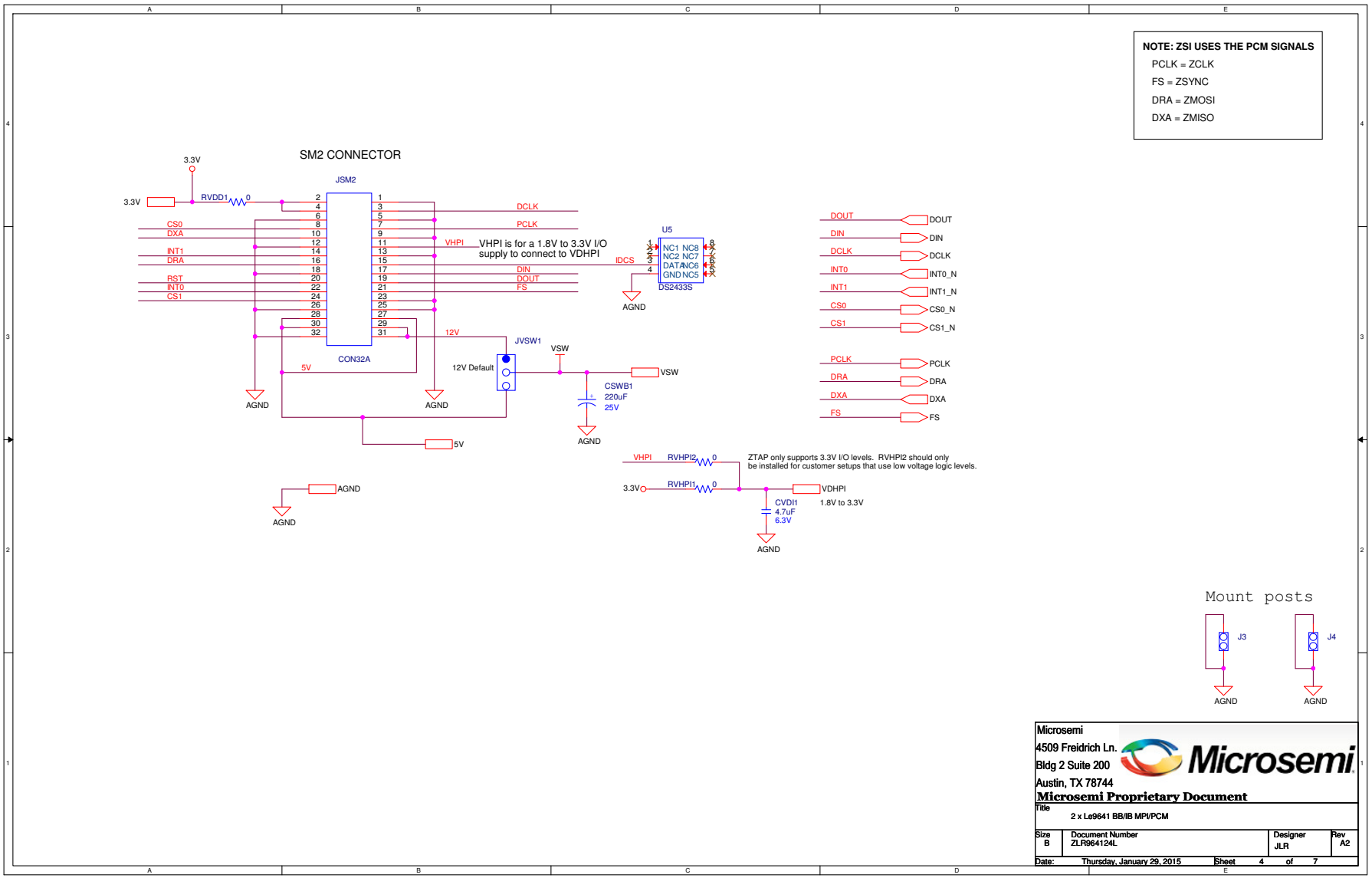
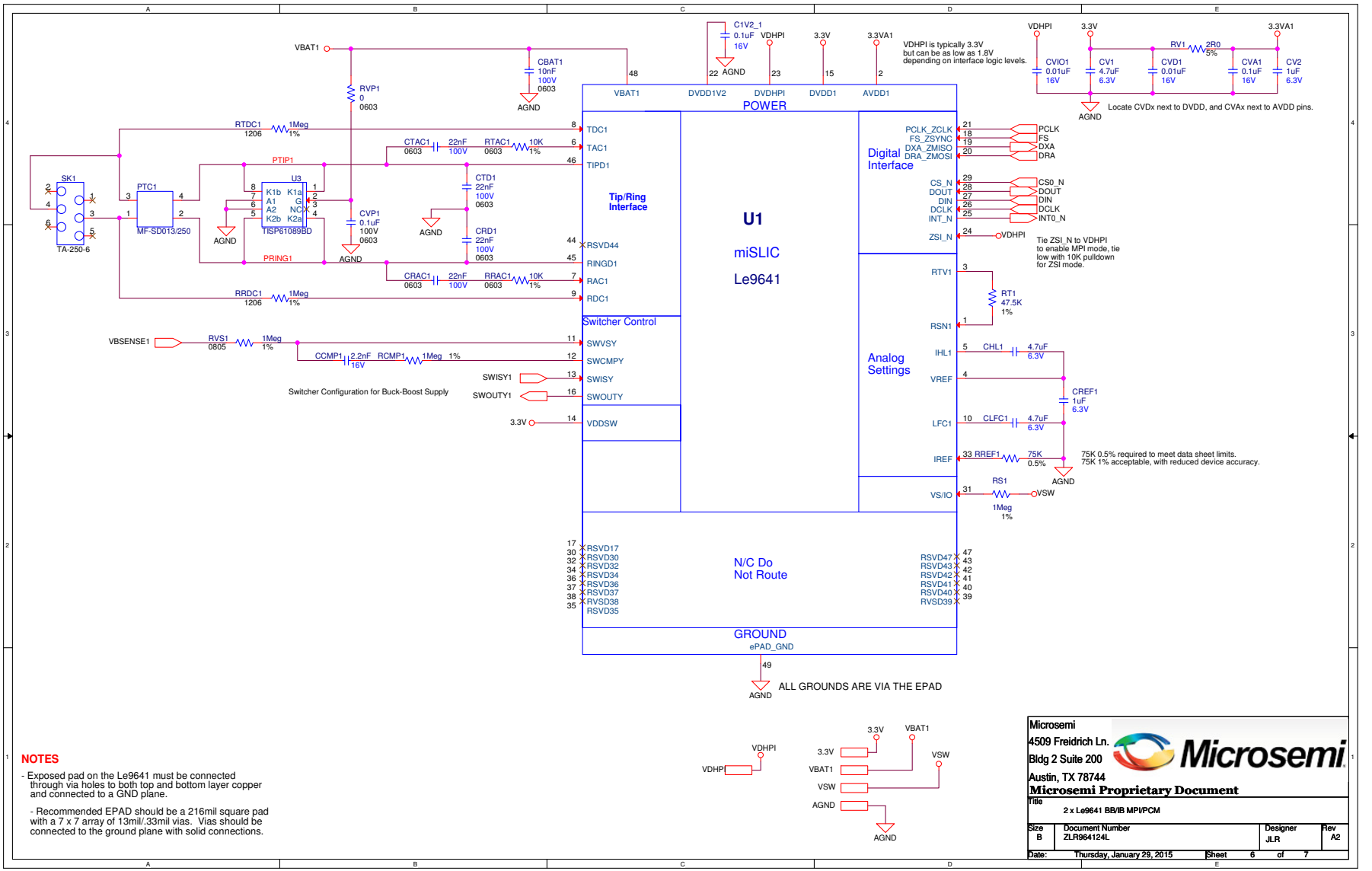
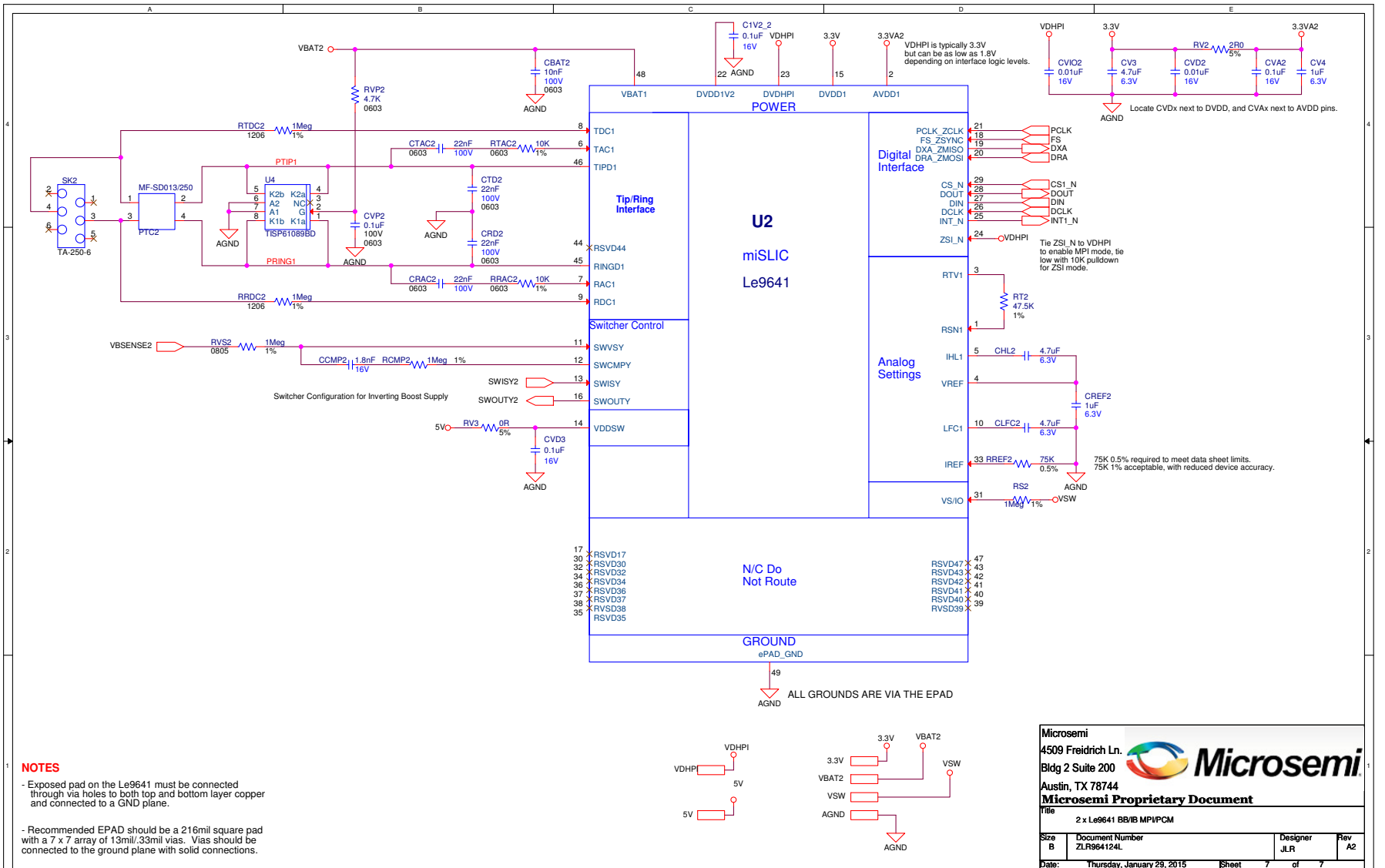
Title: 2 x Le9641 BB/IB MPI/PCM			
Size: B	Document Number: ZLR964124L	Designer: JLR	Rev: A2
Date: Thursday, January 29, 2015	Sheet 3 of 7		






U2
miSLIC
Le9641
POWER
Tip/Ring Interface
Digital Interface
Analog Settings
Switcher Control
GROUND
ePAD_GND
N/C Do Not Route
Switcher Configuration for Inverting Boost Supply
ALL GROUNDS ARE VIA THE EPAD
Locate CVDx next to DVDD, and CVAx next to AVDD pins.
VDHPI is typically 3.3V but can be as low as 1.8V depending on interface logic levels.
Tie ZSI_N to VDHPI to enable MPI mode, tie low with 10K pulldown for ZSI mode.
75K 0.5% required to meet data sheet limits.
75K 1% acceptable, with reduced device accuracy.
NOTES
- Exposed pad on the Le9641 must be connected through via holes to both top and bottom layer copper and connected to a GND plane.
- Recommended EPAD should be a 216mil square pad with a 7 x 7 array of 13mil/.33mil vias. Vias should be connected to the ground plane with solid connections.
Microsemi
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Microsemi Proprietary Document
Title
2 x Le9641 BB/IB MPI/PCM
Size B
Document Number ZLR964124L
Designer JLR
Rev A2
Date: Thursday, January 29, 2015
Sheet 7 of 7

7.4 ZLR964124L Bill of Materials

Item #	Quantity	Part Reference	Value	voltage	rating	tolerance	PCB Footprint	manuf	manuf #	distributor	distributor #	note
1	8	CTD1 CRD1 CRAC1 CTAC1 CTD2 CRD2 CRAC2 CTAC2	0.022uF	100V	X7R	10%	CAP0603					
2	7	CHL1 CHL2 CV1 CV3 CLFC1 CLFC2 CVDI1	4.7uF	6.3V	X5R	20%	CAP0603					
3	4	CREF1 CREF2 CV2 CV4	1uF	10V	X5R	10%	CAP0603					
4	2	CVD1 CVD2 CVIO1 CVIO2	0.01uF	16V	X7R	10%	CAP0402					
5	1	CSWB1	220uF	25V	Elect	20%	CAPTH8	United Chemi-con	EKZE250ELL221MHB5D	Digikey	565-1674-ND	DNP
								Panasonic	EEU-FM1E221	Digikey	P12383-ND	
6	5	CVA1 CVA2 C1V2_1 C1V2_2 CVD3	0.1uF	16V	X7R	10%	CAP0402					
7	2	CVP1 CVP2	0.1uF	100V	X7R	10%	CAP0603					
8	2	CBAT1 CBAT2	.01uF	100V	X7R	105	CAP0603					
9	1	JVSW1	Header, 3 x 1					Samtec	TSW-103-07-L-S			
10	1	JVSW1-shunt	Shunt									
11	2	J3 J4	HDR2x1				HDR2x1	Samtec	TSW-102-07-T-S			
12	1	JSM2	Header, 2 x 16					Samtec	TSW-116-07-T-D			
13	1	PTC1 PTC2	PTC	250V	5R	3A	PTC_BOURNS_SN	Bourns	MF-SD013/250			
14	4	RRAC1 RTAC1 RRAC2 RTAC2	10K		1/10W	1%	RES0603					
16	4	RRDC1 RTDC1 RRDC2 RTDC2	1Meg	200V	1/4W	1%	RES1206					
17	2	RREF1 RREF2	75K		1/16W	0.5%	RES0402					
21	2	RT1 RT2	47.5K		1/16W	1%	RES0402					
22	1	RVDD1	0				RES1206					
23	2	RV1 RV2	2R0		1/16W	5%	RES0402					
24	2	RVHPI1 RVP1	0		1/10W		RES0603					
24a	0	RVHPI2	DNP									DNP
25	1	RVP2	4.7K		1/10W	5%	RES0603					
26	1	RV3	0R		1/16W		RES0402					
27	2	RS1 RS2	1Meg		1/16W	1%	RES0402					
28	2	SK1 SK2	RJ11_6x6x1				RJ11_6x6x1	TE Connectivity	5520250-3			
29	1	U1 U2	Le9641				QFN48	Microsemi	Le9641PQC			
30	1	U5	IC, EEPROM, 4KBITS	DS2433S+			SOIC-8W	Maxim	DS2433S+			
31	2	U3 U4	TISP61089BD				SOIC8	Bourns	TISP61089BD			
Buck-Boost Supply												
40	1	CFL1	10uF	100V	Elect	20%	CAPTH5	Panasonic	ECA2AM100			
								Nichicon	UVR2A100MED			
41	0	CPF1	1uF	100V	Elect	20%	CAPTH5	Panasonic	ECA2AM010			DNP
								Nichicon	UVR2A010MDD			
42	1	CCS1	220pF	16V	X7R	10%	CAP0402					
43	1	CCMP1	2.2nF	16V	X7R	10%	CAP0402					
44	1	CS1	0.1uF	**25V**	X5R	10%	CAP0402					
45	2	CFL2 CPF2	0.1uF	100V	X7R	10%	CAP0603					
46	1	CSW1	10uF	25V	X5R	20%	CAP1206					
47	1	DSW1	Ultra-fast Rectifier	150V	1A		SMA	Diodes	ES1C-13-F			
48	1	L1	47uH		1.5A		8mm	Taiyo Yuden	NR8040T470M			
								Bourns	SRN8040-470M			
49	1	RPF1	20R		1/4W	5%	RES1206					
50	1	RVS1	1Meg		1/8W	1%	RES0805					
51	1	RB1	1K		1/16W	5%	RES0402					
52	1	RCMP1	1Meg		1/16W	1%	RES0402					
53	1	RCS1	3.48K		1/16W	1%	RES0402					
54	1	RP1	10K		1/16W	5%	RES0402					
55	2	RE1 RC1	75R		1/10W	5%	RES0603					
56	1	RTH1	1K		1/16W	1%	RES0402					
60	0	Q1	PNP, 140V, Lo Vce	140V			SOT23	Diodes	ZXTP23140BF			DNP
61	1	Q1	PNP, 140V, Lo Vce	140V			SOT89	Diodes	ZXTP2014Z			
								Diodes	ZX5T955Z			
62	1	Q3	NPN, MMBT3904				SOT23	Diodes	MMBT3904-7-F			
								On Semi	MMBT3904LT1G			
Inverting-Boost Supply												
63	1	CCMP2	1.8nF	16V	X7R	10%	CAP0402					
64	1	CCS2	220pF	16V	X7R	10%	CAP0402					
65	1	CFL4 CPF4	0.47uF	100V	X5R	10%	CAP1206					
66	2	CBH1 CBH2	0.1uF	100V	X7R	10%	CAP0603					
67	1	CSW2	4.7uF	25V	X5R	20%	CAP0805					
68	1	DSW2	Ultra-fast Rectifier	150V	1A		SMA	Diodes	ES1C-13-F			
69	1	DSW3	Dual Diode, BAV23C	200V			SOT23	Diodes	BAV23C-7-F			
70	1	L2	4.7uH		3A		6mm	Taiyo Yuden	NR6045T4R5M			
								Bourns	SRN6045-4R7Y			
71	1	RG1	10R			5%	RES0402					
72	1	RG2	10K			5%	RES0402					
73	5	RLM1 RLM2 RLM3 RLM4 RLM5	1R0		1/16W	5%	RES0402					
74	0	RLIM5	0.05R		1/10W	2%	RES0603					DNP
75	1	RCMP2	1Meg		1/16W	1%	RES0402					
76	1	RCS2	4.99K		1/16W	1%	RES0402					
77	2	RDS1 RDS2	2R0		1/10W	5%	RES0603					
78	1	RTH2	1K		1/16W	1%	RES0402					
79	1	RVS2	1Meg		1/8W	1%	RES0805					
80	1	RPF3	20R		1/4W	5%	RES1206					
80	1	X1	MOSFET	100V			SOT23	Diodes	**DMN220H10LE**			
								IR	IRLML0100			
								Vishay	Si2392DS			
								Analog Power	AM2370N			
81	0	X2	MOSFET	100V			SOT6	Vishay	Si1480DH			DNP
								Analog Power	AM3470N			

7.5 ZLR964124L Layout Plots

Plots of the layout of the *ZLR964124L Line Module* are provided in this section. This layout is available in *Cadence Allegro* ***.brd*** (V16.5) format upon request. The gerber files are also available.

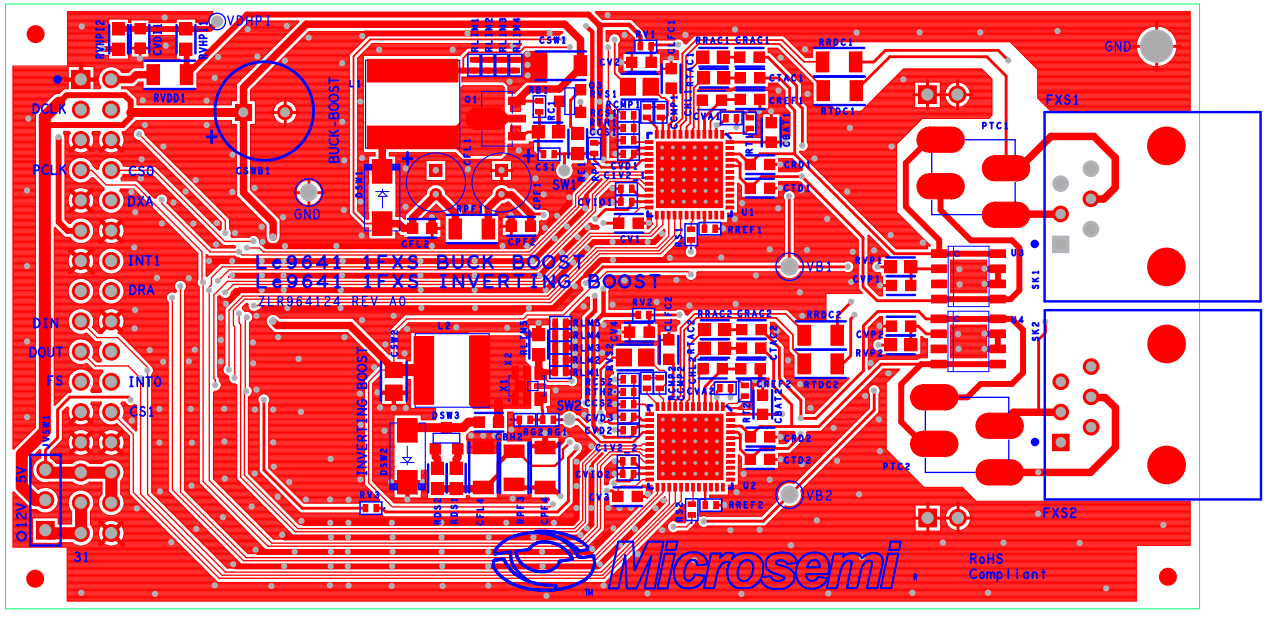

Figure 30 - Top Etch and Silk Screen

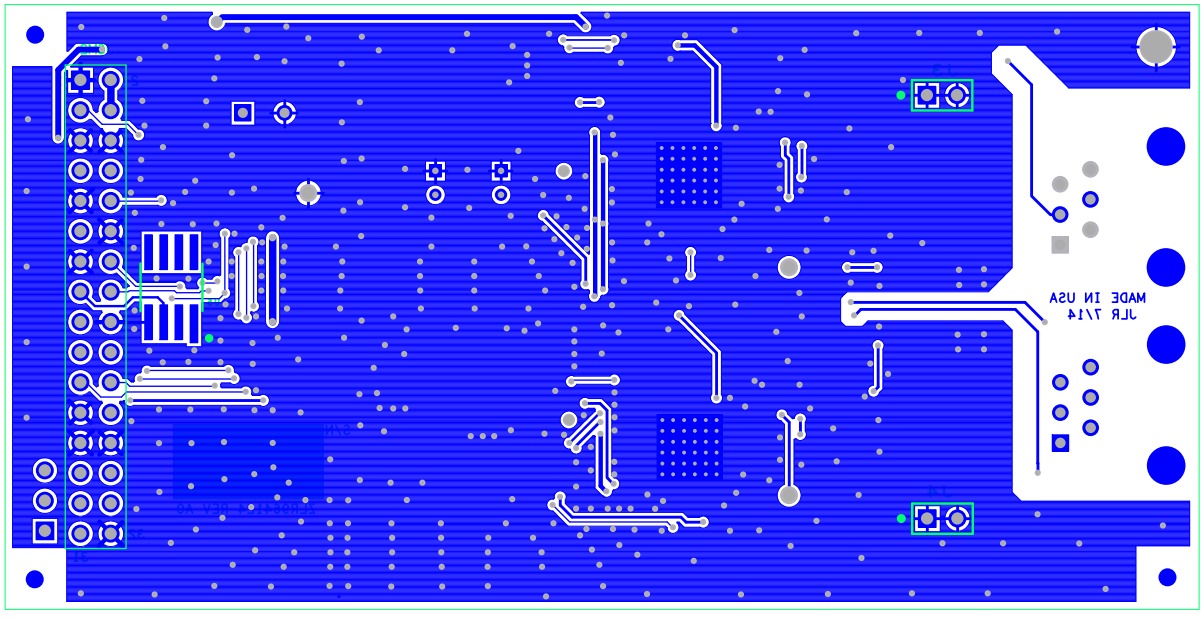

Figure 31 - Bottom Etch and Silk Screen

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