**SIVA CHIDAMBARAM**

**Sr Silicon Validation Engineer | ATE Characterization Engineer | Advantest V93k SM7 and SM8**

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**SUMMARY**

A results-driven professional with 4+ years of experience in post-silicon validation on test planning, program development, test cost optimization, yield improvement and die harvesting for digital SoCs using Advantest Verigy93k SM7 and SM8 ATE platform. Proficient in test program development, DIB hardware verification, yield analysis, test time optimization ensuring throughput with less test costs and time to market. Experienced in WS, FT insertions, and Qual, RMA analysis, and debug. Strong communication and project management skills, collaborating with cross-functional teams on program development, validation, and deployment, mentoring juniors, and adept at working independently or as part of a team.

**WORK EXPERIENCE**

**Sr. Silicon Validation Engineer Jan 2021-Present**

Tessolve Semiconductor Pvt Ltd, Bengaluru, India

* Test Program Integration Engineer for wafer and package-level testing for Snapdragon MDM/MSM 5G digital SOC NPI, AU/AQ Telematics SOC NPI, and other ARM, High-power server chipsets R&D.
* Responsible for hardware setup and deployment for testing across sites, engineering and multisite bring-up, handling program version control from power-on to ES/CS releases and managing IP level teams efficiently.
* Responsible for test program bring-up, resolve debug issues and integration for WS/FT insertions for production screening, Qual, HTOL, ORT/ORM and RMA, with QA checks ensuring test programs meet standards.
* Responsible for CONT, IP char and code level implementation for characterization across PVT, and validation.
* Proficient in Smartest debug tools including Timing analysis, Shmoo, Error map, Pin Margin and Current/Voltage profile analysis, for validating RMA rejects, production fallouts for continuous yield improvement.
* Monitoring production data, test program KPI, implementing test time reduction strategies and coverage optimization.
* Worked on Test Method libraries for per-core peak power testing, partial binning, and DOU equations.
* Implemented application specific Die-harvesting and Partial binning logic to optimize yield.
* Collaborating with IP level teams, DV/DFT, OSATs, Product Engineering and Ops teams to ensure timely delivery, remote debugs, data collection, analysis, program validation, releases, DOE analysis and process improvement.
* Good knowledge on IP level implementation for structural and functional tests, burn-in tests, advanced fault models, protocol-aware, mixed signal and parametric testing.

**TECHNICAL SKILLS**

* Operating System: Windows, Linux/Unix, MacOS
* Tester Platform: Advantest V93k, MaxTC, Hontech handlers, TCU and prober units
* Software: Smartest 8,7 with smart-RDI and C++, Java Test Methods and libraries
* Scripting: Shell, Perl and Python, DSA concepts
* Collaboration and project management using Agile via Jira, and Version control with GIT/SVN
* Data analysis with Excel, JMP, Exensio and Optimal+ tools for continuous KPI monitoring

**AWARDS AND ACHIEVEMENTS**

* Best paper award for publication in NCSPCN 2020, for UG project on ‘Smart Andon System’
* Best performer awards in **Sept 2021, Mar 2022** and **Jan 2025** for exceptional performance and mentoring.
* Quarterly award for **Q2 2021-22** and **Q3 2022-23**, on process improvements, new client preparation activities and extensive support for new test strategy implementation on NPI bring-up.

**EDUCATION**

**B.E., Electronics and Communication Engineering,** Nov 2020 **7.84 CGPA**

Ramco Institute of Technology, Anna University

Full time degree with coursework focused on Electronics including VLSI, LIC, digital and analog electronics, advanced microprocessors & microcontrollers, digital signal processing, communication systems and embedded systems.

**ADDITIONAL INFO**

* Linguistic proficiency: English, Tamil, Hindi, Telugu
* Location: Bengaluru, India (willing to relocate)
* Avid reader and curious to learn, research, tools development and scripting.
* Hobbies in Graphic design, art and music
* Business associate in family-run ventures and possess team management and analytical skills