BLOCK DAIGRAM:

- CycleCounter: This module is responsible for counting cycles based on two input clocks. It has an output count which is updated based on the cycle count
- input_status: This module manages the status of input clocks and an enable signal. It generates an output clock based on the enable signal and the input clock.
- code_div: This module divides the clock signal based on a certain condition. It takes input clocks and an enable signal and generates an output clock.
- top_level: This module acts as a top-level wrapper. It connects the input clocks and enable signal to input_status and passes the output clock to code_div. It also manages clock signals internally.
- tb_top_level: This is the testbench module. It instantiates the top_level module and provides input signals (ph_clk, mc_clk, en) as well as captures the output (clk_out). It also generates clock signals for testing.

The block diagram would illustrate these modules and their interconnections. Here's a textual representation: