S SIVA PRASAD

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DOB: 24-10-1994 **Location**: Thiruvananthapuram, Kerala **Citizenship**: Indian

Work Experience

Position : Project Engineer, **CDAC - Trivandrum** May 2018 – Present

Digital System Design - IP core desgin, development and testing
Design,development and testing of **IIC master controller , IIS master controller, AXI4 Display controller, AXI4 Crossbar** in Verilog/VHDL/BlueSpec.

ASIC tapeout of a RISC-V based Single core SoC on 130nm node
ASIC realization from RTL to GDS tapeout of a single core SoC design on 130nm node technology.
Full PnR flow - Preparing constraints, Floorplanning, Power Grid creation, Routing, SignOff timing (MMMC) , SI checking using Cadence EDA tools.

ASIC tapeout of a RISC-V based Single core SoC on 180nm node
ASIC realization from RTL to GDS tapeout of a single core SoC design on 180nm node technology.
Floorplanning, Power Grid creation, Routing, SignOff timing (MMMC) , SI checking using Cadence EDA tools.

Single/Dual/Quad core RISC-V based SoC design and Realization and testing on FPGA
Integration of various IP cores (Ethernet, SDRAM, DDR4,UART) to a RISC-V SoC design, simulation and FPGA (Xilinx Ultrascale) validation and Debugging.
Paritioning a multi-million gate design and implementing across two FPGA using Veloce prototyping system and Debugging using Exostiv/ChipScope.

ASIC Backend flow for a Dual core SoC on 28nm node
ASIC prototype of a dual core SoC design on 28nm node technology

PCB board Design
Design and development of a prototype PCB board with HDMI PHY, IIC/SPI/QSPI memory and SDRAM.

Other Experience

Digital System Design - IP core desgin, development and testing

Design,development and testing of **RISCV32-IMAF** 3-stage pipeline processor core, AXI4 Crossbar ,AXI4 Clock Converter, SPI/QSPI master controller, UART controller, AXI4 TO APB converter, JTAG Master controller in CHISEL. Details of which are available here.
Designed, Implemented and Successfully tested AES encryption in hardware (VHDL).
ASIC Implemenation of Single Core SoC from RTL design to GDS using Skywater-Google 130nm OpenSource PDK.
PCB design and successful implementation of high end I2S stereo DAC borad for Raspberry Pi board.

Sucessfully completed two independent standalone MPW tapeouts on 130nm SKYWATER foundry organised by Google's OpenMPW initiative programme. Details of MPW tapeout 1 and 2 are available here and here.

Achievements

Completed 4 MPW tapeouts (2 in official capacity, 2 personal) over a span of 1 year.
Best performance Award - CDAC Thiruvananthapuram 2019-2020.

Education

M. Tech — Kalam Technical University
VLSI & EMBEDDED SYSTEMS — 2016-2018
Engineering Research & Development Centre of India — CGPA - 9.0

B. Tech — University of Kerala
ELECTRONICS & COMMUNICATION — 2012-2016
Sree Chitra Thirunal College of Engineering — CGPA - 8.2

HSE — CBSE
Kendriya Vidyalaya — % 92.5

Presentations & Workshops

Presented a paper on Clock Cuncurrent Optimization at RISC-V international conference at IIT-Madras
Conducted workshops on Arduino programming in 2 colleges in Trivandrum

Skills

Programming
Proficient in RTL languages : VHDL, Verilog, CHISEL, BlueSpec
Tools
ASIC EDA Tools : Genus (synthesis), Innovus (PnR), Tempus (SignOff timing).
OpenSource EDA Tools : Yosys (synthesis), Magic (PnR).
PCB development Tools : Allegro, KiCad.
FPGA development Tools : Vivado, Lattice Diamond
Microcontroller development - Arduino, ESP8266 for IoT, Raspberry Pi Pico
Microprocessor development - Raspberry Pi
Other

TCL, Python (basic)

Languages

English, Hindi, Malayalam

Other interests

Cricket.