

# **DESIGN OF LOW NOISE AMPLIFIER USING FRACTAL INDUCTOR FOR 5G APPLICATIONS**

*A report on major project work*

Submitted in the partial fulfillment of the requirements for  
the award of the degree of

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*in*

**ELECTRONICS AND COMMUNICATION ENGINEERING**

*by*

<b>BANDI SRAVANI</b>	<b>B21EC101</b>
<b>KOYALKAR SAHITH</b>	<b>B21EC094</b>
<b>KANNE RETHIL</b>	<b>B21EC096</b>

Under the guidance of

**P.CHIRANJEEVI**

Assistant Professor,  
Department of ECE.



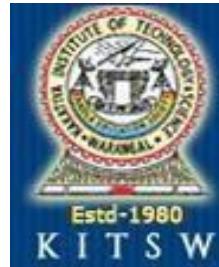
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**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**



**CERTIFICATE**

This is to certify that the project work entitled "**DESIGN OF LOW NOISE AMPLIFIER USING FRACTAL INDUCTORS FOR 5G APPLICATIONS**" is the bonafide project work phase I carried out by **B. Sravani, K.Sahithi, and K.Rethil** bearing Roll.Nos. **B21EC101, B21EC094, and B21EC096** respectively, in partial fulfilment of the requirements for the award of degree of the Bachelor of Technology from Kakatiya Institute of Technology and Science, Warangal during the academic year 2024-2025.

**Project Guide**

**P. Chiranjeevi,**  
Assistant Professor,  
Dept. of ECE,  
KITS, Warangal.

**Head of the Department**

**Dr. V. Venkateswar Reddy**  
Associate Professor & Head,  
Dept. of ECE,  
KITS, Warangal.

## **DECLARATION**

We declare that the work presented in this project report is original and has been carried out in the Department of Electronics & Communication Engineering, Kakatiya Institute of Technology and Science, Warangal, Telangana, and to best of our knowledge it has been not submitted elsewhere for any degree.

**BANDI SRAVANI**

Roll No. B21EC101

**KOYALKAR SAHITHI**

Roll No. B21EC094

**KANNE RETHIL**

Roll No. B21EC096

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**BANDI SRAVANI**

**KOYALKAR SAHITHI**

**KANNE RETHIL**

## **ABSTRACT**

This project aims to design a high-performance Low Noise Amplifier (LNA) for 5G applications using fractal inductors. Inductors are essential in the design of radio frequency integrated circuits (RFICs). However, they often occupy a significant amount of space and exhibit a low-quality factor at high frequencies. Using fractal structures in on-chip inductors can enhance the quality factor, reduce the overall area, and improve the inductance value. 5G technology requires components that are fast, efficient. Fractal inductors, with their unique geometry, can help make the LNA improves its performance at high frequencies.

The advanced simulation tools to design and evaluate different fractal inductor geometry. The primary objective is to reduce noise figure and increase the amplifier's gain, making it more efficient. S-parameters contribute to LNA performance by evaluating input matching ( $S_{11}$ ), gain ( $S_{21}$ ), isolation ( $S_{12}$ ), and output matching ( $S_{22}$ ), crucial for efficient signal amplification and minimal signal reflection.

The use of fractal inductors in the LNA design significantly improves its performance. This approach offers an optimistic solution for creating better and compact components for 5G networks. The project demonstrates that fractal inductors can enhance LNA performance, supporting the advancement of next-generation wireless communication technologies.

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# **CHAPTER-1**

## **INTRODUCTION**

The rapid advancement of wireless communication technologies has transformed the way the world connects and interacts, with 5G standing as a revolutionary milestone. Unlike its predecessors, 5G offers enhanced data rates exceeding 10 Gbps, ultra-low latency below 1 ms, massive network capacity, and the ability to connect billions of devices simultaneously[3]. This transformation not only enables existing applications to flourish but also paves the way for entirely new innovations such as autonomous vehicles, remote surgeries, industrial automation, augmented reality (AR), virtual reality (VR), and advanced IoT ecosystems. These diverse applications require hardware that is not only robust and efficient but also compact and scalable.

Fractal inductors are a unique type of inductor that leverage the principles of fractal geometry to achieve high inductance values within a small footprint. This innovative design enables efficient operation in high-frequency electronic circuits, where space is a premium and high inductance is essential[2].

Fractal inductors employ intricate, self-repeating patterns to maximize conductor length within a confined area. This extended conductor path directly translates to higher inductance values. The compact nature of these inductors makes them ideal for applications where space is limited, such as mobile devices and wearable electronics.

While fractal inductors hold significant promise, challenges remain in their fabrication and modeling. The complex geometry of these inductors can pose manufacturing difficulties, and accurate modeling is crucial for optimal design[1].

Every wireless receiver lies the Low Noise Amplifier (LNA), a fundamental building block responsible for amplifying the extremely weak signals received by the antenna. LNAs ensure that the amplified signals are strong enough for further processing while introducing minimal additional noise[8]. Their role is critical, especially in 5G systems where the high operating frequencies in the millimeter-wave bands pose unique challenges. A poorly designed LNA can degrade the overall system performance, reducing sensitivity, and ultimately impacting the quality of service. Therefore, optimizing the performance of LNAs is crucial for meeting the stringent requirements of 5G networks[7].

The design of LNAs for 5G applications is inherently challenging. Unlike lower-frequency systems, millimeter-wave frequencies (30–300 GHz) exacerbate issues such as parasitic effects, signal losses, and noise contributions. Achieving a balance between key performance metrics—such as low noise figure, high gain, wide bandwidth, and low power consumption—requires innovative design methodologies[11]. Furthermore, the trend toward compact and integrated solutions adds another layer of complexity, as designers must optimize performance within tight physical constraints.

To address these challenges, the use of fractal inductors in LNA design has emerged as a promising approach. Fractal inductors are a class of inductive components characterized by self-similar, recursive geometries. These geometries allow fractal inductors to achieve higher inductance values in a smaller area compared to conventional spiral or planar inductors. They also offer an improved quality factor (Q-factor) and extended self-resonant frequency, making them particularly advantageous for high-frequency applications like 5G. The compact nature of fractal inductors enables efficient use of space, allowing for miniaturized designs that meet the demands of modern integrated circuits[6].

The integration of fractal inductors into LNA design presents multiple benefits. At high frequencies, maintaining a low noise figure is critical, as any noise added during amplification degrades the signal-to-noise ratio (SNR). Fractal inductors help reduce noise by offering high-quality inductance, minimizing power dissipation and losses. Additionally, their small size supports the development of multi-functional RF circuits in space-constrained environments, such as mobile devices and IoT modules. These characteristics position fractal inductors as a transformative technology for the next generation of wireless communication systems[5].

This study focuses on the design, simulation, and optimization of an LNA using fractal inductors for 5G applications. The proposed design aims to achieve superior noise performance, high gain, and wideband operation while maintaining a compact form factor. Simulation tools such as Advanced Design System (ADS) will be employed to validate the performance of the design under realistic conditions. The research also aims to explore the trade-offs involved in using fractal inductors, providing a detailed analysis of their impact on LNA performance metrics[9].

The significance of this work lies not only in addressing the immediate challenges of 5G hardware design but also in contributing to the broader field of RF and microwave circuit

design. By leveraging fractal geometries, this research introduces a novel approach that has the potential to influence the design of a wide range of electronic components beyond LNAs, including filters, oscillators, and matching networks.

In summary, this chapter underscores the critical importance of LNAs in 5G communication systems, the challenges associated with designing high-performance LNAs, and the innovative role of fractal inductors in overcoming these challenges. This study bridges the gap between theoretical advancements and practical implementation, aiming to provide a scalable and efficient solution for 5G hardware design[2]. The subsequent chapters will delve deeper into the theoretical foundations of fractal inductor technology, the design methodology of the LNA, and the experimental validation of the proposed approach, ultimately demonstrating its feasibility and potential for real-world applications.

## **CHAPTER 2**

### **LITERATURE REVIEW**

Inductors are crucial components of on-chip radio frequency components. According to Saberhosseini et al. (2016), the quality ratio is a crucial design parameter for inductors, which are used in high-performance radio frequency circuits such as voltage-controlled oscillators and low-noise amplifiers. Regrettably, parasitic factors like substrate losses and capacitance couplings cause the inductor's efficiency to decline. These days, mobile communication devices like cell phones and wireless networks, as well as low-cost, good-performance on-chip radio-frequency devices and microwave integrated circuit applications, require inductors with an excellent performance factor and small area of occupancy. A multipath circular helical inductor was presented in this study. By lowering skin irritation or closeness effects, the multipath approach raises the inductors' quality factor.[1]

In this short, we provide a unique multipath parallel-stacked inductor topology that greatly minimizes the consequences of current crowding. The parallel stack's two metal layers are split into several segments, with crossovers positioned in the middle of each turn to direct the currents such that each segment has an equal travel length. Prototype inductor structures are made in 0.18- $\mu\text{m}$  high-resistivity silicon-on-insulator tech utilizing a twin thick metal stack method, according to the multipath design. Measurements indicate that the suggested architecture improves the quality factor ( $Q$ ) by over 30% when compared to a typical parallel-stacked inductor. We provide a new multipath parallel-stacked inductor topology in this brief that greatly diminishes the current crowding effects. The parallel stack's two metal layers are split into several segments, and crossovers are positioned in the middle of each turn to direct the currents such that each segment has an equal travel length. Prototype inductor structures are made in a 0.18- $\mu\text{m}$  high-resistivity silicon-on-insulator tech utilizing a twin thick metal stack technique, according to the multipath design. Measurements indicate that the suggested architecture improves quality factor ( $Q$ ) [4]

The paper presents an innovative suspended spiral inductor design incorporating a patterned ground shield (PGS) structure. The authors demonstrate that by elevating the spiral inductor above the substrate and implementing a specialized PGS pattern, substrate losses can be significantly reduced. 4 The design achieves this through air-gap isolation and strategic

placement of shield segments that minimize eddy current formation. Experimental results show a 45% improvement in quality factor compared to conventional designs while maintaining a compact footprint suitable for modern RF integrated circuits.[2]

This research introduces a symmetric interleaved dual-path inductor topology that addresses current distribution challenges in high-frequency applications. By implementing an interleaved structure with carefully balanced current paths, the design mitigates both proximity and skin effects. The authors developed their prototype using a 65nm CMOS process with triple-thick metal layers. The measured results demonstrate a peak Q-factor improvement of 38% over traditional single-path designs while maintaining similar self-resonant frequency characteristics.[7]

The authors present a novel approach to inductor design utilizing three-dimensional solenoid architecture. By leveraging vertical space rather than traditional planar structures, the design achieves superior magnetic coupling and reduced parasitic capacitance. The 3D structure is fabricated using advanced through-silicon via (TSV) technology in a  $0.13\mu\text{m}$  process. Experimental results indicate a 50% reduction in area occupancy while maintaining a quality factor comparable to conventional planar designs, making it particularly suitable for dense RF circuit integration.[5]

This paper explores the integration of magnetic core materials within a transformer-based inductor structure to enhance inductance density. The proposed design incorporates a specialized composite magnetic material that maintains high permeability up to GHz frequencies while minimizing eddy current losses. Through careful optimization of the magnetic layer thickness and winding geometry, the authors achieve a 65% reduction in footprint compared to air-core designs. Measurements show that the magnetic enhancement provides a 40% improvement in quality factor at the target frequency of 2.4 GHz, making it particularly suitable for modern wireless communication applications.[6]

## CHAPTER 3

### SOFTWARE REQUIREMENT

The design and development of advanced electronic components, such as a Low Noise Amplifier (LNA) for 5G applications, require precise simulation, analysis, and optimization tools. Software plays a pivotal role in every phase of the development process, from conceptualization and modeling to verification and performance evaluation. The complexity of modern RF and microwave circuits, coupled with the stringent performance requirements of 5G systems, necessitates the use of specialized software to ensure accuracy and efficiency.

For the design and simulation of the LNA with fractal inductors, several software tools are essential. These tools assist in performing tasks such as schematic design, circuit simulation, electromagnetic (EM) analysis, and layout generation. Each software package brings unique capabilities that cater to specific stages of the design workflow, ensuring that the final product meets the desired specifications.

#### **1. Applied Wave Research(AWR):**

AWR Design Environment, developed by Cadence Design Systems, is a powerful electronic design automation (EDA) software platform specifically tailored for the design and simulation of RF, microwave, and high-frequency circuits. Widely used in academic research and industry, AWR provides a comprehensive set of tools for the development of components such as Low Noise Amplifiers (LNAs), power amplifiers, filters, mixers, and antennas. Its user-friendly interface, coupled with robust simulation capabilities, makes it an essential tool for engineers working on advanced communication systems, including 5G applications.



Fig no 3.1.1.1: Tool Used For Inductor design

### **3.1.1. Design Environment:**

AWR offers an intuitive design environment that allows engineers to create, simulate, and analyze RF/microwave circuits and systems efficiently. The user interface is user-friendly and highly customizable, providing easy access to design tools and simulation capabilities.

### **3.1.2 EM Simulation:**

A key feature of AWR is its electromagnetic (EM) simulation capabilities, which allow engineers to analyse the electromagnetic behaviour of RF/microwave structures, such as transmission lines, antennas, and RF interconnects.

### **3.1.3. Circuit Simulation:**

AWR supports various types of circuit simulation, including linear and nonlinear analysis, time-domain simulation, and frequency-domain simulation. The tool provides accurate modeling of passive and active components, such as resistors, capacitors, inductors, transistors, amplifiers, and filters.

### **3.1.4. System Simulation:**

AWR facilitates the simulation of complex RF/microwave systems, allowing engineers to analyze system-level performance, including gain, noise figure, and intermodulation distortion.

System-level simulation capabilities enable the evaluation of system architectures, signal integrity, and RF propagation effects

### **3.1.5. Optimization and Yield Analysis:**

AWR includes optimization tools that allow engineers to automatically tune circuit parameters to meet design specifications and performance targets. Yield analysis capabilities enable engineers to assess the robustness of designs to variations in component values, manufacturing tolerances, and environmental conditions.

### **3.1.6. Integration with Third-Party Tools:**

AWR integrates seamlessly with other design and analysis tools, such as MATLAB, Python, and Cadence Virtuoso, allowing for enhanced design workflows and interoperability.

### 3.1.7. Design Management and Collaboration:

AWR provides features for version control, design management, and collaboration, allowing multiple engineers to work on the same project simultaneously. Collaboration tools enable efficient communication and sharing of design data, facilitating teamwork and project coordination.

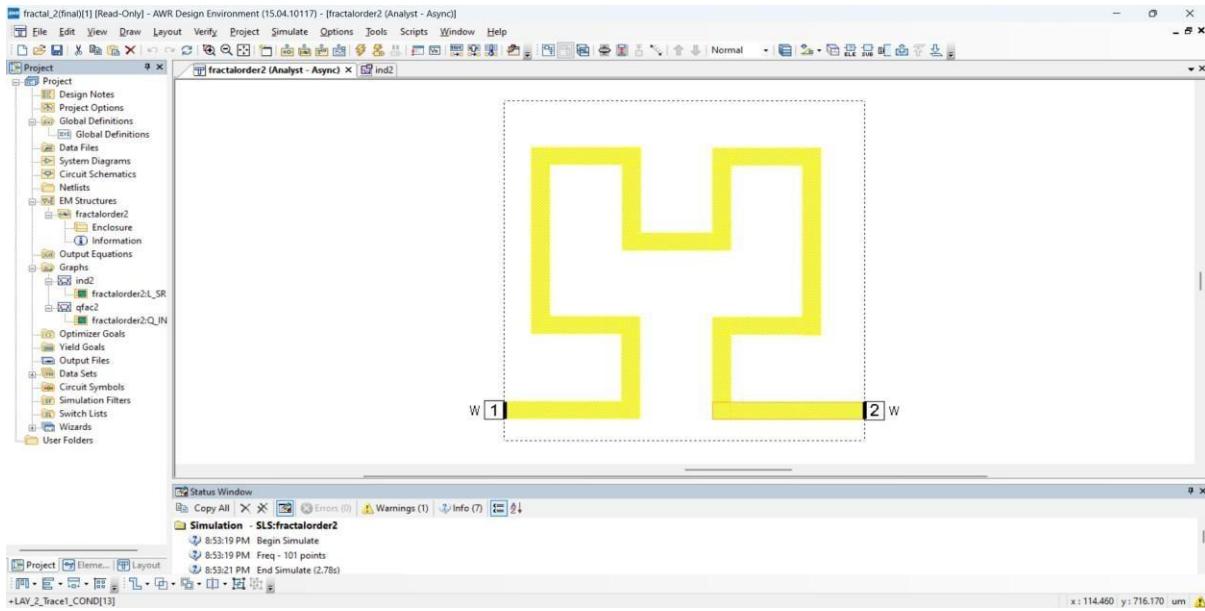


Fig.no.3.1.2.1 2<sup>nd</sup> order Hilbert Inductor Design

### 3.1.8. 3D View of Fractal Inductor:

AWR offers specialized modules tailored to specific applications, such as RFIC (RF integrated circuit) design, antenna design, and PCB (printed circuit board) layout. These modules provide advanced features and automation capabilities to streamline the design process and improve productivity.

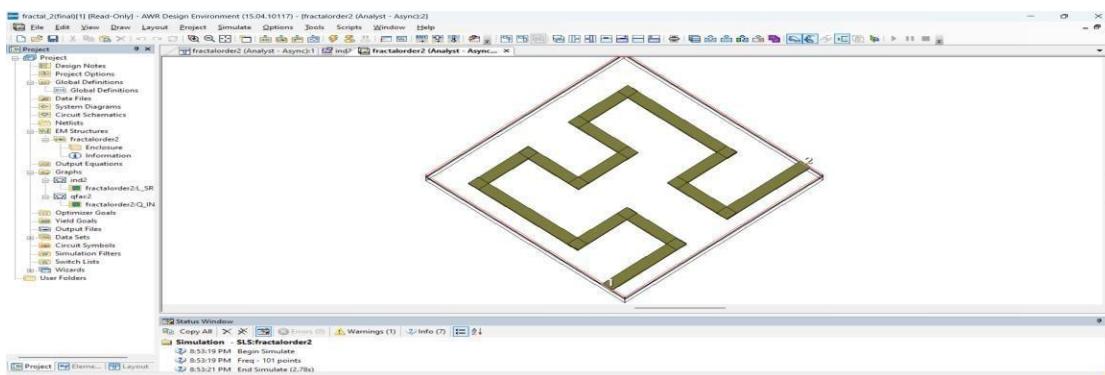


Fig.no.3.1.3.1: 3D- View of 2<sup>nd</sup> order Hilbert Inductor

## 2. Advanced Design System(ADS):

ADS is a leading electronic design automation (EDA) software developed by Keysight Technologies. It is widely used in RF, microwave, and high-frequency circuit design.



Fig.no.3.1.4.1: Tool used For Design Of LNA

ADS provides a comprehensive suite of tools for schematic design, circuit simulation, and layout optimization. For this project, ADS is essential for creating and simulating the LNA circuit. It enables designers to analyze critical parameters such as noise figure, gain, input/output matching, and stability across the operating frequency range.

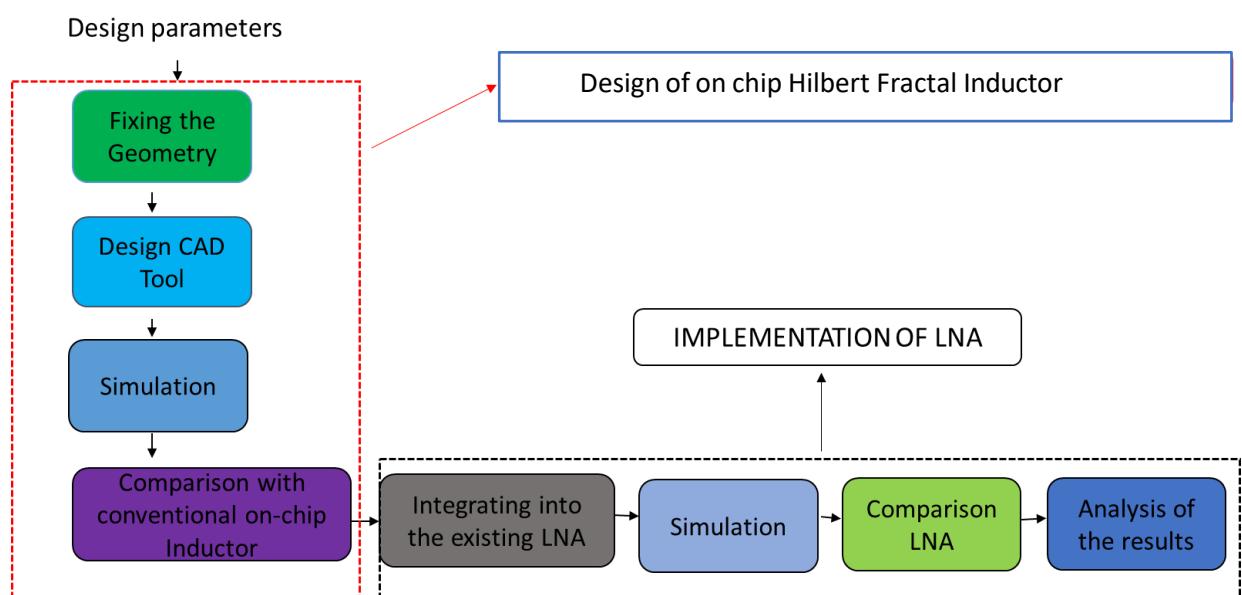


Fig.no.3.1.5.1: Project Implementation

## **CHAPTER 4**

### **OBJECTIVE OF THE PROJECT**

The primary objective of this project is to design an on-chip Hilbert fractal inductor with enhanced performance metrics and integrate it into a Low-Noise Amplifier (LNA) for 5G applications. Traditional spiral inductors, often used in LNAs, suffer from significant limitations, including low-quality factor (Q-factor), high parasitic effects, and large chip area requirements. These issues make them less suitable for high-frequency applications, particularly in the mm-Wave range critical for 5G networks. To overcome these challenges, the Hilbert fractal inductor is proposed as a compact and efficient alternative, providing improved Q-factor, minimized parasitics, and reduced area usage.

The project emphasizes designing the Hilbert fractal inductor through iterative refinements to optimize critical parameters like Q-factor and inductance. Using AWR EDA tools, multiple design iterations are performed to evaluate the impact of fractal geometry on the inductor's electrical characteristics. These iterations identify the optimal configuration that achieves the best balance between inductance, Q-factor, and compactness within a constrained area of  $100 \mu\text{m} \times 100 \mu\text{m}$ .

After selecting the optimal iteration, the proposed Hilbert inductor is compared against traditional spiral inductors. This evaluation underscores the superior performance of the Hilbert fractal inductor, showcasing its potential for high-frequency 5G applications. The optimized inductor is then integrated into an LNA circuit, and performance analysis is conducted using ADS EDA tools. Key performance metrics, such as gain, noise figure, and impedance matching, are analyzed to validate the efficacy of the proposed design in improving LNA functionality while maintaining compactness and efficiency.

By achieving these objectives, this project highlights the practical feasibility of Hilbert fractal inductors for next-generation RF systems. The outcomes are expected to make significant contributions to the development of compact, energy-efficient, and high-performance circuits, addressing the stringent demands of 5G communication networks, radar systems, and other advanced wireless technologies.

## CHAPTER 5

### EXISTING METHOD

#### 5.1.1 Spiral Inductors:

Spiral inductors are essential passive components in RF and analog integrated circuits, widely utilized for their straightforward design and compatibility with CMOS and BiCMOS processes. Fabricated on silicon substrates using planar spiral patterns, these inductors are well-suited for integration in modern ICs. They are commonly employed in oscillators, filters, and impedance-matching networks, playing a critical role in various applications. Advantages of Spiral Inductors

Spiral inductors offer ease of fabrication using standard photolithographic techniques, making them cost-effective for large-scale production. Their planar structure ensures compact integration into IC layouts, minimizing chip area usage. These inductors function effectively across a wide frequency range, from MHz to GHz, depending on their design. Additionally, their inductance values can be customized by adjusting parameters such as the number of turns, spacing, and dimensions, offering scalability for diverse applications.

#### Design of Spiral Inductors

The design of spiral inductors typically involves single-layer or multi-layer planar structures, with the inductance determined by the number of turns, conductor width, and spacing. Conductive metals like aluminium or copper are used, supported by a silicon substrate. Designers must account for parasitic capacitance to avoid self-resonance within the desired frequency range. Optimization of parameters such as conductor width, turn-to-turn spacing, and substrate material is critical to balancing inductance, Q-factor, and chip area requirements.

#### 5.1.2 Key Characteristics of Spiral Inductors:

The inductance of a spiral inductor is proportional to the number of turns and the area it encloses. Smaller spirals provide lower inductance, while larger spirals offer higher values but consume more chip area. The Q-factor, which measures energy efficiency, is influenced by resistive losses in the conductor and substrate coupling losses. As frequency increases, inductance decreases due to parasitic effects, and the Q-factor peaks before dropping beyond

the self-resonant frequency. The planar design also leads to magnetic coupling between adjacent turns, impacting inductance and losses.

### **5.1.3 Challenges in Spiral Inductor Designs:**

One of the major challenges in spiral inductor design is parasitic capacitance introduced by the silicon substrate, which degrades performance at high frequencies and lowers the self-resonant frequency. Resistive losses, exacerbated by the skin effect and proximity effects at high frequencies, further reduce the Q-factor. Substrate losses caused by eddy currents dissipate energy, decreasing efficiency. Additionally, achieving high inductance values requires larger structures, which occupy significant chip area and limit their use in compact designs.

### **5.1.4 Performance Characteristics of Spiral Inductors:**

Spiral inductors exhibit variability in inductance with frequency due to parasitic capacitance and substrate losses, which can impact circuit stability in high-frequency applications. The Q-factor peaks within a certain frequency range but decreases significantly beyond the self-resonant frequency. Resistive losses generate heat, affecting thermal stability and performance in high-power applications. Although spiral inductors perform well up to several GHz, their efficiency diminishes rapidly at higher frequencies due to these limitations.

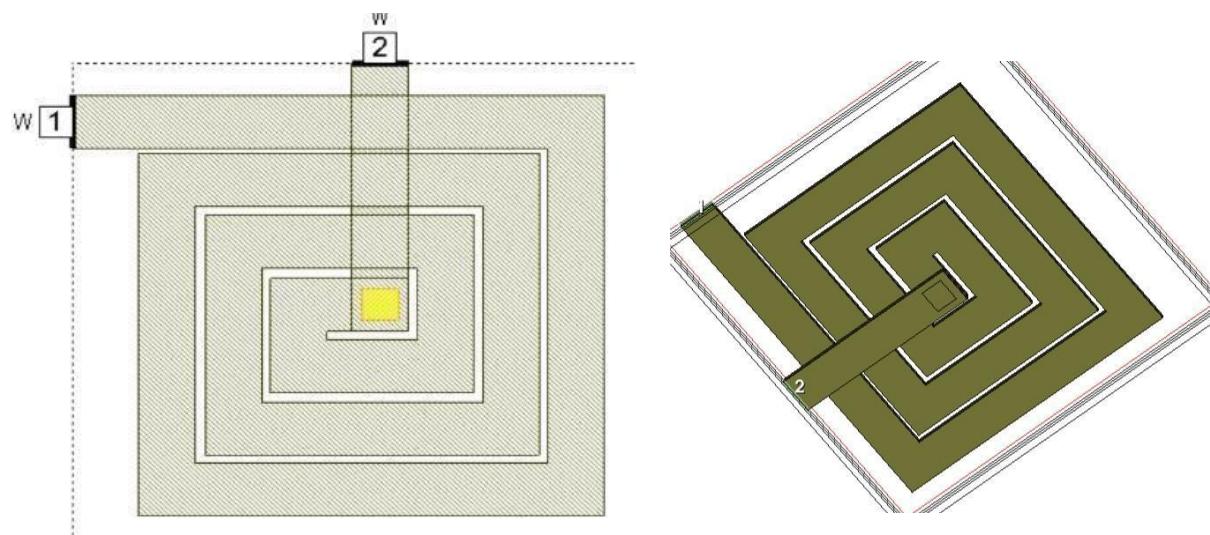


Fig.no.5.1.1.1: Spiral inductor and 3D view of spiral inductor

### 5.1.5 SIMULATION AND RESULT:

The simulation results for a spiral inductor typically include values for inductance and quality factor, which vary based on design parameters and operating conditions. Inductance, measured in nanohenries (nH) or microhenries ( $\mu$ H), depends on factors no.of.turns of spiral.

Turn of spiral inductor	Thickness ( $\mu$ m)	Width ( $\mu$ m)	Inductance (nH)	Q-factor
Turn 1	2	10	0.01234(30GHZ)	4
Turn 2	2	10	0.123(41GHZ)	4
Turn 3	2	10	0.1567(41GHZ)	9

Table No:5.1

(Inductance and Q-factor values Of Spiral Inductor with Different Turns

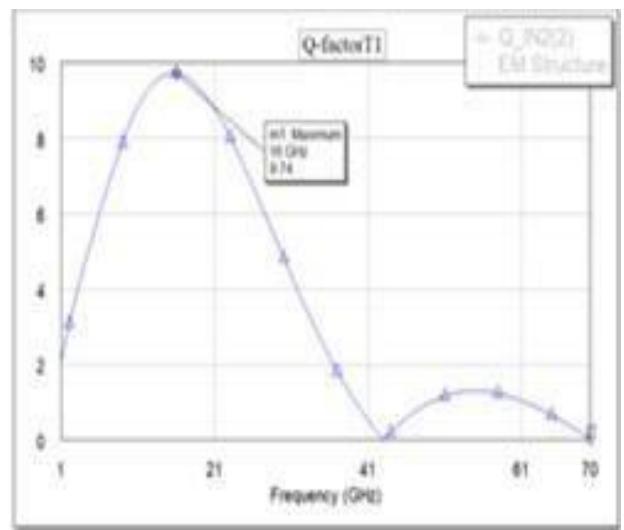
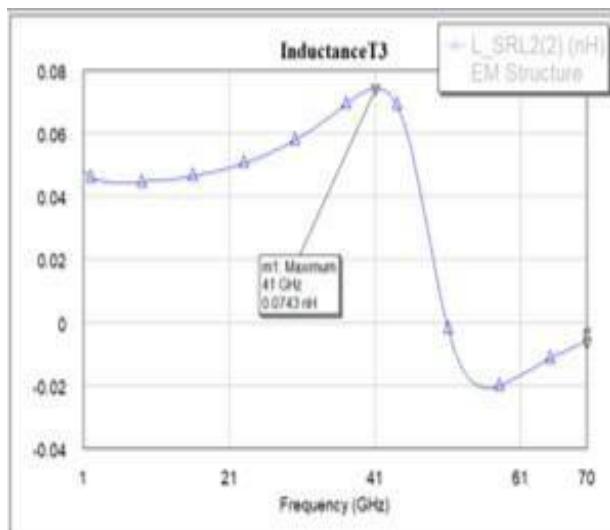


Fig.no5.1.2.1: Spiral inductor Inductance Graph Fig.no.5.1.3.1: Spiral inductor Q-Factor

# **CHAPTER 6**

## **METHODOLOGY**

To address the shortcomings of spiral inductors, this project explores the implementation of a Hilbert fractal inductor. The Hilbert fractal inductor utilizes self-repeating geometric patterns to achieve a longer conductor path within a compact layout, effectively minimizing parasitic effects and enhancing the Q-factor. This innovative design is anticipated to improve inductor performance, particularly in high-frequency applications crucial for 5G technologies.

The development of the Hilbert fractal inductor employs a structured methodology aimed at optimizing Q-factor and inductance within the constrained chip dimensions of  $100 \mu\text{m} \times 100 \mu\text{m}$ . The Hilbert fractal's strength lies in its recursive geometric architecture, which maximizes space efficiency while ensuring superior electrical performance.

### **6.1 Design Constraints:**

The Hilbert fractal inductor is designed with specific constraints to optimize its performance. The thickness of the inductor is fixed at  $2 \mu\text{m}$  for all iterations, ensuring consistency in the design while focusing on the effects of path width on the inductor's performance.

#### **6.1.1 First Iteration:**

In the first iteration, a basic Hilbert fractal structure is designed with a uniform path width. This serves as the initial test case, providing a baseline for evaluating the inductor's Q-factor and inductance.

#### **6.1.2 Second Iteration:**

In the second iteration, the path width is increased to  $10 \mu\text{m}$ . This modification aims to enhance the current-carrying capacity of the inductor, thereby improving the overall performance and reducing losses.

#### **6.1.3 Third Iteration:**

The third iteration involves further refinement by varying the path width between  $2 \mu\text{m}$ ,  $2.5 \mu\text{m}$ , and  $5 \mu\text{m}$ . These variations are intended to explore how different path widths influence the electrical characteristics, such as inductance and Q-factor, of the Moore fractal inductor.

Each iteration is designed and simulated using the AWR EDA tool, which provides detailed results on inductance, Q-factor, and parasitic losses. The goal is to identify the iteration that offers the best balance between inductance, Q-factor, and compactness, ensuring that the inductor meets the stringent performance requirements for high-frequency LNA applications.

## **6.2 Integration of Hilbert Fractal Inductor into LNA:**

Once the optimal Hilbert fractal inductor is selected from the iterative design process, it is integrated into a Low-Noise Amplifier (LNA) circuit. This integration is critical for demonstrating the practical benefits of the proposed inductor in real-world applications. Using ADS EDA tools, the modified LNA is simulated to evaluate key performance parameters such as noise figure, gain, input matching, and output matching. These parameters are crucial for assessing the overall performance of the LNA and determining whether the Moore fractal inductor offers tangible improvements over the traditional spiral inductor.

The simulation results from the LNA with the Hilbert fractal inductor are compared with those of the LNA using the spiral inductor to assess the impact on gain, noise figure, and overall efficiency. This comparison helps validate the proposed inductor design and its suitability for microwave applications.

## **6.3 Evaluation and Validation:**

The final step in the methodology involves a comprehensive evaluation of the results obtained from the simulations. The performance metrics of the Hilbert fractal inductor—specifically its inductance, Q-factor, and effect on the LNA's performance—are compared against those of the spiral inductor. This validation step ensures that the Hilbert fractal inductor outperforms the traditional design, demonstrating its potential for high-performance, compact RF circuits suitable for next-generation communication technologies.

In conclusion, this methodology aims to design, optimize, and integrate the Hilbert fractal inductor into an LNA circuit, providing a comprehensive solution to improve the performance of microwave applications. The approach emphasizes systematic design, iterative optimization, and real-world validation through LNA simulations to ensure the proposed inductor's effectiveness in enhancing RF circuit performance.

# CHAPTER 7

## IMPLEMENTATION OF PROPOSED METHOD

The design and implementation of the Hilbert fractal inductor for Low-Noise Amplifier (LNA) applications involves a systematic approach that includes the design of the inductor, simulation, and optimization using AWR EDA tools. This process focuses on developing a high-performance inductor that meets the requirements for microwave applications. Below is a detailed description of the design and implementation process.

### 7.1 Hilbert Fractal Inductor Design Process:

The design of the Hilbert fractal inductor begins with the specification of the geometric parameters. The key design constraints are the area ( $100 \mu\text{m} \times 100 \mu\text{m}$ ), thickness (2  $\mu\text{m}$ ), and different path widths for each iteration. The goal is to improve the inductor's quality factor (Q-factor) and inductance by adjusting the path width in each iteration.

#### 1. First Iteration:

The initial inductor design uses a simple Hilbert fractal structure with a uniform path width. The objective of the first iteration is to establish a baseline for performance, measuring inductance and Q-factor.

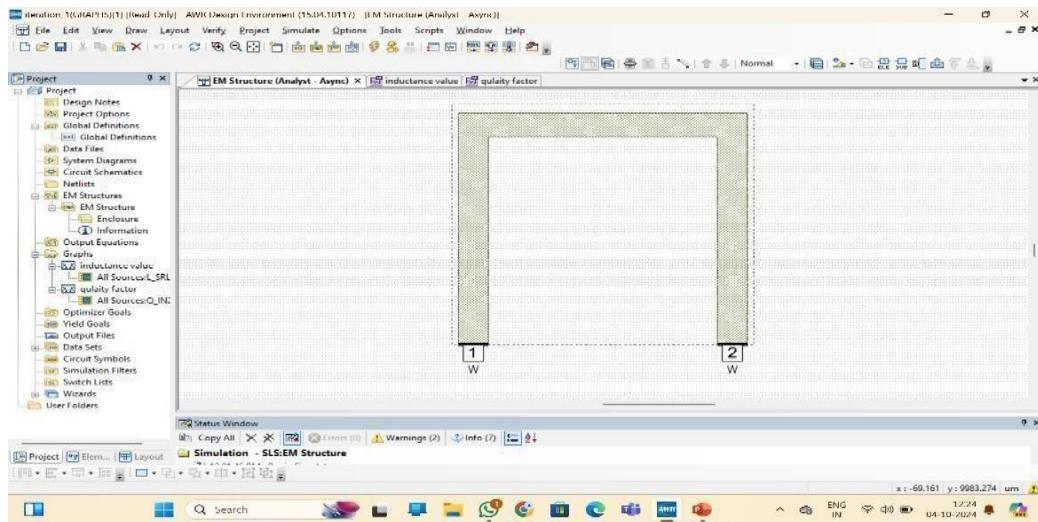


Fig.no.7.1.1.1: 1<sup>st</sup> Order Hilbert Fractal Inductor.

## 2. Second Iteration:

In this iteration, the path width is increased to 10  $\mu\text{m}$ . This adjustment is expected to enhance the current-carrying capacity of the inductor, improving the inductance and Q-factor.

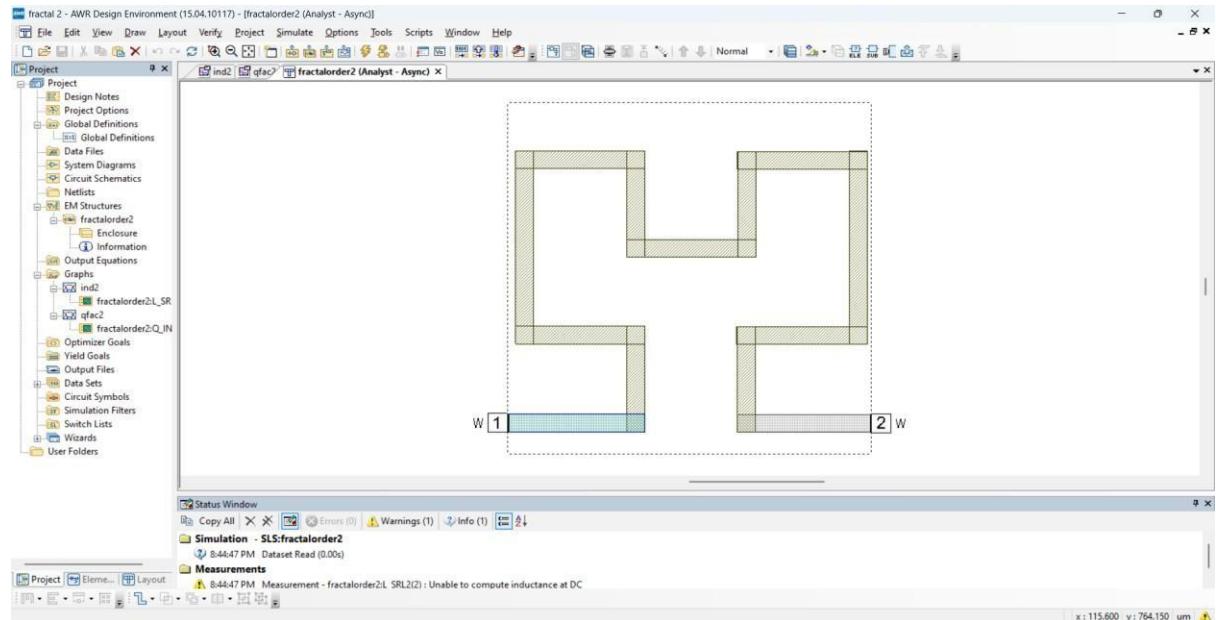


Fig.no.7.1.2.1: 2<sup>nd</sup> Order Hilbert Fractal Inductor

## 3. Third Iteration:

The third iteration introduces multiple variations in the path to investigate the impact of different widths on the overall performance of the inductor. The goal is to find the optimal combination of path width and inductance.

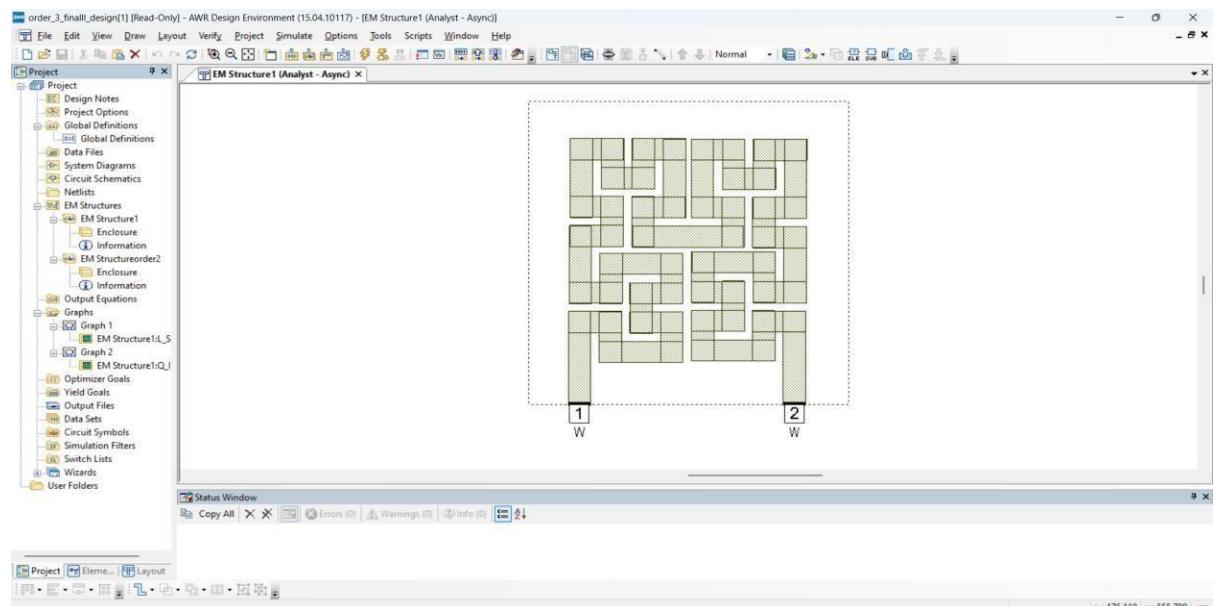


Fig.no.7.1.3.1: 3<sup>rd</sup> Order Hilbert Fractal Inductor.

The AWR Microwave Office tool is used for the design and simulation of the Moore fractal inductor. The tool allows for detailed analysis of the inductor's inductance, Q-factor, and parasitic losses, and it facilitates iterative optimization to meet the design objectives.

## 7.2 AWR Tool Flow:

The AWR Microwave Office tool is central to the design, simulation, and optimization of the Moore fractal inductor. The design process follows these main steps:

### 1. Geometrical Parameters:

The initial Hilbert fractal inductor layout is created using AWR's geometric layout editor. The design area is set to  $100 \mu\text{m} \times 100 \mu\text{m}$ , and the thickness is fixed at  $2 \mu\text{m}$ . The path width is adjusted for each iteration to evaluate its effect on performance.

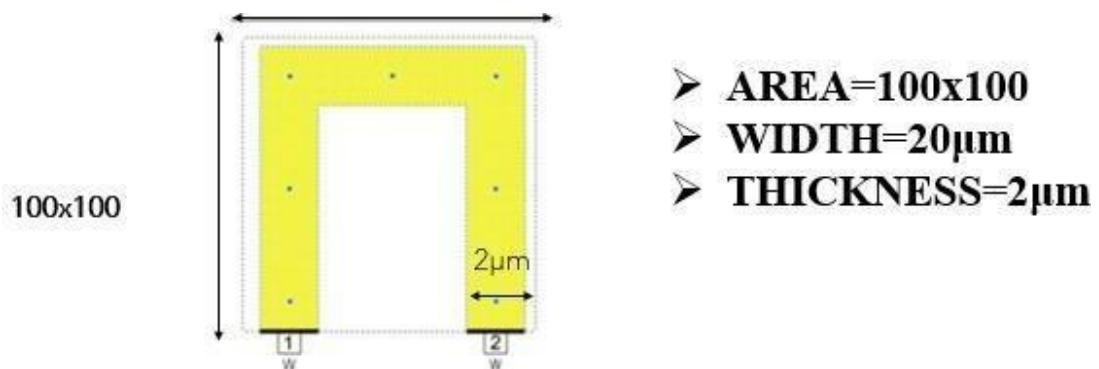


Fig.no.7.1.4.1: Geometric parameters of Fractal

### 2. Steps involved in Designing of Hibert Fractal Inductor:

The layout is then transferred to the simulator. AWR Microwave Office is used to simulate the electrical properties, including inductance, Q-factor, parasitic losses, for each iteration.

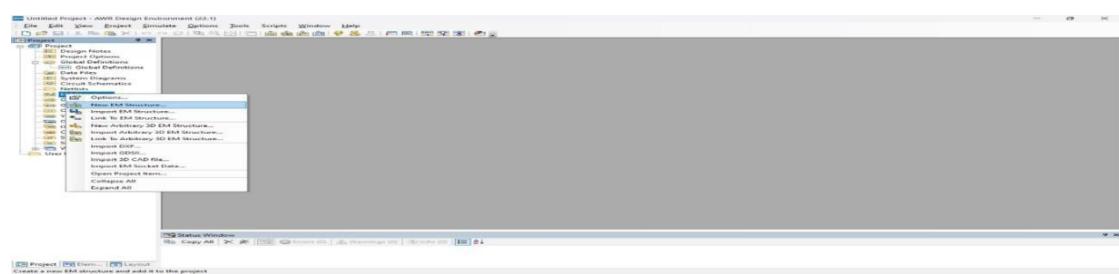


Fig.no.7.1.5.1:Creating New Em Structure Of Hilbert Fractal Inductor

### 3. Defining Materials Of Fractal:

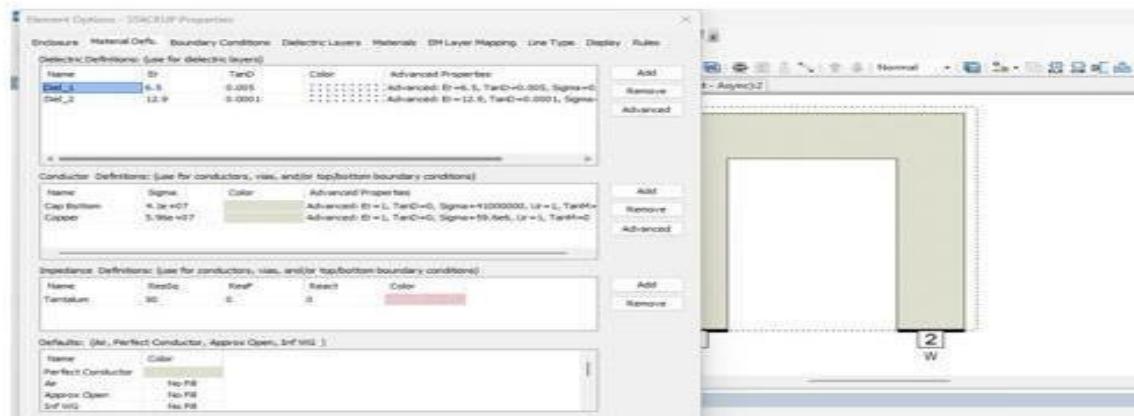


Fig.no.7.1.6.1:Material Defining Of Fractal

### 4 . Adding Boundary Conditions:

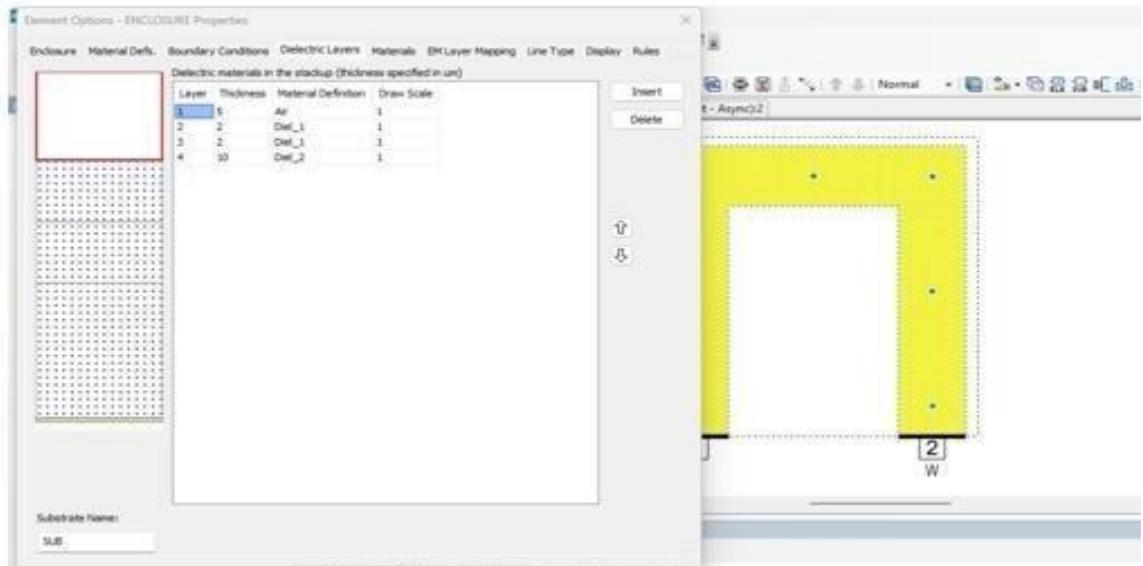


Fig.no.7.1.7.1:Adding Boundary Conditions To Fractal

### 5. Dielectric Materials:

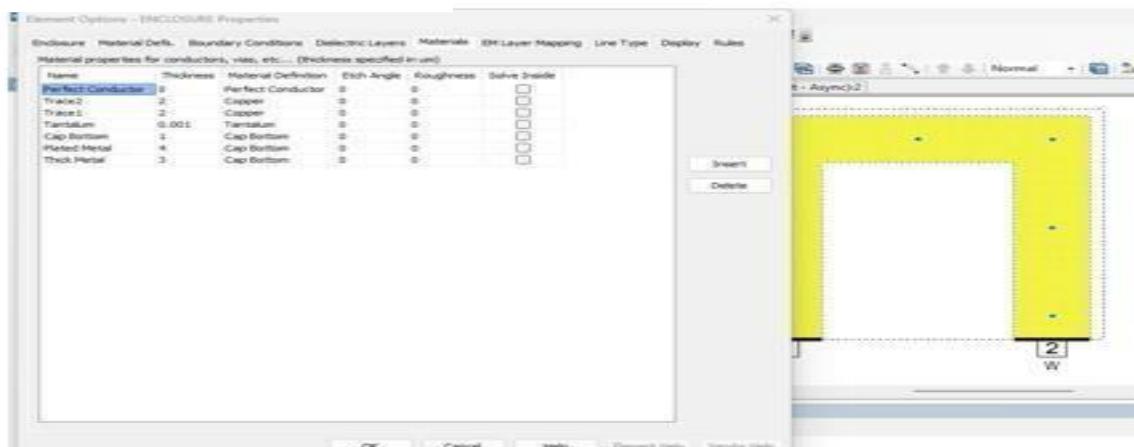


Fig.no.7.1.8.1: Dielectric materials defining of fractal

## 6. Performance Analysis:

After simulating the initial design, the inductance and Q-factor values are analyzed to evaluate the inductor's performance. The results from each iteration provide insight into the impact of path width on the inductor's performance.

## 7. Iteration Process:

The design is refined through multiple iterations by varying the path width. The goal is to select the iteration that provides the best combination of inductance and Q-factor while maintaining the design constraints.

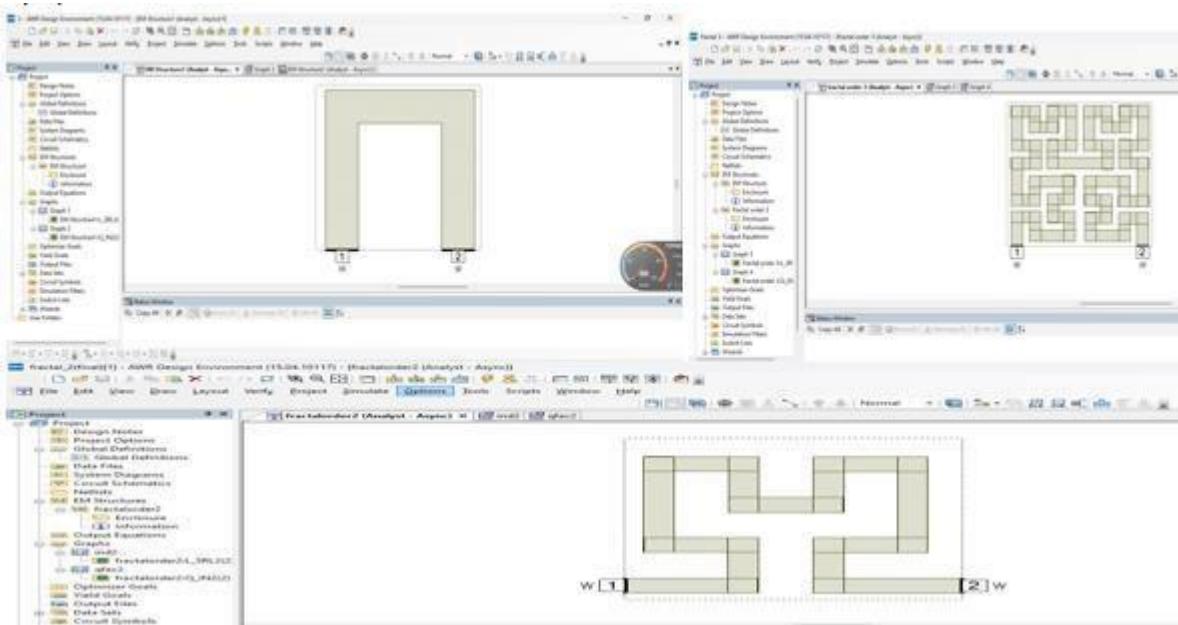


Fig.no.7.1.9.1:Fractal With Different Iterations

## 8. Optimization:

Once the optimal iteration is selected, the design is further optimized to minimize parasitic losses and improve performance at high frequencies.

# CHAPTER 8

## SIMULATION AND RESULTS

The simulation of the Hilbert fractal inductor was conducted using AWR Microwave Office to analyze its performance across multiple design iterations. The primary focus was on optimizing key parameters such as inductance and quality factor (Q-factor) to ensure suitability for high-frequency microwave applications. The results for each iteration are summarized in the table below:

Table No:8.1.1

S.No	Iteration	Path Width ( $\mu\text{m}$ )	Thickness ( $\mu\text{m}$ )	Quality Factor (Q)	Inductance (nH)
1	1	10	2	24.75 (33GHz)	0.6113
2	2	10	2	17.13 (43 GHz)	0.68557
3	3	2	2	8.59 (43.98 GHz)	0.6677
4	3	2.5	2	10.90 (43.98 GHz)	0.6459
5	3	5	2	12.04 (49.98 GHz)	0.1847

### Comparison of Q-factor and Inductance value for various Iterations:

#### 8.1 First Iteration:

In the initial iteration, a path width of 10  $\mu\text{m}$  was used with a thickness of 2  $\mu\text{m}$ . The simulation at 15 GHz yielded an inductance of 0.1343 nH and a Q-factor of 22.75.

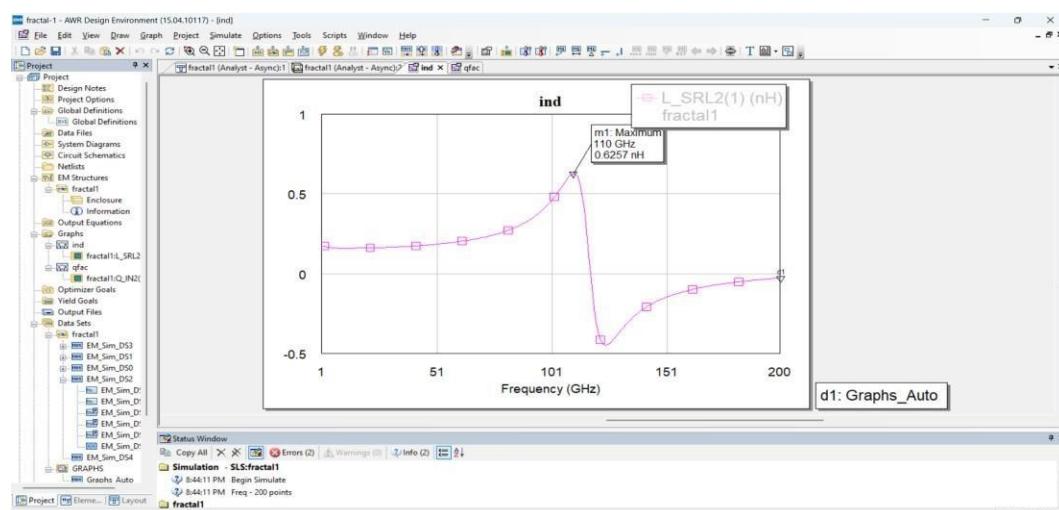


Fig.no.8.1.1.1: Q-Factor vs. Frequency for the First Iteration of 2.5 path width

These values served as the baseline for further optimizations. The higher Q- factor at this frequency highlights the reduced energy loss and improved efficiency of the initial design.

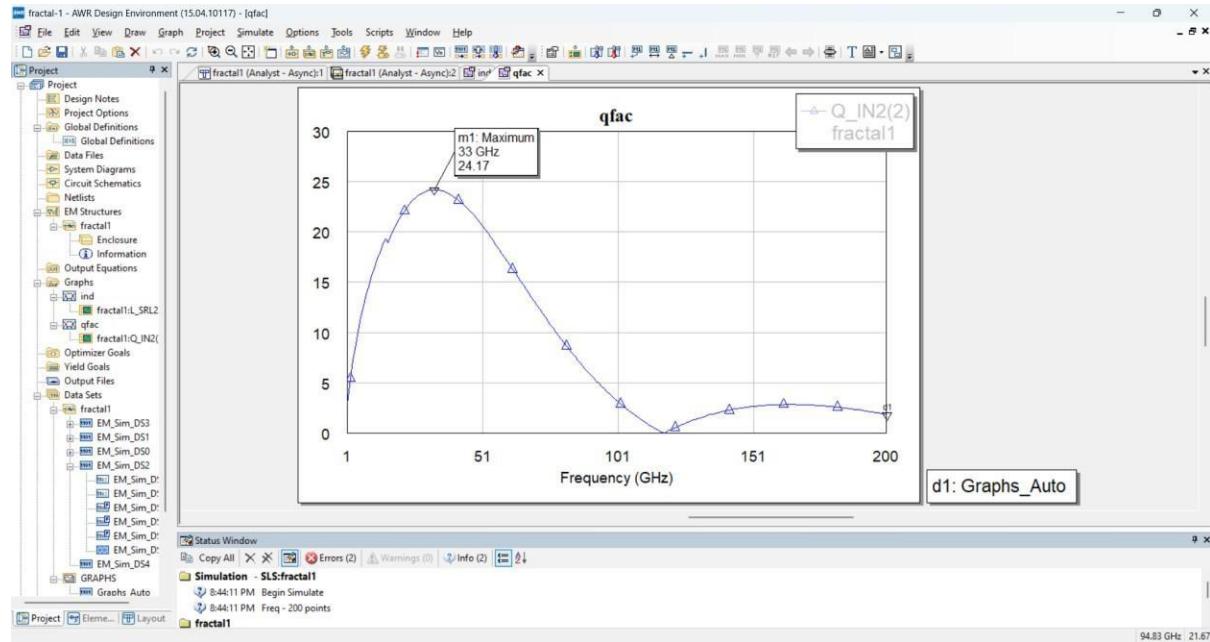


Fig.no.8.1.2.1: Q-Factor vs. Frequency for the first Iteration of 2.5 path width

## 8.2 Second Iteration:

In the second iteration, the path width remained at 10  $\mu\text{m}$ , but the operating frequency was increased to 46 GHz. The resulting inductance dropped slightly to 0.1157 nH, while the Q-factor also decreased to 18.58.

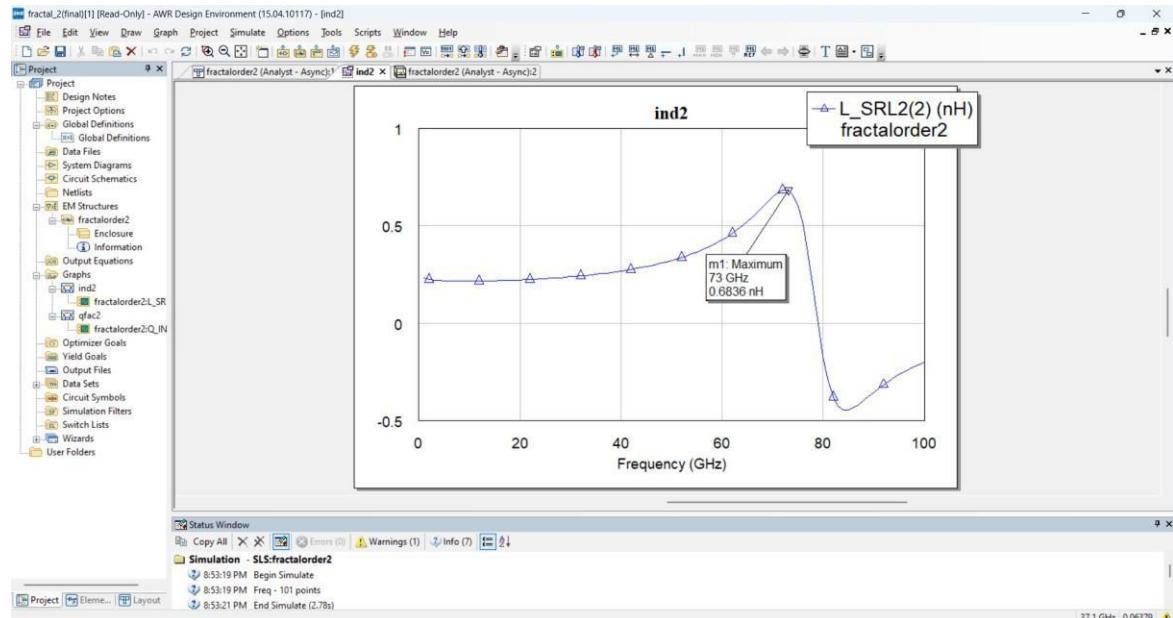


Fig.no.8.1.3.1: Inductance vs. Frequency for the Second Iteration of 2.5 path width

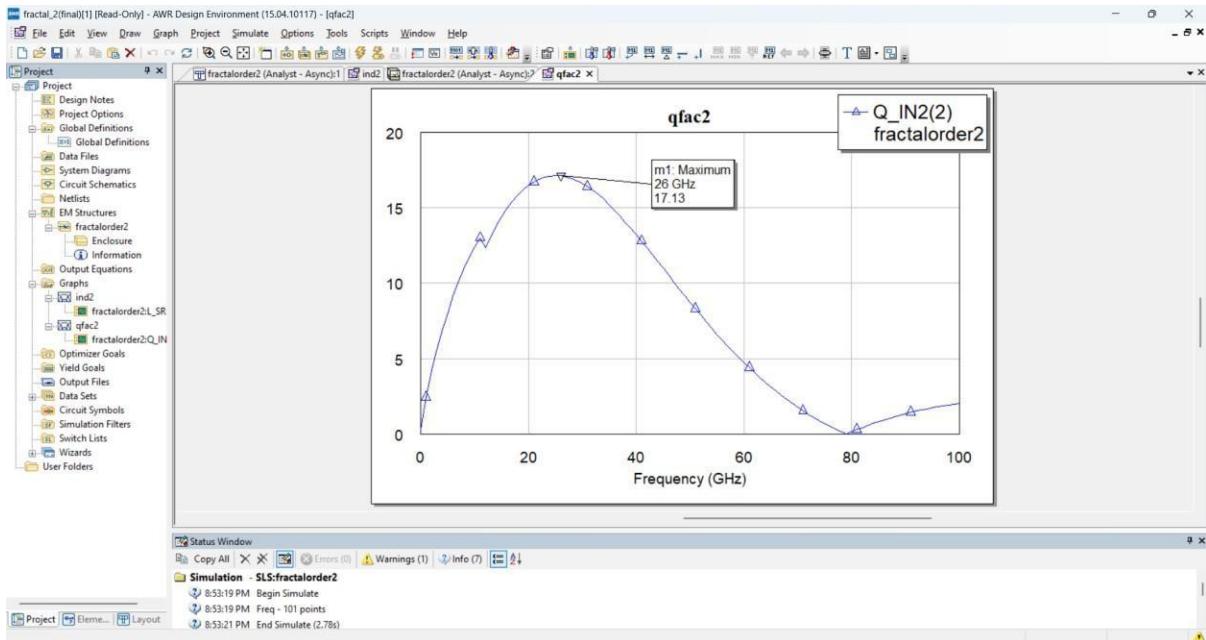


Fig.no. 8.1.4.1: Q-Factor vs. Frequency for the Second Iteration of 2.5 path width

### 8.3 Third Iteration:

The third iteration involved varying the path width to explore its effect on performance. At an operating frequency of 49.98 GHz:

- For a 2  $\mu$ m path width, the inductance increased to 0.2677 nH, while the Q- factor was 10.59.

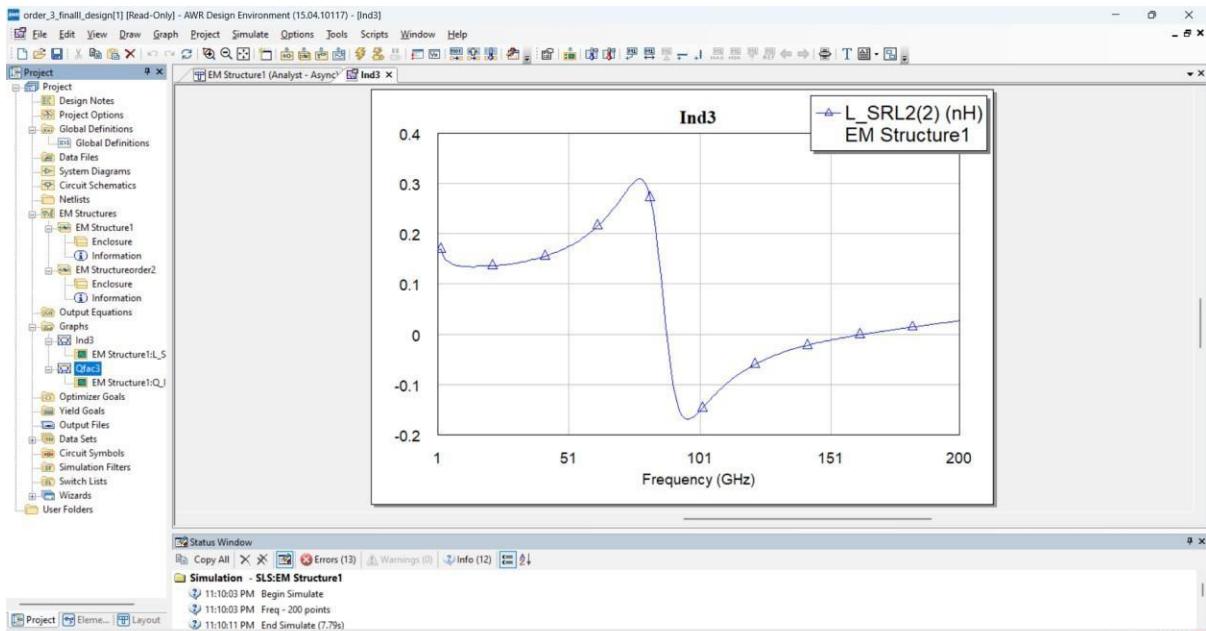


Fig.no.8.1.5.1: Inductance vs. Frequency for the Third Iteration of 2.5 path width

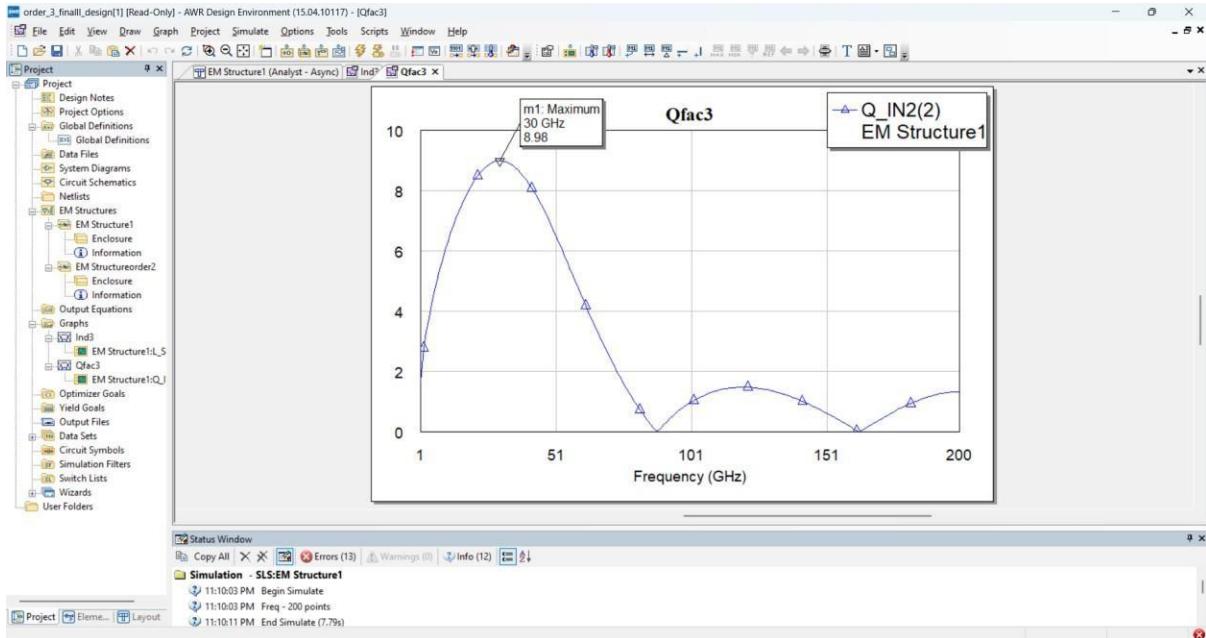


Fig.no.8.1.6.1: Q-Factor vs. Frequency for the Third Iteration of 2.5 path width

These results demonstrate the trade-offs between inductance and Q-factor as the path width varied. Narrower paths yielded higher inductance values but lower Q-factors, while wider paths improved the Q-factor but reduced inductance.

#### 8.4 Analysis:

The simulation results highlight the flexibility of the Hilbert fractal inductor in achieving specific performance goals. The first iteration provided a strong balance at lower frequencies, while the second iteration demonstrated adaptability to higher frequencies with acceptable performance. The third iteration offered a detailed exploration of design parameters, with the 5  $\mu\text{m}$  path width achieving the best Q-factor and overall efficiency at 49.98 GHz.

These findings validate the potential of Hilbert fractal inductors for microwave applications, offering significant advantages over traditional designs. The results from this study will guide the next phase of integrating the inductor into an LNA circuit for further evaluation.

# CHAPTER 9

## LOW NOISE AMPLIFIER

This schematic appears to be a circuit designed in Advanced Design System (ADS), a software tool used for RF, microwave, and high-speed digital circuit design.

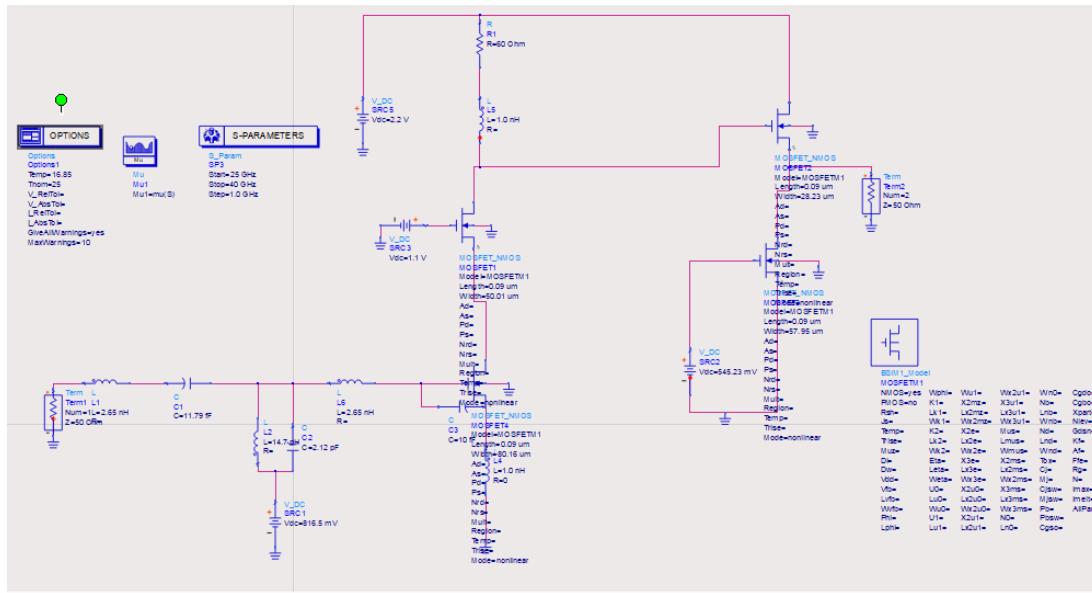


Fig No: :9.1.1.2 Low Noise Amplifier

### 9.1 Resistors:

Resistors in this circuit play a crucial role in controlling current flow, setting biasing conditions, and defining the gain of active components like MOSFETs. The schematic includes R<sub>1</sub> (80Ω), which is likely used as a load resistor, ensuring that the transistors operate within their designed parameters. Resistors like this help stabilize the voltage and current levels, preventing fluctuations that could degrade the circuit's performance. In RF applications, resistors also contribute to impedance matching and controlling the overall power dissipation.

### 9.1.1 Capacitors:

Capacitors serve multiple functions in this circuit, including coupling, decoupling, and impedance matching. C<sub>1</sub> (1.79 fF) is likely a coupling capacitor, allowing AC signals to pass while blocking DC components, preventing unwanted voltage shifts between stages. C<sub>2</sub> (2.12 pF) is part of an LC network, working alongside inductors to tune the circuit's resonant frequency and optimize signal transmission. C<sub>3</sub> (10 fF) functions as a decoupling capacitor, stabilizing voltage levels by filtering out unwanted noise and preventing fluctuations from affecting the active components. These capacitors collectively ensure the circuit's stability and

efficient signal transfer.

### **9.1.2 MOSFET Transistors:-**

The circuit contains multiple MOSFET transistors that are used for amplification and signal processing. MOSFET1 (50.09  $\mu\text{m}$  width) likely functions as the primary RF amplifier, boosting weak signals while maintaining linearity. MOSFET2 (546.12  $\mu\text{m}$  width) is significantly larger, suggesting it is designed for high-power amplification, capable of handling larger signal swings. MOSFET3 (28.23  $\mu\text{m}$  width) acts as a buffer stage, ensuring signal integrity as it transitions through different stages.

The presence of a BSIM1 Model MOSFETM1 indicates that this circuit has been optimized for accurate high-frequency performance, taking into account real-world device characteristics during simulation.

### **9.1.3 Voltage Sources:**

Several DC voltage sources provide power and biasing to the transistors. V\_DC (SRC1, 1.1V) ensures the MOSFETs operate in their intended region, maintaining stable amplification. V\_DC (SRC2, 2.2V) supplies additional power, possibly for different amplification stages. V\_DC (SRC4, 816.5 mV) suggests a negative biasing mechanism, which can be used to improve transistor stability and reduce distortion in the circuit. Proper biasing is crucial in RF circuits to ensure the correct functioning of active components and prevent unwanted oscillations.

### **9.1.4 Termination Components:**

To ensure proper signal transmission and impedance matching, the circuit includes  $50\Omega$  terminations (TermG1 and TermG2). These components are essential in high-frequency designs to prevent signal reflections, which can degrade circuit performance. Proper termination ensures maximum power transfer and minimizes signal degradation, making it a key consideration in RF and microwave applications.

### **9.1.5 Simulation Parameters (S-Parameters & Options Block):**

To analyze the circuit's behavior at high frequencies, an S-parameter simulation block is included, covering a frequency range of 0.1 GHz to 30 GHz with a 1.0 MHz step size. S-parameters are used to evaluate how signals are transmitted, reflected, and amplified across different frequencies, making them essential for RF circuit design. The Options block defines key simulation parameters, including temperature ( $16.85^\circ\text{C}$ ) and reference voltage settings,

## **9.2 SIMULATION RESULTS:**

To simulate the circuit successfully, we need to follow a structured approach. First, we set up the circuit in the simulation tool, ensuring all components, connections, and biasing conditions are correctly defined. Next, we configure the simulation parameters, including S-parameter analysis, noise figure calculation, and stability factor evaluation over the desired frequency range.

After running the simulation, we analyze the results, focusing on key parameters such as gain ( $S_{21}$ ), input reflection ( $S_{11}$ ), and stability ( $M_u$ ) to assess performance. Finally, based on the results, we optimize the design by adjusting component values, biasing, or impedance matching networks to improve efficiency.

### **9.2.1 Setup the Circuit:**

Ensure that all components (MOSFETs, resistors, capacitors, inductors, voltage sources, and terminations) are correctly placed and connected as per the schematic. Double-check the biasing voltages to avoid incorrect transistor operation.

### **1 Configure the Simulation Parameters:**

- a. Use S-Parameter analysis to evaluate circuit behavior from 0.1 GHz to 30 GHz with a 1 MHz step size.
- b. Enable DC analysis to verify the biasing conditions of MOSFETs.
- c. Use Transient analysis to study time-domain response if required.

### **2 Run the Simulation:**

Execute the simulation and analyze the S-parameters ( $S_{11}$ ,  $S_{21}$ ,  $S_{12}$ ,  $S_{22}$ ) to check the circuit's gain, reflection coefficient, and transmission efficiency. Observe voltage and current waveforms to confirm expected performance.

### **3 Interpret the Results:**

- a.  $S_{21}$  (Gain): Should be positive, indicating amplification.
- b.  $S_{11}$ ,  $S_{22}$  (Reflections): Should be minimal for proper impedance matching.

c. Power Dissipation: Ensure the MOSFETs operate within their limits. Networks using inductors and capacitors can reduce reflections and enhance power transfer, improving overall circuit performance.

The simulation results from Advanced Design System (ADS) for an RF circuit, likely an amplifier, analyzed using S-parameters, noise figure, and stability factor across a frequency range of 25 GHz to 30 GHz.

### **9.2.2 (S11 - Input Reflection Coefficient):**

This graph represents dB(S11), which indicates the input return loss or how much of the input signal is reflected instead of being transmitted into the circuit. A lower return loss (more negative dB value) means better impedance matching, while a higher return loss suggests poor matching. At 28.46 GHz, the return loss is -1.368 dB, indicating a moderate amount of signal is being reflected.

This suggests that the circuit's input impedance is not perfectly matched to the source impedance, causing some power loss. Proper impedance matching techniques, such as adjusting component values or adding matching networks, could help reduce reflections and improve power transfer efficiency.

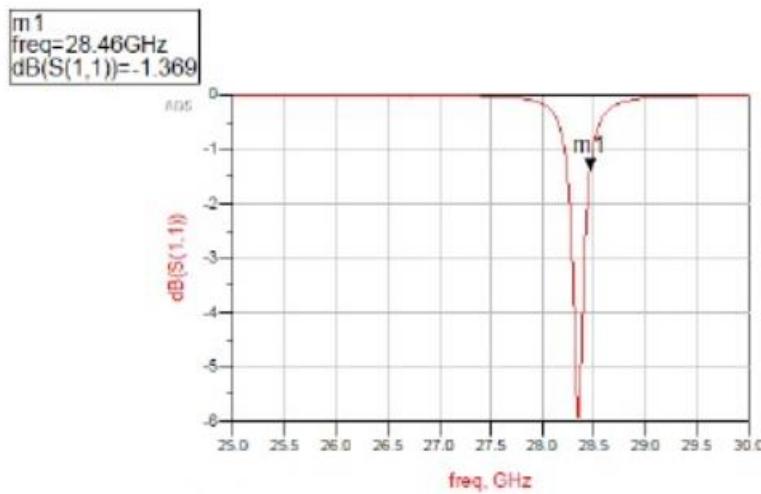


Fig no: 9.2.1.1 Impedance Matching

### **9.2.3 (Noise Figure - NF):**

This plot shows the noise figure (NF) in dB, which quantifies how much additional noise the circuit introduces compared to an ideal noiseless system. A lower noise figure is desirable, as it ensures better signal-to-noise ratio (SNR) and overall circuit performance. In this simulation,

at 28.54 GHz, the NF is 7.721 dB, which is relatively high.

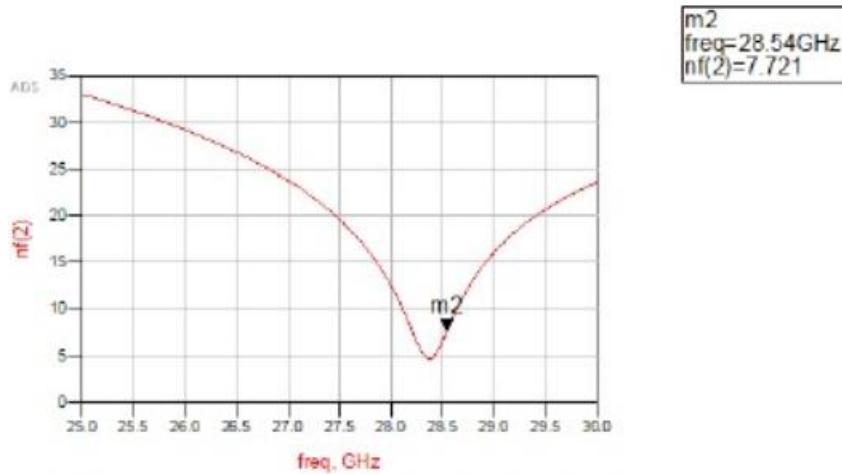


Fig no: 9.2.1.2 Noise figure

The plot displays the noise figure (NF) versus frequency response of a circuit, likely a low noise amplifier (LNA) or similar RF front-end component. The **x-axis represents frequency (in GHz)** ranging from **25 to 30 GHz**, and the **y-axis shows the noise figure in dB**. A distinct dip in the curve indicates the frequency at which the system exhibits **minimum noise**, which is a critical parameter for optimizing receiver sensitivity in communication systems.

From the graph, the **minimum noise figure is marked at point m2**, which occurs at **28.54 GHz** with an NF value of **7.721 dB**. This frequency is likely the **design frequency or center frequency** of the component, suggesting optimal performance at this point. The symmetrical nature of the curve around the dip suggests a well-tuned design targeting operation near 28.5 GHz, possibly for **5G or millimeter-wave applications**.

Overall, this plot is a valuable tool for designers to **evaluate the noise performance** of RF systems across a frequency band. A low and narrow noise figure curve implies **good selectivity and efficiency**, while deviations or high values would necessitate further circuit tuning. This analysis is crucial in ensuring **low signal distortion and high sensitivity**, especially in advanced communication systems operating at high frequencies.

Graphs play a vital role in analyzing the performance of a Low Noise Amplifier (LNA), offering visual insight into key parameters like noise figure, stability, and gain across various frequencies. The **Noise Figure (NF) vs Frequency** graph helps identify the frequency at which

the LNA introduces the least amount of noise, .

#### 9.2.4 (S21 - Gain of the Amplifier):

This graph represents dB(S21), the gain of the amplifier, which is a critical factor in determining the effectiveness of signal amplification. A higher gain means the amplifier effectively boosts the input signal, making it useful for RF and microwave applications. However, in this circuit, the peak gain occurs at 28.51 GHz, but the value is only -2.783 dB, meaning the circuit is not amplifying the signal as expected.

Instead, it is introducing losses. Furthermore, at 29.84 GHz, the gain drops further to -19.997 dB, which means the circuit is significantly attenuating the signal instead of amplifying it. This behavior suggests that the design needs optimization, possibly through adjusting biasing conditions, modifying the transistor width/length ratio, or improving impedance matching to achieve proper amplification.

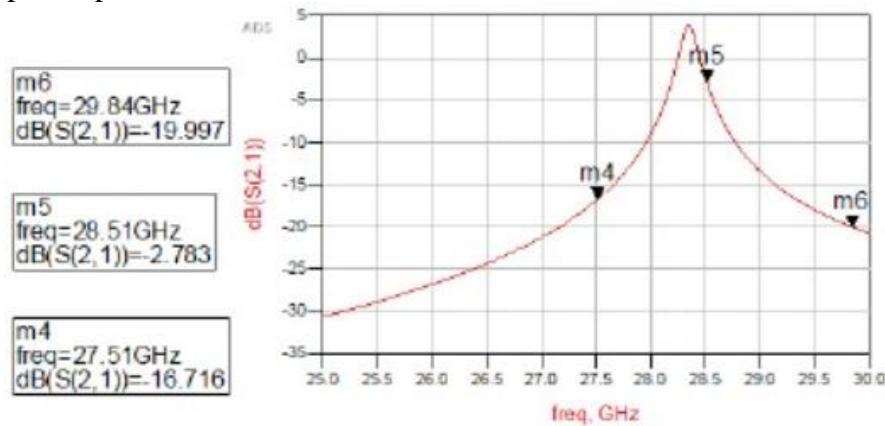


Fig no: 9.2.3.1 Gain

#### 9.2.5 (Stability Factor - Mu):

The stability factor ( $\mu$ ) determines whether the amplifier is unconditionally stable, meaning it will not oscillate or become unstable under any operating conditions. For an amplifier to be stable,  $\mu$  should always be greater than 1. At 28 GHz, the stability factor is 5.162, which is well above 1, confirming that the circuit is stable at this frequency.

This suggests that the amplifier will operate without unwanted oscillations, making it reliable for practical applications. However, stability should be checked across the entire frequency range of interest, as variations in transistor parameters and parasitics can lead to instability at different frequencies. Further improvements in stability can be made by adding feedback networks or using stabilization techniques such as resistive loading.

These are the results obtained for a normal inductor, which serves as a baseline for analyzing the circuit's performance under standard conditions. The normal inductor provides a certain

level of inductance, but it also introduces parasitic effects such as resistance and capacitance, which can impact the circuit's efficiency at high frequencies.

implementing a fractal inductor, we aim to observe improvements in key performance metrics such as gain (S21), input reflection (S11), output reflection (S22), noise figure (NF), and stability factor ( $\mu$ ).

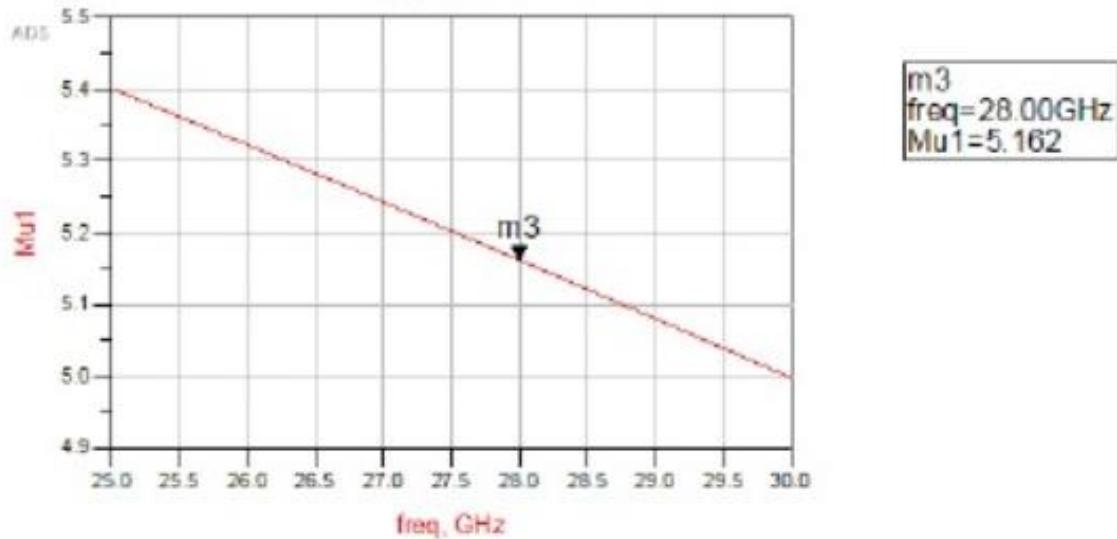


Fig no: 9.2.4.1 Stability Factor

Once the fractal inductor is incorporated, we will run a new set of simulations to compare its impact on circuit performance. The objective is to determine whether the fractal inductor reduces signal losses, enhances power transfer, and minimizes unwanted noise in the circuit. Since fractal inductors offer a higher inductance density, they may help in achieving better frequency response and improved efficiency.

The plot shows the **Mu stability factor ( $\mu$ 1)** on the y-axis and frequency (in GHz) on the x-axis, indicating how stable the circuit is across the specified frequency range. The Mu factor is a key parameter in amplifier design and must be **greater than 1** to ensure unconditional stability. In this graph, the curve gently slopes downward as frequency increases, but it consistently stays above 4.9, demonstrating that the design remains stable throughout the entire range.

At the marked point **m3**, which corresponds to **28.00 GHz**, the Mu value is **5.162**. This value is well above the critical threshold of 1, confirming that the circuit is **unconditionally stable** at the desired operating frequency. This is essential in practical high-frequency systems, especially in applications like **5G** and **millimeter-wave communications**, where component stability ensures predictable and reliable performance.

Additionally, the changes in stability factor ( $M_u$ ) will be examined to ensure the circuit remains unconditionally stable after the modification. A detailed comparison between the normal and fractal inductor designs will help in identifying the most effective configuration for optimizing performance in high-frequency applications.

### **9.3 Design of the Fractal Inductor in ADS Tool:**

The design of the fractal inductor in Advanced Design System (ADS) involves creating a self-similar, space-efficient inductor structure to enhance inductance and minimize losses. Using the layout editor in ADS, we will define the fractal geometry, ensuring proper scaling and symmetry for high-frequency applications. The design parameters, such as trace width, spacing, and number of fractal iterations, will be carefully adjusted to achieve optimal performance. Once the layout is completed, electromagnetic (EM) simulations will be performed to analyze the inductance value, quality factor (Q), and impedance characteristics. The goal is to compare the fractal inductor's efficiency against a conventional inductor to determine its advantages in RF circuit applications.

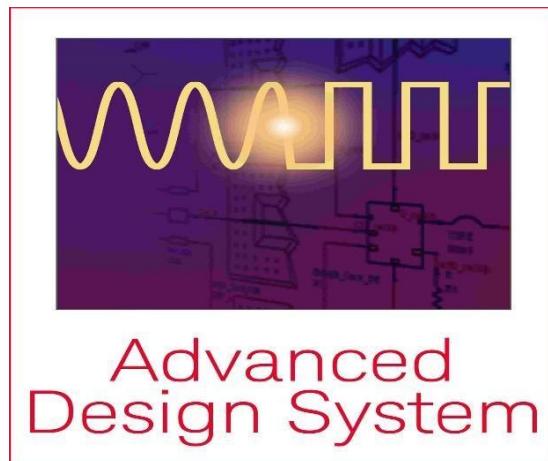


Fig no: 9.3.1 tool used for lna design

#### **1 Steps to integrate the fractal in LNA:**

- Open the ADS layout Editor and design the fractal inductor.
- Convert the fractal layout into a component.
- Import the fractal inductor into the LNA schematic.
- Adjust matching.

## 2 Creation of Workspace:

In ADS, creating a workspace is the first step to designing the fractal inductor, allowing proper organization of schematics, layouts, and simulations. This involves setting up a new project directory and defining key parameters like frequency range and substrate properties for accurate analysis. A structured workspace ensures efficient design and optimization.

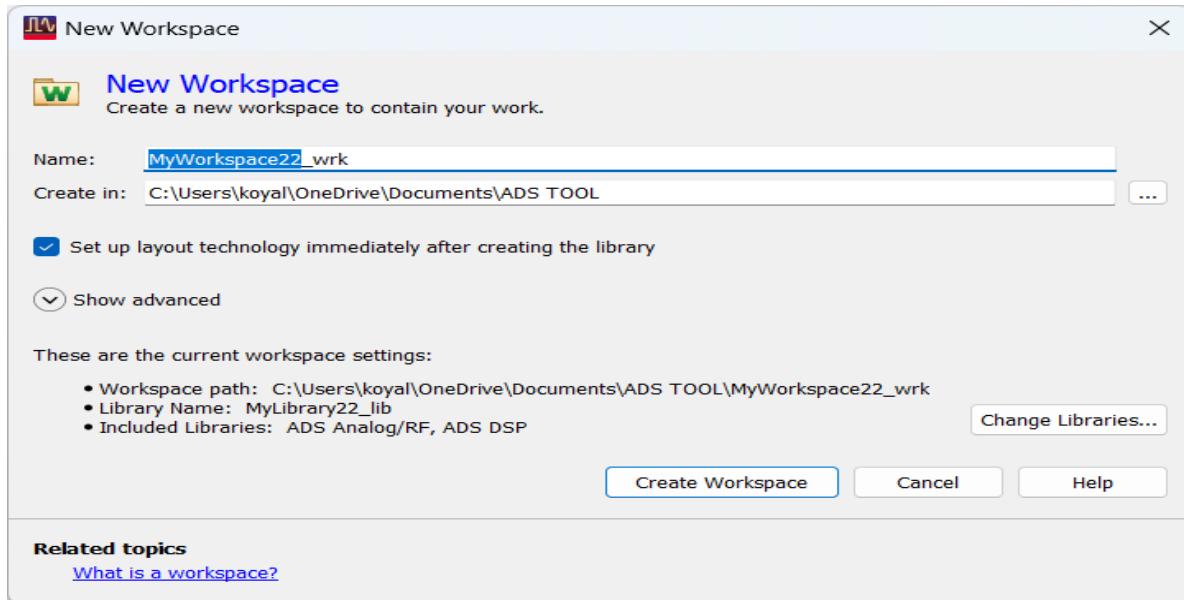


Fig no:9.3.2.1 workspace creation in ads tool

## 3 Layout Creation:

In ADS, layout creation involves designing the physical structure of the fractal inductor by defining its shape, trace width, and spacing. Using the layout editor, we accurately place and connect the inductor elements while considering high-frequency performance.

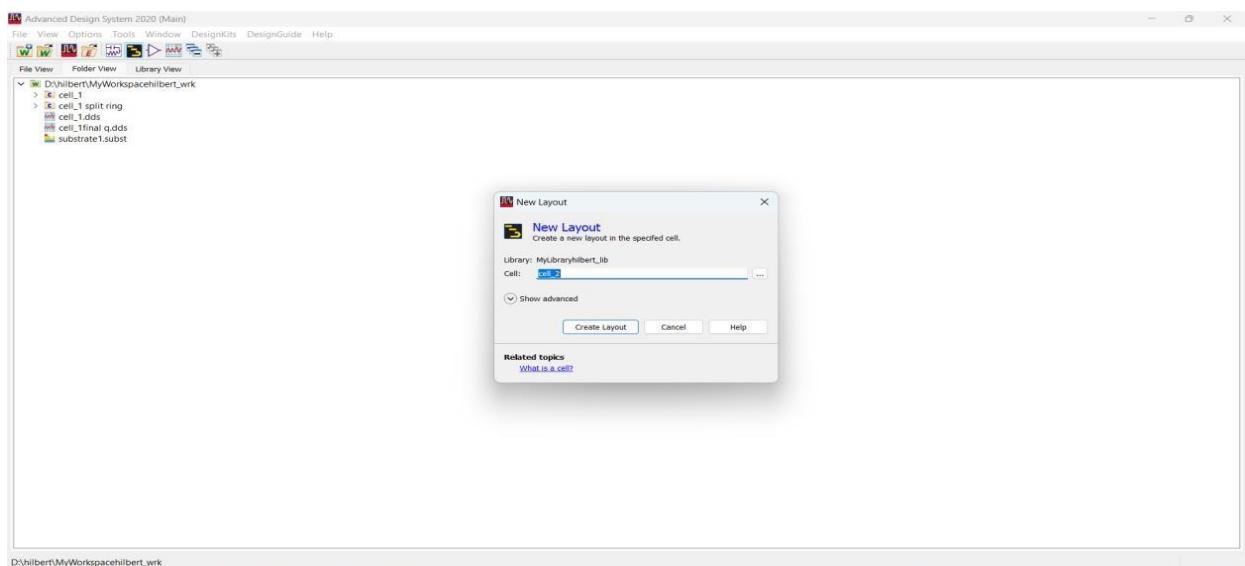


Fig no:9.3.2.1 layout design in ads tool

## 4 Layout Technology:

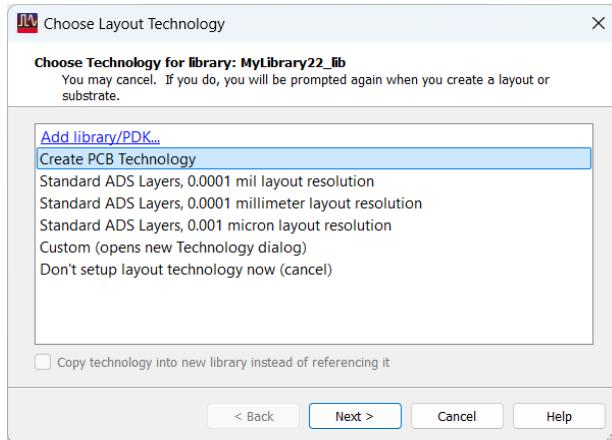


Fig no: 9.3.3.1 creating pcb technology

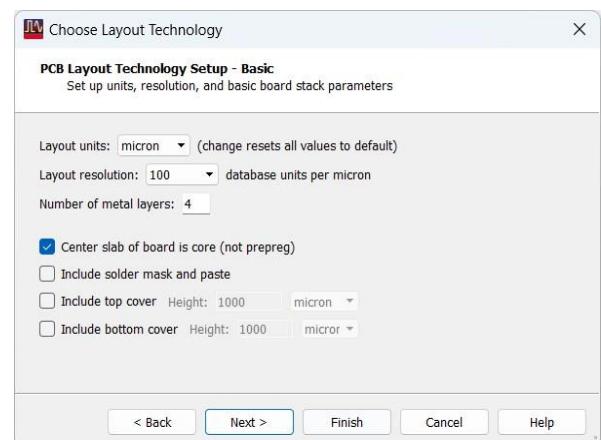


Fig no9.3.3.2 considering area

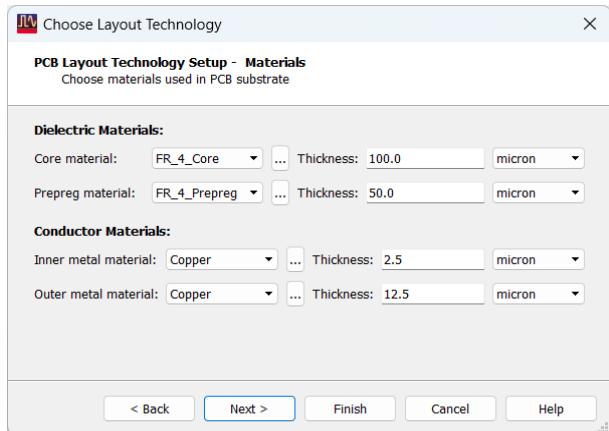


Fig no: 9.3.3.3 choosing layout techhnology

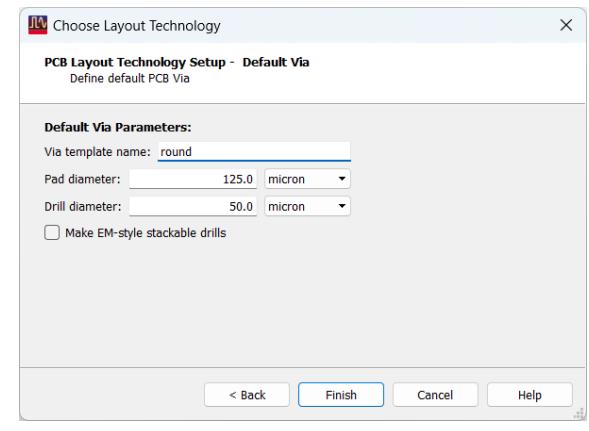


Fig no: 9.3.3.4 default via settings

## 5 ADS TOOL WINDOW:

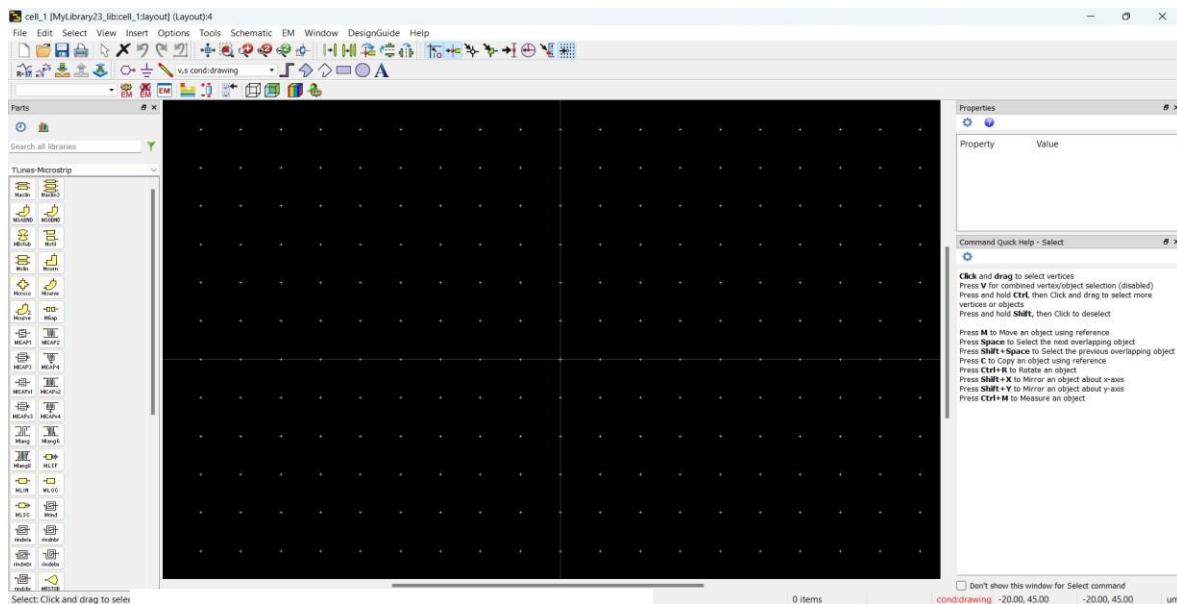


Fig no:9.3.3.5 ads tool window

Design of the fractal inductor in ADS by carefully defining the path structure, ensuring optimal inductance and minimal losses. The path is created using the layout editor, where parameters like trace width, spacing, and number of iterations are adjusted for high-frequency performance. Proper path design helps in reducing parasitic effects and improving the overall efficiency of the inductor.

## 9.4 DESIGN OF FRCTAL INDUCTOR:

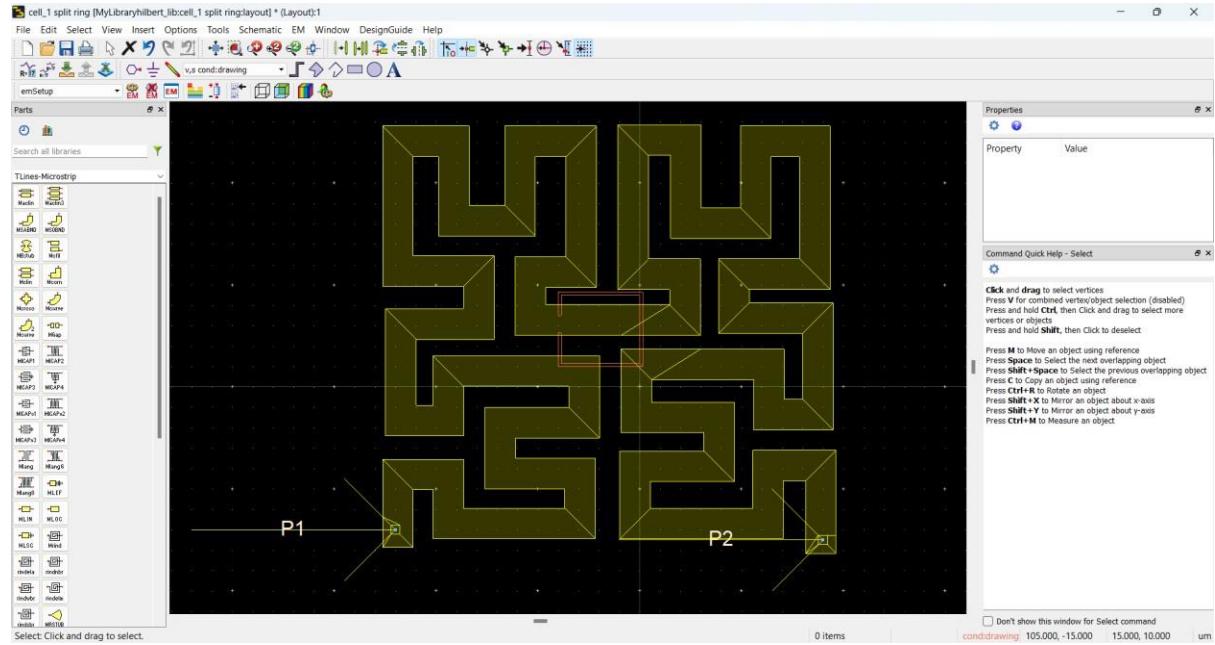


Fig no: 9.4.1.1 design of fractal inductor

The above design represents a 3-turn fractal inductor, created using a self-similar geometric structure to enhance inductance and high-frequency performance. This design helps in reducing the overall footprint while maintaining efficient signal transmission by minimizing parasitic effects and losses. The fractal structure improves the Q-factor and impedance matching, making it ideal for RF and microwave applications.

### 9.4.1 PORTS ASSIGNMENT:

In ADS, port assignment is a crucial step in setting up simulations for the fractal inductor design. Ports serve as input and output terminals, allowing the software to analyze parameters such as S-parameters, impedance, and inductance characteristics. Typically, two ports are assigned: one at the signal input and the other at the signal output, ensuring proper excitation and measurement of circuit behavior. The placement of ports must be carefully chosen to match the real-world implementation and minimize undesired parasitic effects.

## 9.4.2 EM SETTINGS:

In Advanced Design System (ADS), setting up an Electromagnetic (EM) simulation is essential for accurately analyzing the performance, losses, and impedance characteristics of a fractal inductor. The Momentum EM solver is typically used for planar structures, providing precise results for high-frequency applications. To begin, the substrate properties must be defined correctly, including parameters such as dielectric constant, thickness, and conductor type, which directly impact the inductor's behavior. Proper material selection ensures minimal resistive and dielectric losses.

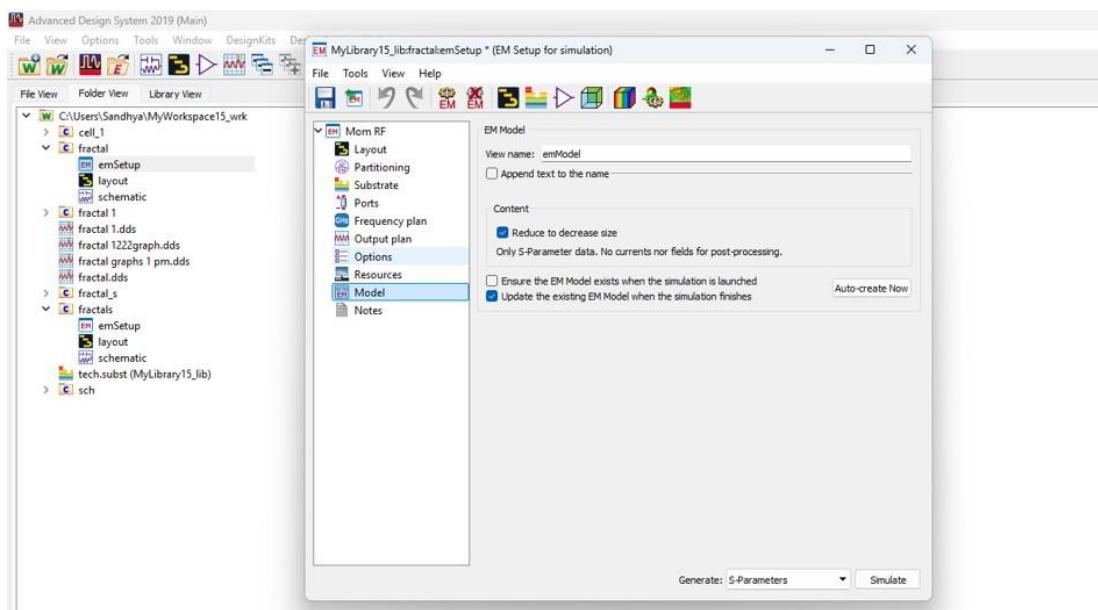


Fig no: 9.4.2.1 em settings in ads tool for every design

The next step is to configure the simulation domain and mesh refinement to accommodate the intricate fractal geometry. A denser mesh is required for highly detailed structures like a Hilbert fractal inductor to ensure accuracy while balancing computational efficiency.

Boundary conditions should be set appropriately to prevent unwanted reflections that could distort results. The frequency range must be chosen based on the target application, ensuring a comprehensive analysis of key parameters such as S-parameters, impedance ( $Z$ ), and quality factor ( $Q$ ).

Additionally, port assignment plays a vital role in capturing the inductor's response. The inductor can be tested using single-ended or differential ports, depending on the application. Correct placement of ports ensures proper excitation and measurement of the inductor's behavior.

## CHAPTER 10

### ROLE OF THE INDUCTOR IN LNA

In a Low Noise Amplifier (LNA), the inductor plays a crucial role in impedance matching and signal amplification. One of the primary uses of an inductor in an LNA is to resonate with the parasitic capacitance at the input, forming a tuned circuit that maximizes the voltage gain at a specific frequency. This resonance enhances signal strength while maintaining a low noise figure, which is essential for sensitive receiver applications like wireless communication systems. In a Low Noise Amplifier (LNA), inductors play a crucial role in achieving high performance, especially in RF and microwave frequency applications. One of their primary functions is in **impedance matching** at both the input and output. Proper matching ensures maximum power transfer and helps in reducing signal reflection, which is vital for maintaining signal integrity and minimizing losses. Inductors are used in LC matching networks to adjust the impedance seen by the transistor, which also contributes to lowering the overall noise figure of the amplifier.

Another important role of the inductor in LNA design is in source degeneration and load tuning. Source degeneration inductors are used to improve the linearity and stability of the amplifier by providing negative feedback. At the same time, inductors in the load section are used to form part of the output matching network, ensuring maximum power transfer to the next stage. These inductors help control the gain-bandwidth trade-off and allow the amplifier to operate efficiently over the desired frequency range.

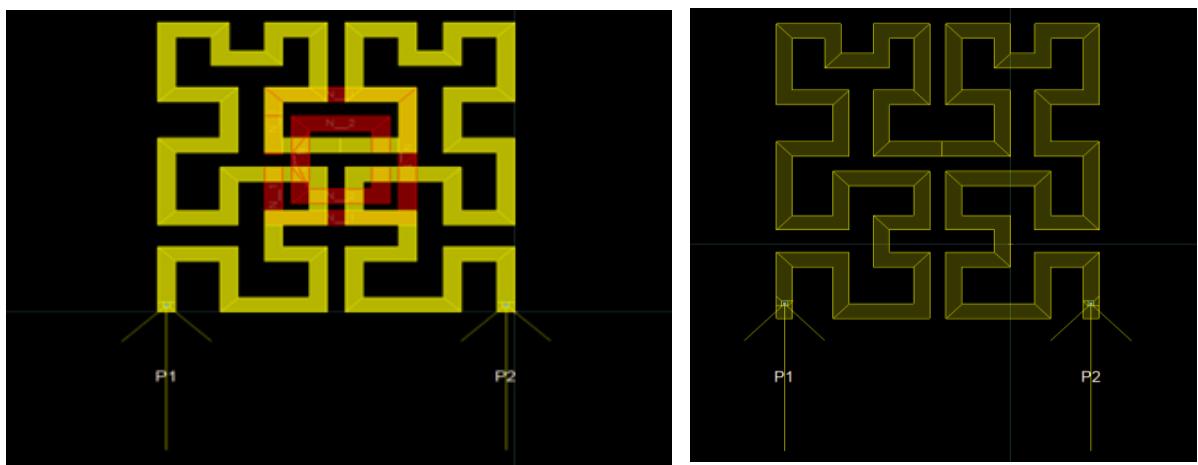


Fig No:10.1 Hilbert inductors with and without csrr.

## **10.1 HILBERT FRACTAL INDUCTOR WITH COMPLEMENTARY SPLIT RING RESONATOR(CSRR):**

A Complementary Split Ring Resonator (CSRR) is a type of metamaterial structure that exhibits unique electromagnetic properties not found in natural materials. It is widely used in microwave engineering, antenna design, and RF/microwave circuits for applications like filtering, sensing, and miniaturization. Below is a detailed breakdown of what a CSRR is, how it works, and its applications.

### **Use of CSRR in Fractal Inductor:**

#### **◆ 1. Enhancement of Quality Factor (Q-Factor):**

- CSRR introduces a sharp resonance at a specific frequency, improving the selectivity and energy storage ability of the inductor.
- The high-Q resonance of the CSRR reduces energy loss, which enhances the overall Q-factor of the fractal inductor.
- This is particularly beneficial at high frequencies (mmWave) where losses are more critical.

#### **◆ 2. Inductance Control and Tuning:**

- Embedding CSRRs in or near fractal inductors allows tuning of the effective inductance.
- The CSRR acts as a resonant load, adding a distributed inductance and capacitance, which can modify the overall inductive behavior.
- This tuning capability helps in miniaturizing the inductor while maintaining the desired inductive performance.

#### **◆ 3. Suppression of Parasitics:**

- Fractal inductors inherently have some parasitic capacitance due to their geometry.
- The CSRR's stopband characteristics help suppress unwanted parasitic resonances, leading to cleaner frequency response.

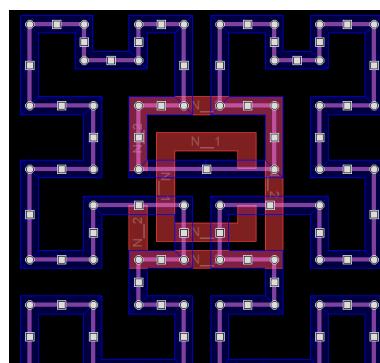


Fig no:10.1.1Hilbert Fractal inductor with comlementary split ring resonator

## 10.2 FRACTAL INDUCTOR WITH CSRR:

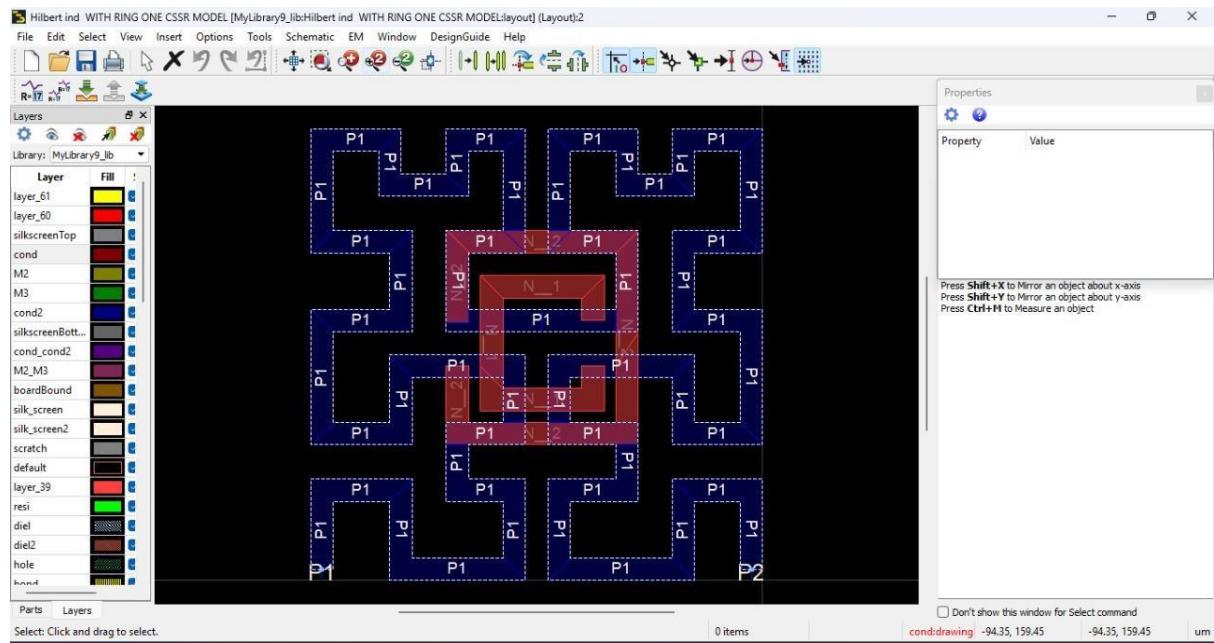


Fig no: 10. 2.1 Hilbert fractal inductor with csrr.

A fractal inductor with a CSRR combines the compact, high-inductance design of a Hilbert fractal geometry with the resonant filtering properties of a Complementary Split Ring Resonator. This integration enhances the Q-factor, enables tunable inductance, and provides better frequency selectivity. It is especially useful in compact and high-performance RF circuits, such as LNAs for 5G applications.

## 10.3 3D VIEW OF FRACTAL INDUCTOR WITH CSRR:

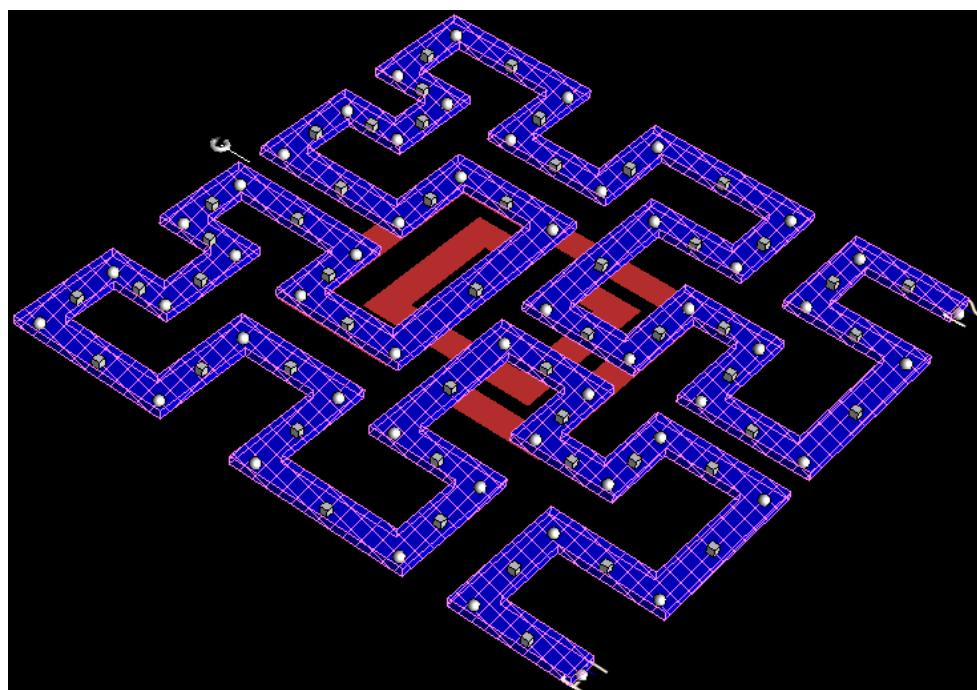


Fig no:10.2.2 3-D view of Hilbert fractal inductor with csrr.

## 10.4 SUBSTRATE SETTINGS OF CSRR MODEL :

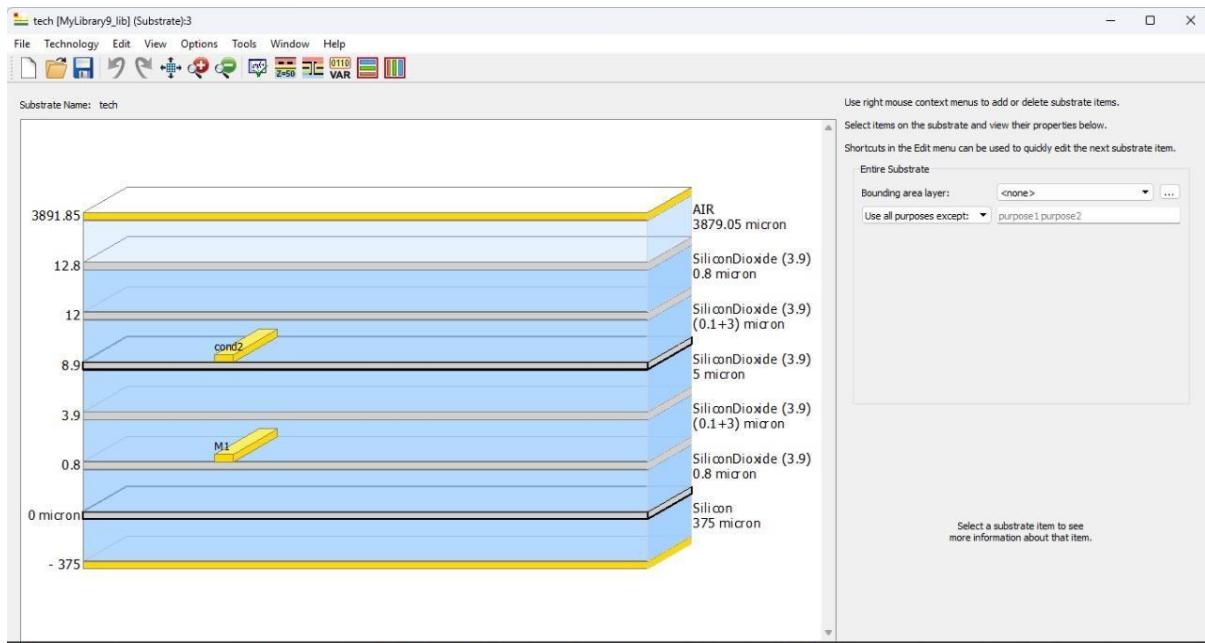


Fig no:10.4.1 substrate of Hilbert fractal inductor with csrr.

### Air (3879.05 $\mu\text{m}$ )

- Topmost layer for EM wave propagation in simulations.
- Acts as free space with dielectric constant  $\epsilon_r = 1$ .

### □ Silicon Dioxide (0.8 $\mu\text{m}$ )

- Thin insulation/passivation layer above the upper metal.
- Provides dielectric isolation from the air.

### □ Silicon Dioxide (0.1 + 3 $\mu\text{m}$ )

- Layer separating upper conductor (cond2) from other levels.
- Offers dielectric spacing and reduces coupling.

### □ Silicon Dioxide (5 $\mu\text{m}$ )

- Bulk dielectric layer ensuring RF isolation.
- Helps in minimizing substrate coupling and loss.

### □ Silicon Dioxide (0.1 + 3 $\mu\text{m}$ )

- Additional dielectric separation below the main metal level.
- Supports signal integrity and layer stacking.

### □ Silicon Dioxide (0.8 $\mu\text{m}$ )

- Buffer layer between substrate and metal layer M1.
- Reduces parasitic capacitance to the silicon.

□ **Silicon (375  $\mu\text{m}$ )**

- Main substrate base providing mechanical support.
- May cause losses unless high-resistivity silicon is used.

## 10.5 SIMULATION RESULTS OF CSRR MODEL HILBERT INDUCTOR:

### 1 Inductance:

This graph shows the Effective Inductance ( $L_{\text{eff}}$ ) of a component, most likely a fractal or planar inductor, as a function of frequency ranging from 0 to 100 GHz. At 19.53 GHz, the inductance is approximately  $6.596 \times 10^{-10} \text{ H}$  (or 659.6 pH), as marked by the point m2. The inductance remains relatively stable at lower frequencies but shows sharp fluctuations around 50–60 GHz, indicating possible self-resonance or parasitic effects. This behavior is critical in RF design because beyond the self-resonant frequency, the inductor no longer behaves as a pure inductive element and may degrade circuit performance. Understanding this trend helps ensure the inductor operates effectively within the desired frequency band.

The graph shows the effective inductance ( $L_{\text{eff}}$ ) of a component versus frequency, measured using ADS (Advanced Design System). At a frequency of 19.53 GHz, the effective inductance is approximately 659.6 pH, indicating typical inductor behavior. However, around 40–50 GHz, the inductance sharply increases and then drops, showing a resonance peak followed by a negative inductance region, which is a sign of self-resonance.

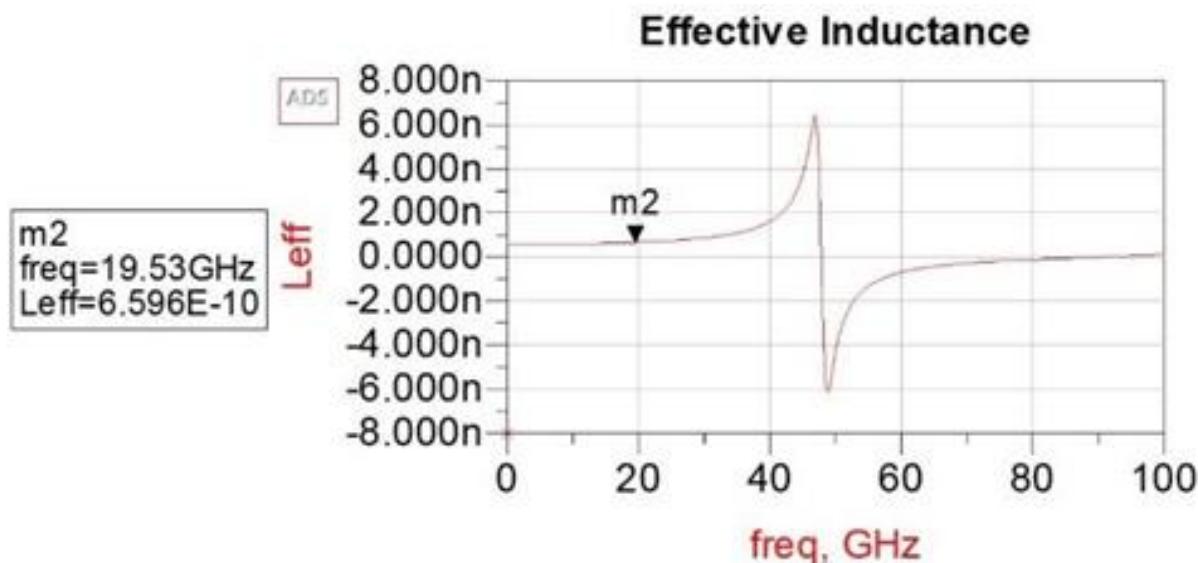


Fig No: 10.5.1 inductance vfreq graph of with csrr model

## 2 Quality Factor:

The graph illustrates the variation of the Quality Factor (Q) with frequency for an inductor used in the design. The peak Q value of 16.992 is observed at 19.01 GHz, indicating the frequency .

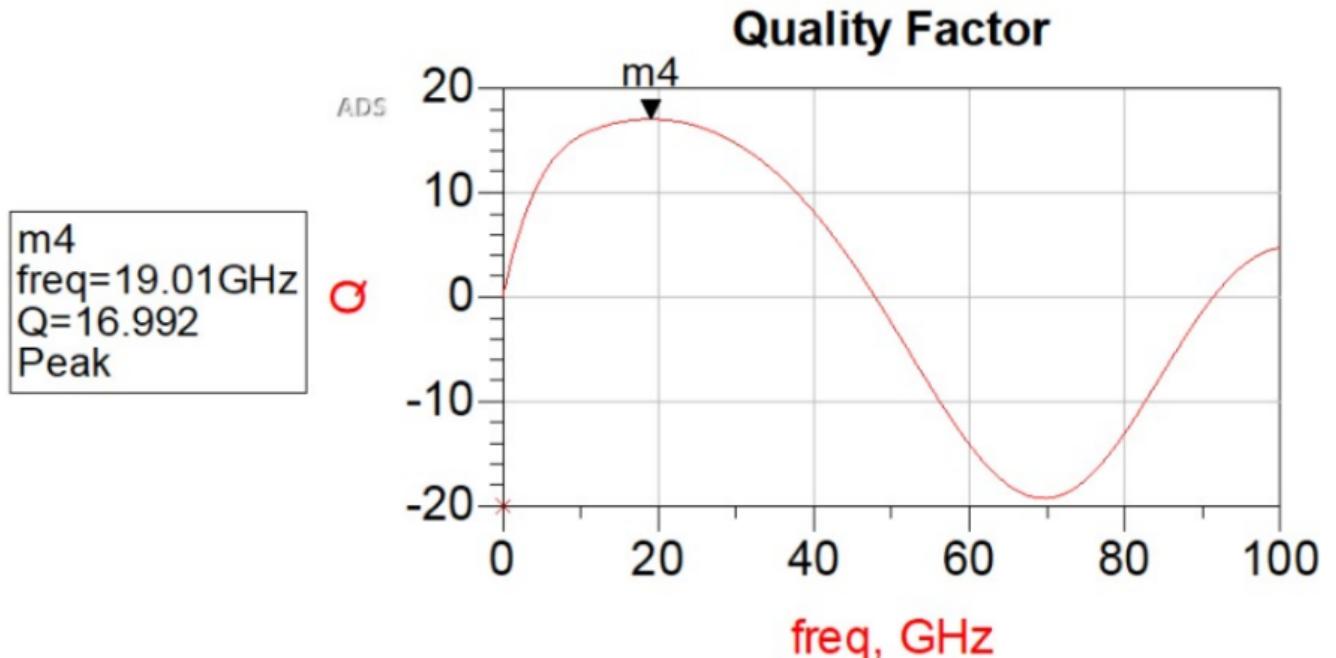


Fig No: 10.5.2 Q-factor vs freq graph of with csrr model

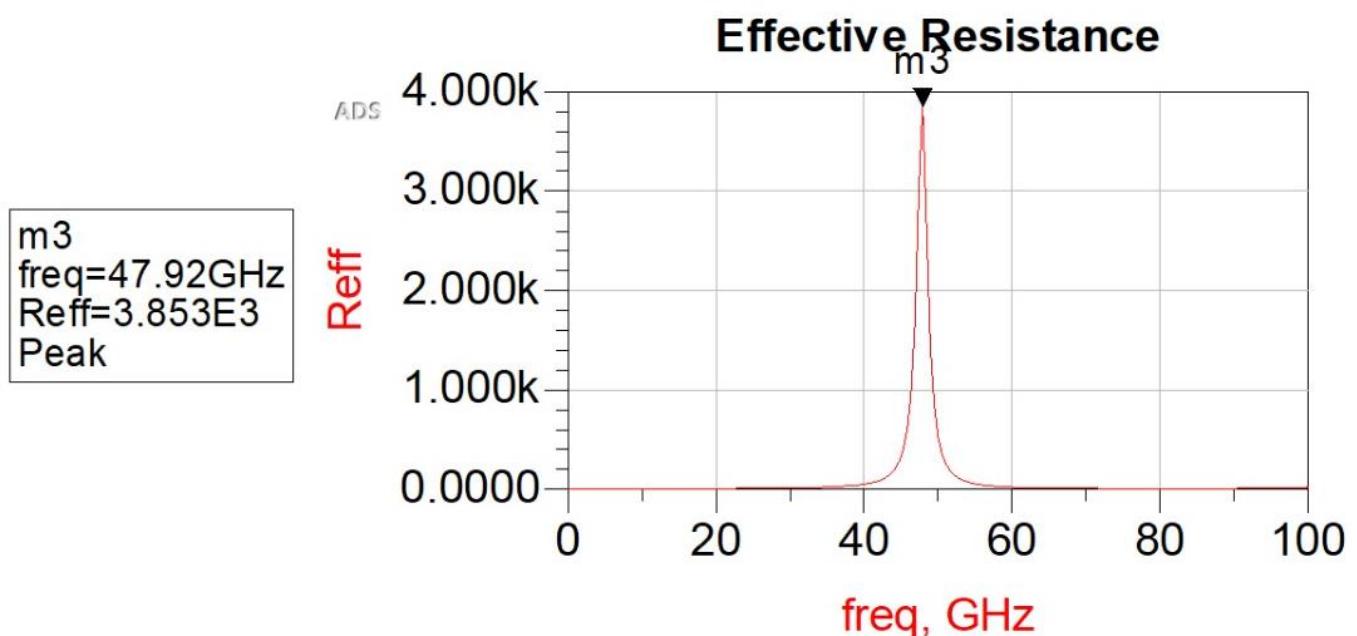


Fig no:10.5.3 Effective resistance vs freq graph of with csrr model

## 10.6 FRACTAL INDUCTOR WITHOUT CSRR:

A Hilbert fractal inductor is a type of planar inductor that uses the Hilbert curve, a space-filling fractal geometry, to create a compact and high-inductance structure. The design folds a long conductive path into a small area, which significantly increases the inductance without enlarging the physical size. This makes it especially suitable for on-chip RF applications, where area efficiency is crucial.

Hilbert inductors offer high inductance density, low mutual coupling, and good electromagnetic compatibility. However, as the fractal order increases, parasitic capacitance and resistive losses also increase, which can reduce the Q-factor. Despite this trade-off, Hilbert fractal inductors are widely used in low-noise amplifiers (LNAs), filters, and impedance matching networks, particularly in high-frequency designs like 5G systems.

This structure increases the effective inductance per unit area by folding the conductive path into a compact, space-efficient pattern. The fractal geometry enhances the inductor's performance by enabling a higher inductance value within a limited chip area, which is critical in modern high-frequency applications like LNAs for 5G systems. Additionally, this design can improve quality factor (Q) and reduce substrate losses, making it ideal for integration in on-chip circuits where both miniaturization and performance are key.

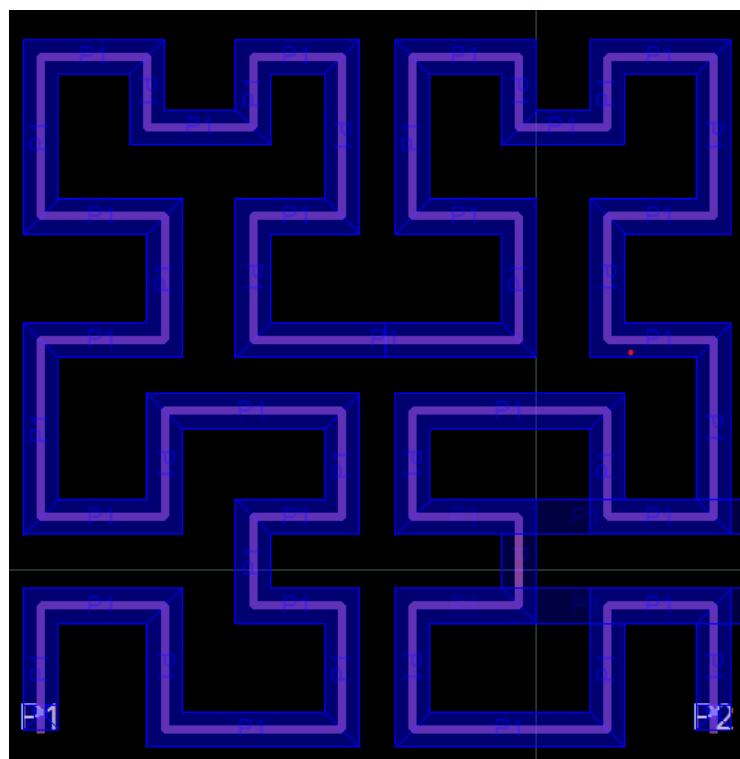


Fig no:10.6.1 Hilbert fractal inductor without csrr

## 10.7 3D VIEW OF FRACTAL INDUCTOR WITHOUT CSRR:

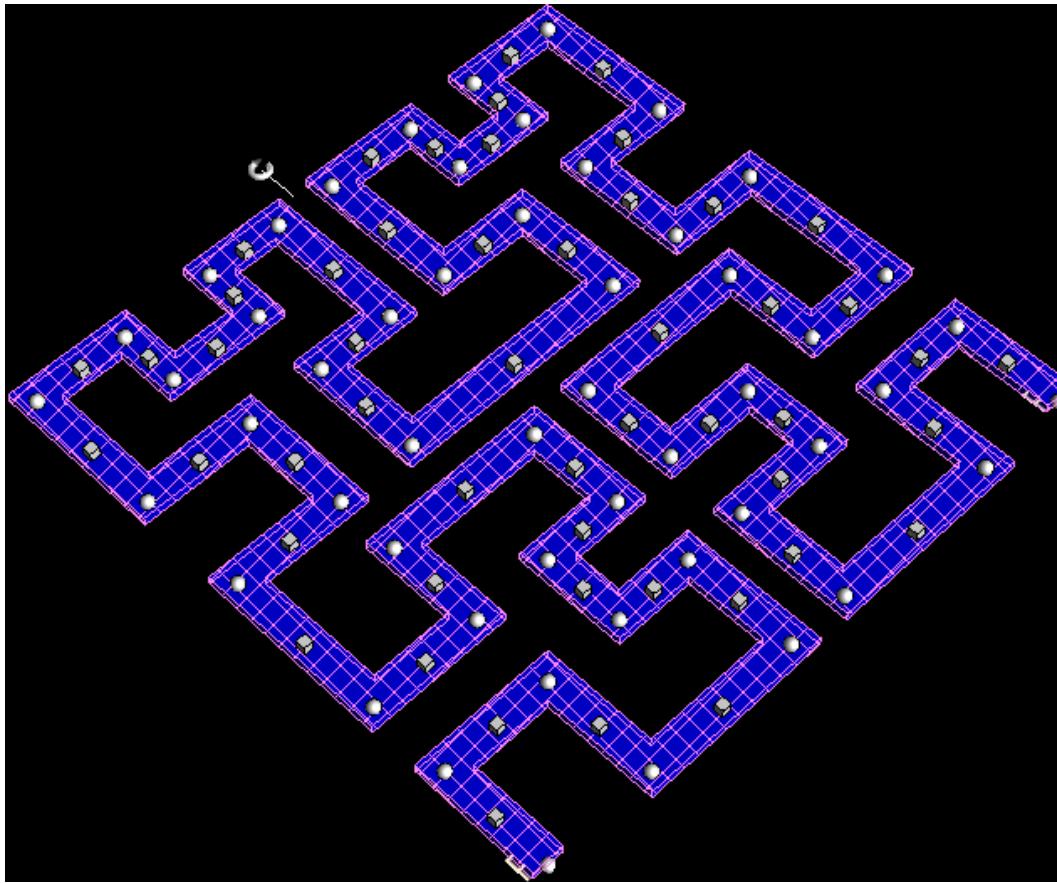


fig No: 10.7.1 3D-view of Hilbert fractal inductor without csrr

The 3D view of the fractal inductor provides an insightful representation of its compact and efficient layout, which follows a Hilbert curve structure. This space-filling geometry allows the inductor to achieve high inductance in a limited footprint, crucial for modern RF integrated circuits. The segmentation seen in the layout helps in analyzing current distribution, while the blue mesh and via connections indicate multiple layers or nodes for interconnection, which can aid in minimizing parasitic resistance and improving performance at high frequencies. The copper trace routing in 3D ensures strong magnetic coupling between adjacent paths, enhancing overall inductance.

In addition, the 3D model helps evaluate the electromagnetic behavior of the inductor, including parasitic capacitance and mutual inductance effects, which are critical at millimeter-wave frequencies.

## 10.8 SUBSTRATE SETTINGS OF HILBERT INDUCTOR WITHOUT CSRR MODEL :

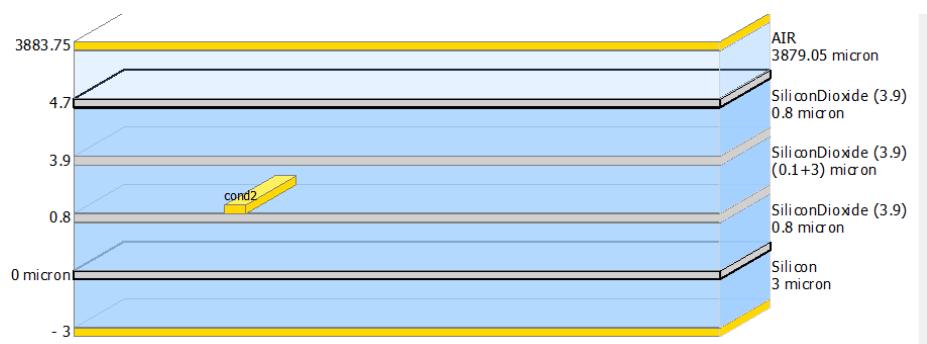


Fig No:10.8.1 Substrate of Hilbert inductor without csrr model.

### Air (3879.05 $\mu\text{m}$ )

- Topmost layer for EM wave propagation in simulations.
- Acts as free space with dielectric constant  $\epsilon_r = 1$ .

### Silicon Dioxide (0.8 $\mu\text{m}$ )

- Thin insulation/passivation layer above the upper metal.
- Provides dielectric isolation from the air.

### Silicon Dioxide (0.1 + 3 $\mu\text{m}$ )

- Layer separating upper conductor (cond2) from other levels.
- Offers dielectric spacing and reduces coupling.

### Silicon Dioxide (0.8 $\mu\text{m}$ )

- Buffer layer between substrate and metal layer M1.
- Reduces parasitic capacitance to the silicon.

### Silicon (375 $\mu\text{m}$ )

- Main substrate base providing mechanical support.
- May cause losses unless high-resistivity silicon is used.

## 10.9 SIMULATION RESULTS OF CSRR MODEL :

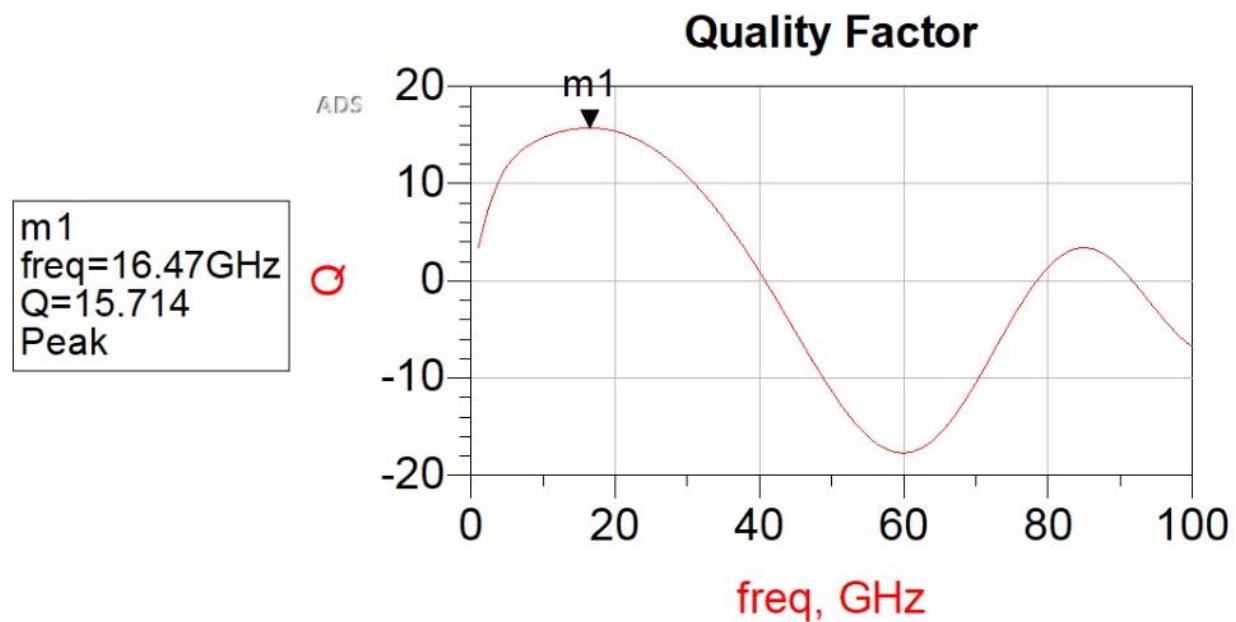


Fig No:10.9.1 inductance vs freq graph of csrr model

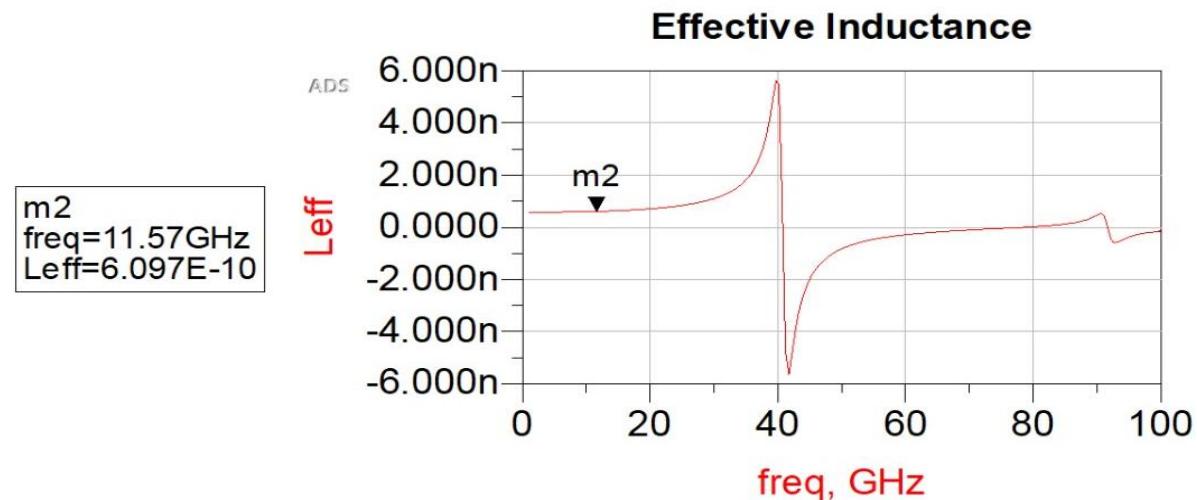


Fig No:10.9.2 Q-factor vs freq graph of csrr model

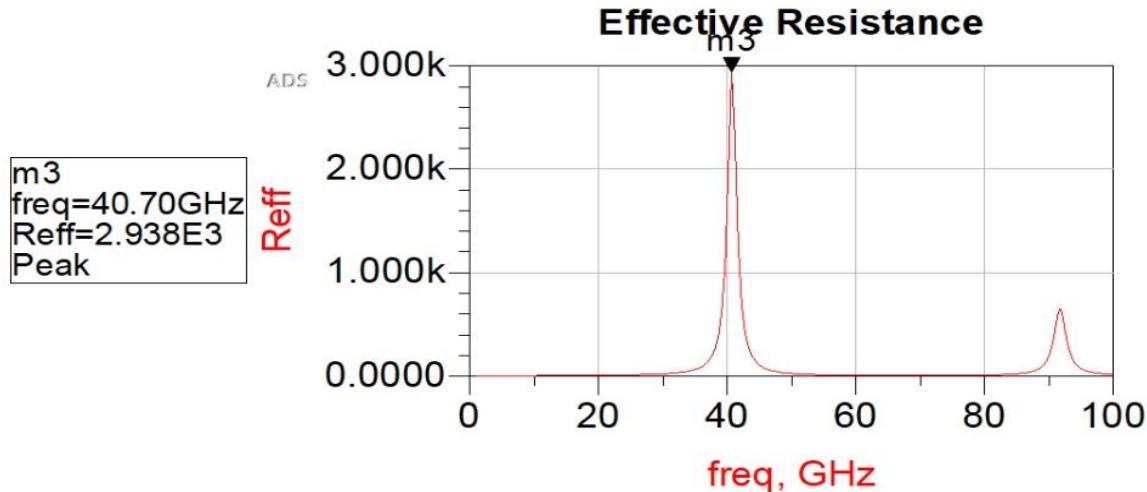


Fig No:10.9.3 Effective resistance vs freq graph of csrr model

## COMPARISON TABLE :

PARAMETER	CSRR DESIGN	WITHOUT CSRR
<b>Q-Factor</b>	<b>16.992(19.53GHZ)</b>	<b>15.714(16.47GHZ)</b>
<b>Inductance</b>	<b>0.6596(19.53GHZ)</b>	<b>0.609(11.57GHZ)</b>
<b>Figure of Merit(GHZ/<math>\mu\text{m}^2</math>)</b>	<b>4.0708</b>	<b>3.1975</b>
<b>SRF</b>	<b>47.92(GHZ)</b>	<b>40.70(GHZ)</b>
<b>Area</b>	<b>200<math>\mu\text{m}^2</math></b>	<b>200<math>\mu\text{m}^2</math></b>
<b>Width</b>	<b>10<math>\mu\text{m}</math></b>	<b>10<math>\mu\text{m}</math></b>

Table No:10.9.1Comparising the parameters with and without csrr model



To calculate the Figure of Merit (FoM) and the percentage increase, we'll use the given formula:

$$\text{FoM} = \text{SRF (GHz)} \times \text{Q} / \text{Area } (\mu\text{m}^2)$$

### With CSRR (New):

- Q=16.99
- SRF=47.92 GHz
- Area=200  $\mu\text{m}^2$
- FOM=47.92 GHz\*16.99/200  $\mu\text{m}^2$ =4.0708GHz/ $\mu\text{m}^2$

### Without CSRR (Old):

- Q=15.714
- SRF=40.70 GHz
- Area=200  $\mu\text{m}^2$
- FOM=40.70 GHz\*15.714/200  $\mu\text{m}^2$ =3.1975GHz/ $\mu\text{m}^2$
- **Percentage Increase:** %increase=(FoMnew-FoMold)/FoMold×100  
 $\rightarrow (4.0708 - 3.1975) / 3.1975 \times 100 = (0.8733 / 3.1975) \times 100 \approx 27.31\%$

# CHAPTER 11

## IMPORTING THE FRACTAL IN LNA DESIGN

### 11.1 CONVERSION OF FRACTAL LAYOUT INTO A COMPONENT:

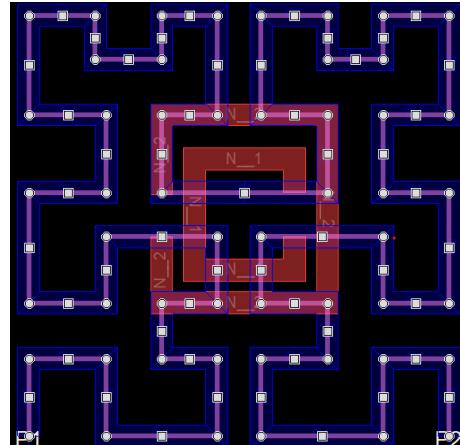


Fig No:11.1.1CSRR Hilbert fractal layout

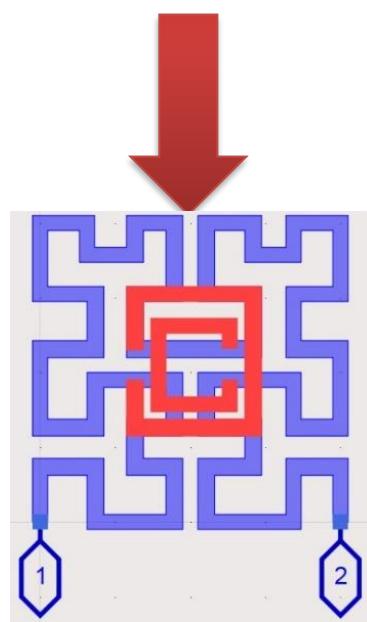
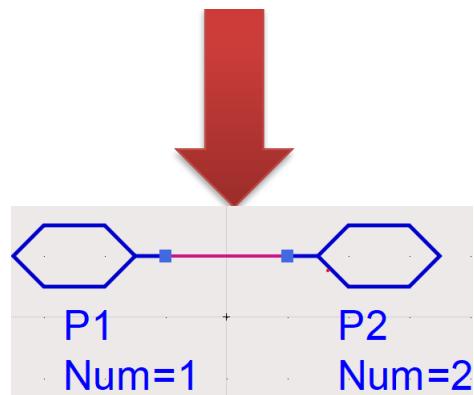


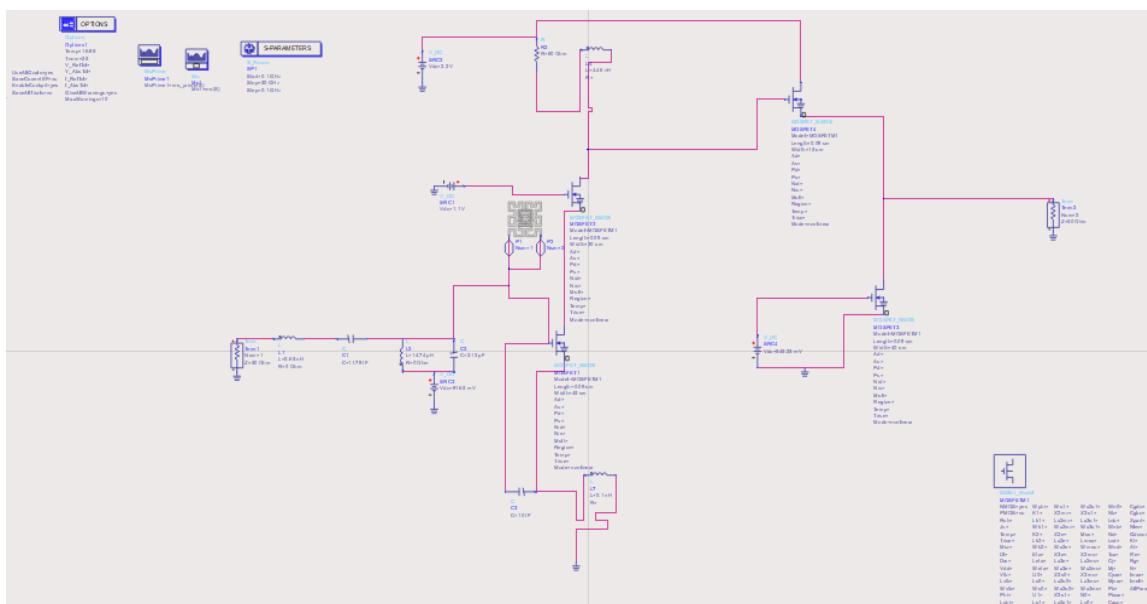
Fig No:11.1.2 Component of Hilbert Fractal Inductor(CSRR)

## 11.2 IMPORTING THE HILBERT FRACTAL WITH CSRR IN LNA DESIGN:

In ADS, this process involves opening the schematic or layout editor and selecting the fractal inductor from the library or project workspace. The imported component maintains its predefined electrical characteristics, including inductance, quality factor (Q), and impedance, ensuring accurate simulations when combined with other circuit elements. Proper placement and orientation are crucial to minimize unwanted parasitic effects and to ensure efficient signal flow.

In This LNA utilizes a **CSRR structure** integrated into the design, typically for **performance enhancement in terms of selectivity, bandwidth control, and miniaturization**. CSRRs are known for their **negative permittivity characteristics**, which enable them to act like notch or bandpass filters, depending on their configuration. In LNA circuits, integrating a CSRR can help in **suppressing unwanted frequencies**, improving **gain flatness**, and even contributing to **noise reduction** by filtering out-of-band noise components.

Overall, combining CSRR structures with traditional LNA design improves **compactness and functional performance**, making the circuit suitable for modern communication systems where size, noise performance, and frequency selectivity are critical.



When integrating it into the LNA schematic, special attention should be given to impedance matching and noise reduction, as the inductor plays a key role in determining the amplifier's overall efficiency. Additional tuning may be required by adjusting the LNA's transistor biasing and matching networks to fully utilize the benefits of the fractal inductor's enhanced inductance and compact design.

### 11.3 SIMULATION RESULTS:

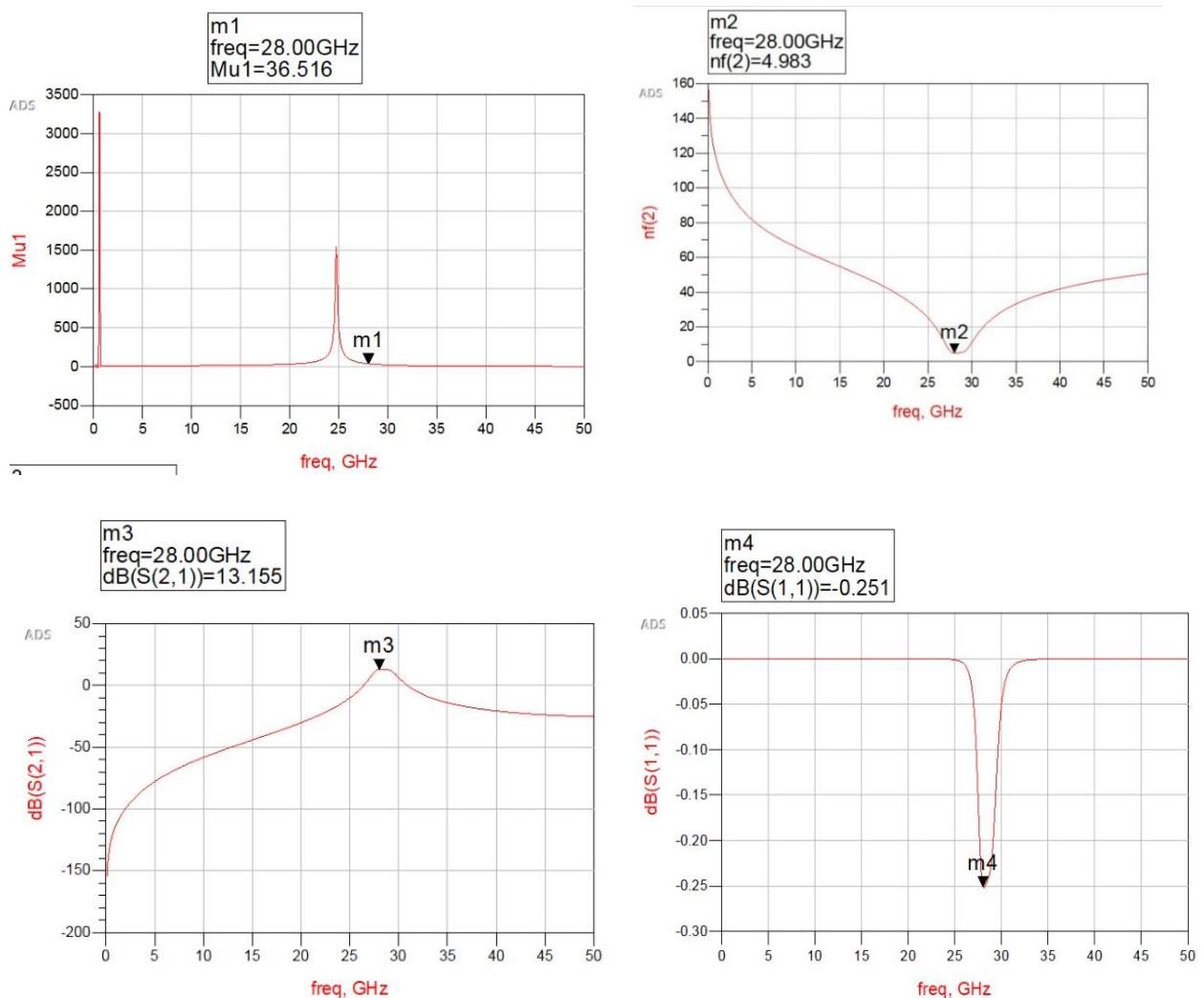


Fig No:11.1.4 LNA results with csrr model Hilbert Fractal Inductor

#### 11.3.1 MU STABILITY FACTOR

LNA across frequency. At 28 GHz, the Mu value is 36.516, which is significantly greater than 1, indicating that the amplifier is **unconditionally stable** at this frequency. This is an essential

requirement for low-noise amplifiers to prevent oscillations during operation.

The first plot in the top-left corner represents the **Mu stability factor** plotted against frequency. This factor is crucial in determining whether the Low Noise Amplifier (LNA) is stable over its intended frequency range. The Mu value at 28 GHz is 36.516, which is far above the threshold of 1, indicating **unconditional stability** at the target frequency.

This means that under any passive source or load impedance conditions, the LNA will not oscillate, which is essential for reliable performance in sensitive receiver systems, especially in high-frequency bands like the **Ka-band (26.5–40 GHz)** used in 5G, satellite, and radar communications. The sharp rise in Mu near 28 GHz also suggests that the circuit has been finely tuned to operate optimally at that point, and the falloff before and after this frequency shows that the design is frequency-selective. High Mu values also provide design flexibility for the matching networks without compromising stability, making this a strong indicator that your LNA can be integrated into larger RF front-end modules without risk of unwanted feedback or oscillations.

### **11.3.2 S(11)INSERTION LOSS:**

The second and fourth plots (top-right and bottom-right) display the parameters **S12** and **S11**, respectively, which help analyze the **reverse isolation** and **input matching** of the amplifier. The S12 parameter at 28 GHz is approximately -4.983 dB, indicating that there is some reverse transmission from the output back to the input. While ideal LNAs would exhibit S12 values below -10 dB for strong isolation, a value near -5 dB is still acceptable for many applications, particularly when layout and parasitic constraints exist.

It shows that some energy is reflected back, but not enough to cause major issues unless cascaded stages are very sensitive. The **S11 value of -0.251 dB**, however, is a concern—it shows that the input is **very poorly matched**, as nearly all the incident power is being reflected rather than accepted by the amplifier. Ideally, for maximum power transfer and minimal reflection, S11 should be below -10 dB (or even lower in precision systems). This poor input return loss suggests that the input matching network needs significant improvement, perhaps by adjusting the transmission line impedance, using matching stubs, or optimizing lumped elements. Poor input matching can degrade noise performance and reduce the effective gain, especially in narrowband, high-frequency applications.

### **11.3.3 GAIN:**

The third plot, located in the bottom-left corner, corresponds to **S21 in dB**, which measures the **forward gain** of the amplifier, a critical parameter that defines how effectively the LNA amplifies incoming signals. At 28 GHz, the gain is **13.155 dB**, which is considered very good for a low-noise amplifier in millimeter-wave applications. This level of gain ensures that weak signals, typical in wireless front-end receivers, are sufficiently amplified before being passed on to subsequent stages, such as mixers or filters.

The smooth gain curve peaking near 28 GHz confirms that the amplifier is optimally designed for this frequency, with minimal gain roll-off in the vicinity. High gain is especially important in mmWave systems due to higher path loss and atmospheric attenuation, so achieving over 13 dB in this band is beneficial. Additionally, the shape of the gain curve suggests that the amplifier has decent bandwidth characteristics, although exact bandwidth analysis would require 3 dB cutoff points. In summary, while the LNA design offers solid gain and excellent stability, its input matching performance needs to be enhanced to achieve the full potential of the amplifier in practical deployment scenarios.

### **11.3.4 NOISE FIGURE:**

The graph displays the Noise Figure (NF) response of the designed LNA over a frequency range from 0 to 50 GHz. As observed, the noise figure varies significantly with frequency, reaching its minimum value of 4.983 dB at 28 GHz, which is the target operating frequency of the amplifier. This result indicates that the amplifier maintains low internal noise at the desired frequency, which is essential for enhancing signal clarity in sensitive receiver applications. At lower frequencies, the noise figure rises steeply, reaching values above 140 dB below 5 GHz, due to impedance mismatches and reduced gain in off-resonance regions. Similarly, after 28 GHz, the NF starts increasing again, suggesting that the amplifier's optimal low-noise performance is sharply centered around 28 GHz. This emphasizes the effectiveness of the Hilbert fractal and CSRR structures in achieving narrowband low-noise behavior, which is highly desirable in applications like 5G receivers, where minimal noise is critical for maintaining signal fidelity.

## CHAPTER 12

### CONCLUSION

The design and simulation of a 28 GHz Low Noise Amplifier (LNA) using a Hilbert fractal inductor integrated with a Complementary Split Ring Resonator (CSRR) structure have shown promising results for high-frequency, compact, and efficient amplifier applications—especially in the mmWave domain. The use of Hilbert fractal geometry has enabled effective miniaturization while maintaining the necessary inductive behavior at millimeter-wave frequencies. This fractal structure also enhances electromagnetic performance by enabling multi-resonance paths, increasing the inductance per unit area, and improving the overall frequency response.

The inclusion of CSRRs plays a critical role in tuning the impedance and achieving enhanced filter-like characteristics within the signal path. CSRRs act as sub-wavelength resonant structures etched on the ground plane, offering negative permittivity effects that allow precise control over the resonance frequency, return loss, and bandwidth. Their integration within the matching or feedback network contributes to enhanced selectivity, sharp resonance, and band rejection capabilities, which are vital in suppressing undesired harmonics or spurious responses. In the current design, the use of CSRR improved the circuit's filtering behavior and added degrees of freedom in impedance matching.

From simulation results, the LNA demonstrates a forward gain ( $S_{21}$ ) of 13.15 dB, excellent stability ( $M_u = 36.516$ ) at 28 GHz, and moderate reverse isolation ( $S_{12} = -4.98$  dB). However, the input return loss ( $S_{11} = -0.25$  dB) indicates poor impedance matching at the input, which requires optimization through either enhanced matching network design or tuning the CSRR placement for improved input coupling. Nonetheless, the CSRR's contribution to gain shaping and stability tuning is evident, and with slight design improvements, the input reflection can also be minimized.

In summary, the combination of Hilbert fractal inductors and Complementary Split Ring Resonators has proven to be a powerful approach in designing compact, stable, and high-gain LNAs for 5G and millimeter-wave applications. This hybrid structure enhances the electromagnetic performance of the circuit without increasing chip area, making it suitable for modern RF front-end integration. With future optimization focused on improving return loss and bandwidth extension, this design can be evolved into a practical solution for next-generation wireless systems.

# **CHAPTER 13**

## **FUTURE SCOPE**

This project has laid a strong foundation for the design of compact and high-performance Low Noise Amplifiers (LNAs) using Hilbert fractal inductors and Complementary Split Ring Resonators (CSRRs). Moving forward, one of the most promising areas for future development lies in hardware implementation and fabrication of the proposed LNA. Although simulation results are encouraging, real-time performance can vary due to parasitics, substrate losses, and layout effects. Therefore, designing this LNA on a physical substrate (such as GaAs, CMOS, or RF-PCB) and validating the simulation results with S-parameter measurements, gain, and noise figure analysis using a Vector Network Analyzer (VNA) would be a crucial step toward practical deployment.

Another key area of improvement is the optimization of input matching and noise performance. In this design, the input return loss ( $S_{11}$ ) was relatively poor, which can impact noise figure and overall signal integrity. Future work could explore advanced matching techniques using additional CSRRs, defected ground structures (DGS), or adaptive tuning circuits to improve impedance matching across a wider bandwidth. Additionally, integrating a low noise figure (NF) optimization module and studying the amplifier's performance under different temperature and bias conditions would make the design more robust for real-world applications.

This architecture can also be extended for multi-band or wideband applications, where fractal geometries like Hilbert curves naturally exhibit multiband properties. By cascading different orders of fractal inductors or varying the dimensions of CSRRs, future designs can support multiple frequencies simultaneously, making them ideal for next-generation systems like 5G, 6G, satellite receivers, and IoT front-ends. Moreover, with the growing interest in reconfigurable and tunable RF systems, this work can serve as a foundation for reconfigurable LNA designs, where the resonance frequency or gain can be dynamically adjusted using varactors, MEMS switches, or tunable metamaterials.

## CHAPTER 14

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## CHAPTER 14

### TIME LINE

	<b>Sl no</b>	<b>Activity</b>	<b>Tentative month</b>	<b>Status</b>
PHASE-1	1	Team allotment	August 2024	Completed
	2	Abstract submission	August 2024	Completed
	3	Registration presentation - I	September 2024	Completed
	4	To learn on-chip Hilbert inductor basics	September 2024	Completed
	5	designing on-chip inductorwith tools		
	6	Study of proposed method	October 2024	Completed
	7	Software development & Presentation - II	November 2024	Completed
	8	Report submission	December 2024	Completed
PHASE-2	9	LNA design with ADS tool	Jan 2024, Feb 2024	Completed
	10	Final Presentation	March 2024	completed
	11	Submission of project Report and paper	March 2024	-----