PROJECT - 2

NAVIGATION CHIP

COMPLETE DFT DOCUMENTATION

CONTENTS

1. Introduction

The Level-4 Navigation Chip project represents a high-complexity System-on-Chip (SoC) design intended to model real-world navigation and positioning systems used in automotive electronics, aerospace systems, defense applications, and advanced embedded platforms. Navigation chips differ significantly from mid-level communication chips due to their strict performance, reliability, and timing accuracy requirements. Any functional failure or timing defect in such systems can lead to catastrophic consequences, making manufacturability and testability extremely critical.

As semiconductor technology advances, navigation chips have grown significantly in size and complexity, integrating tens of thousands of flip-flops, deep pipelines, and high-speed datapaths. In such designs, traditional functional testing is completely insufficient to guarantee defect coverage. Design for Testability (DFT) therefore becomes an essential part of the design flow rather than an optional enhancement.

The primary objective of this project was to implement a scalable, production-quality DFT architecture capable of handling a very large number of sequential elements while ensuring high fault coverage, minimal test cost, and support for at-speed testing. The project focuses on full scan insertion, aggressive scan compression, robust clock handling, ATPG for both structural and timing faults, and comprehensive verification using industry-standard tools.

This project closely mirrors real semiconductor industry workflows for large SoCs and provides hands-on exposure to the challenges faced by DFT engineers working on high-end navigation and control systems.

2. Problem Statement and Motivation

Modern navigation chips operate in safety-critical environments and are fabricated using advanced semiconductor technologies where manufacturing defects are unavoidable. These defects include stuck-at faults, transition delay faults, bridging faults, and timing-related defects that cannot be reliably detected using functional test vectors alone.

The primary problem addressed in this project is the lack of controllability and observability in large, deeply sequential designs. Internal nodes in such designs are buried behind multiple layers of logic and registers, making it impossible to activate and observe faults through primary inputs and outputs. As design size increases, this problem worsens, leading to low test coverage and reduced yield if DFT is not applied.

Another major motivation is test cost. Large designs generate massive volumes of test data, which translates directly into higher tester memory requirements and longer test application times. Without compression, testing a 44K-flip-flop design would be economically impractical.

Additionally, navigation chips operate at very high frequencies, making timing defects a serious concern. Detecting these defects requires at-speed testing, which introduces further complexity in clock control and scan architecture. This project demonstrates how modern DFT techniques overcome these challenges and enable reliable, cost-effective testing of large navigation SoCs.

3. Design Specifications

The Level-4 Navigation Chip was designed as a large-scale digital SoC optimized for high performance and accurate timing behavior. Unlike smaller hierarchical designs, this project uses a flat scan architecture to maximize compression efficiency and simplify ATPG.

The approximate flip-flop count of the design is around 44,000, placing it firmly in the large-SoC category. The design operates at a high functional frequency of approximately 400 MHz, reflecting real navigation and signal-processing requirements. A dedicated scan clock is used exclusively for scan shift operations to ensure safe and reliable testing.

The selected DFT methodology includes full scan insertion combined with high-ratio scan compression using Embedded Deterministic Test (EDT) and at-speed testing enabled by an On-Chip Clock Controller (OCC). These choices align with industry best practices for large, performance-critical SoCs.

4. Functional Architecture Description

The functional architecture of the navigation chip consists of multiple high-performance logic blocks responsible for computation, control, and data handling. These blocks are tightly integrated and heavily pipelined to achieve high throughput and low latency. Unlike communication chips that emphasize IP reuse, navigation chips often prioritize performance optimization, leading to flatter architectures.

From a DFT perspective, this functional complexity presents significant challenges. Deep pipelines increase the difficulty of fault activation, while tight timing margins make it essential that DFT logic does not degrade performance. Therefore, scan logic was carefully integrated to remain transparent during functional operation.

The architecture was designed such that DFT structures remain inactive during normal operation and are enabled only during test mode, ensuring no functional or timing penalty.

5. Design Complexity Breakdown

The complexity of the Level-4 Navigation Chip arises primarily from three factors: large flip-flop count, high operating frequency, and deep sequential logic. With approximately 44,000 flip-

flops, naive scan insertion would result in extremely long scan chains and unacceptable test times.

To manage this complexity, a flat scan architecture was adopted with a large number of scan chains distributed evenly across the design. This approach simplifies compression logic placement and improves ATPG efficiency. The design complexity also necessitated careful consideration of clocking, reset behavior, and power consumption during scan.

This section highlights how large-scale SoC complexity directly influences DFT architectural decisions.

6. Flip-Flop Count Estimation Methodology

Accurate flip-flop estimation is a foundational step in DFT planning. In this project, the total flip-flop count of approximately 44,000 was determined through a combination of RTL analysis and scan chain planning.

Rather than relying solely on raw RTL statistics, the estimation process considered how flip-flops would be distributed across scan chains to ensure balanced chain lengths. This approach helps avoid extremely long chains that could negatively impact test time and ATPG convergence.

The high flip-flop count directly influenced decisions related to scan chain count, compression ratio, and tester resource requirements.

7. Clock Architecture and Constraints

7.1 Functional Clock

The navigation chip operates at a functional frequency of approximately 400 MHz, reflecting the performance requirements of real navigation systems. This high-frequency clock drives performance-critical datapaths and control logic.

From a DFT standpoint, it was essential to ensure that scan logic does not interfere with functional timing. Functional clocks were carefully isolated from scan clocks, and appropriate timing constraints were applied to avoid false violations during timing analysis.

7.2 Scan Clock

A dedicated scan clock operating at 25 MHz was introduced for scan shift operations. The lower frequency minimizes switching activity and reduces dynamic power consumption during scan.

Clock multiplexing controlled by scan enable signals ensures safe switching between functional and scan clocks without causing glitches or metastability.

8. Scan Insertion Strategy

The scan insertion strategy for the Level-4 Navigation Chip was designed with the primary goal of achieving maximum controllability and observability while preserving the high-performance nature of the functional design. Given the large size of the design and the presence of deeply pipelined logic, a full scan methodology was selected. In this approach, all functional flip-flops were replaced with scan-enabled flip-flops, allowing direct access to internal states during test mode.

A flat scan insertion approach was adopted instead of a hierarchical one, as flat architectures are better suited for aggressive scan compression in large SoCs. This decision simplified scan chain balancing and enabled uniform distribution of scan logic across the design. Scan enable signals were globally controlled to ensure consistent behavior during scan shift and capture operations.

Special care was taken to ensure that scan insertion did not adversely impact functional timing. Scan multiplexers were placed in a timing-aware manner, and scan logic was kept inactive during normal functional operation. Reset behavior was also carefully reviewed to ensure that scan flip-flops initialize correctly in both functional and scan modes.

This scan insertion strategy ensured that the design remained fully testable while maintaining functional correctness and timing integrity.

9. Scan Chain Architecture

The scan chain architecture of the Level-4 Navigation Chip was designed to efficiently handle the large number of flip-flops while minimizing test time and ATPG complexity. With approximately 44,000 flip-flops, a single or small number of scan chains would result in extremely long shift times, making production testing impractical.

To address this, the design was partitioned into 106 balanced scan chains, each containing approximately 420 flip-flops. This distribution ensured that scan shift time was evenly spread across all chains, reducing overall test time and avoiding bottlenecks caused by excessively long chains.

Balanced scan chains also improve ATPG efficiency by simplifying pattern generation and reducing convergence issues. Additionally, uniform chain lengths help minimize power spikes during scan shifting, as switching activity is evenly distributed across the design.

The scan chain architecture was validated using scan DRC checks to ensure proper connectivity, correct scan enable behavior, and safe clocking across the entire design.

10. Scan Compression (Embedded Deterministic Test – EDT)

Given the massive test data volume associated with a 44K-flip-flop design, scan compression was a mandatory requirement. Embedded Deterministic Test (EDT) was selected as the compression technique due to its proven effectiveness in large-scale industrial designs.

EDT works by reducing the amount of data that must be supplied by the tester. Test stimuli are compressed at the tester interface and then decompressed on-chip before being applied to scan chains. Similarly, scan responses are compacted on-chip before being sent back to the tester. This approach drastically reduces tester memory requirements and test application time.

In this project, a compression ratio of approximately 53× was achieved. This means that the number of external tester channels required was significantly reduced, making the design economically viable for high-volume manufacturing. Despite the high compression ratio, fault coverage remained high due to the deterministic nature of EDT.

The EDT logic was carefully integrated to ensure compatibility with the flat scan architecture and to avoid any impact on functional operation.

11. Automatic Test Pattern Generation (ATPG) Flow

Automatic Test Pattern Generation (ATPG) is a critical step in converting the DFT-enabled design into manufacturable test patterns. For the Level-4 Navigation Chip, ATPG was performed targeting both stuck-at faults and transition delay faults, ensuring comprehensive coverage of structural and timing-related defects.

ATPG was primarily executed in compressed mode, leveraging the benefits of EDT to reduce the number of patterns. Compressed ATPG significantly reduced test time while maintaining high fault coverage. In addition, bypass mode ATPG was used selectively for debug purposes, allowing direct access to scan chains without compression logic.

Fault simulation was used to evaluate coverage and identify untested faults. Any coverage gaps were analyzed and resolved through minor DFT refinements or constraint adjustments. Despite the large design size, the ATPG flow achieved fault coverage that meets industry standards for navigation-class SoCs.

12. At-Speed Testing and OCC Integration

Navigation chips operate at high frequencies and are susceptible to timing-related defects that cannot be detected using slow scan clocks. To address this, at-speed testing was implemented using an On-Chip Clock Controller (OCC).

The OCC generates precise, high-frequency clock pulses during the capture phase of scan testing while isolating scan clocks from functional clocks. This allows the design to be tested under real operating conditions without violating scan timing constraints.

In this project, the functional clock operates at approximately 400 MHz, and the OCC ensures that capture cycles occur at this speed. This enables detection of transition delay faults, hold violations, and other timing-related defects that could otherwise escape detection.

The integration of OCC significantly enhanced test quality and reliability, making the design suitable for safety-critical navigation applications.

13. Verification and Simulation

Verification is a crucial step in validating the correctness of the DFT implementation. For the Level-4 Navigation Chip, verification was performed at multiple stages to ensure robustness and reliability.

Scan Design Rule Checks (DRC) were first executed to verify scan connectivity, clocking rules, reset behavior, and scan enable control. Any violations identified during DRC were analyzed and corrected before proceeding further.

Following DRC, scan pattern simulations were performed using industry-standard simulation tools. These simulations verified correct scan shift, capture, and response behavior under realistic conditions. Both compressed and bypass ATPG patterns were simulated to ensure correctness across all test modes.

This comprehensive verification flow ensured that the DFT architecture was functionally correct and ready for production use.

14. Challenges and Debugging

Several challenges were encountered during the implementation of DFT for the Level-4 Navigation Chip. One major challenge was managing the power consumption during scan shift, as large designs can experience significant switching activity. This was mitigated through careful scan clock frequency selection and balanced scan chains.

Another challenge involved timing closure in the presence of scan logic, particularly due to the high functional frequency. This required careful clock isolation and constraint management. Debugging long scan chains and ATPG convergence issues also required iterative refinement of scan architecture and ATPG constraints.

Overcoming these challenges provided valuable real-world experience in debugging large-scale DFT implementations.

15. Tools Used and Their Purpose

The successful implementation of Design for Testability (DFT) in a large-scale Level-4 Navigation Chip requires the use of robust, industry-proven Electronic Design Automation (EDA) tools. Given the high flip-flop count, aggressive compression requirements, and at-speed testing needs, only production-grade tools were suitable for this project. The tools used in this project closely reflect those employed in real semiconductor companies, ensuring strong industry relevance.

15.1 Tessent Scan (Mentor Graphics / Siemens EDA)

Tessent Scan was the primary tool used for scan insertion and scan architecture management. This tool played a foundational role in converting the functional design into a testable design.

Tessent Scan was used to replace all functional flip-flops with scan-enabled flip-flops while preserving functional behavior. It enabled the definition of scan enable signals, scan clock routing, and scan data paths across the entire design. Given the flat architecture and large size of the navigation chip, Tessent Scan was essential in creating and managing a large number of scan chains in a structured and scalable manner.

In addition to scan insertion, Tessent Scan was extensively used to perform Scan Design Rule Checks (DRC). These checks ensured that all scan chains were correctly connected, clocks were safely multiplexed, resets were scan-safe, and no structural violations existed that could affect ATPG or scan operation. Fixing scan DRC violations early prevented costly debug cycles later in the flow.

15.2 Tessent TestKompress (Embedded Deterministic Test – EDT)

Tessent TestKompress was used to implement scan compression using Embedded Deterministic Test (EDT). Given the approximately 44,000 flip-flops in the design, uncompressed scan testing would have resulted in extremely long test times and excessive tester memory requirements.

TestKompress enabled the creation of a highly compressed scan architecture by inserting decompression logic on the input side and compaction logic on the output side. This allowed a large number of internal scan chains to be driven using a much smaller number of external tester channels.

A compression ratio of approximately 53× was achieved, significantly reducing the number of ATPG patterns and test application time. Despite this aggressive compression, high fault

coverage was maintained due to the deterministic nature of EDT, making TestKompress a critical enabler for manufacturability of the Level-4 Navigation Chip.

15.3 Tessent ATPG

Tessent ATPG was used for Automatic Test Pattern Generation targeting both structural and timing-related faults. This tool was responsible for generating test patterns that detect manufacturing defects in the scan-enabled design.

ATPG was performed for:

- Stuck-at faults, which represent static defects such as opens and shorts
- Transition delay faults, which model timing-related defects critical in high-frequency designs

The tool supported both compressed ATPG mode, which works in conjunction with EDT, and bypass mode, which allows direct access to scan chains for debug purposes. Fault simulation and coverage analysis features were used to measure test quality and identify any remaining coverage gaps.

The ability of Tessent ATPG to efficiently handle very large designs was essential in achieving industry-acceptable fault coverage within reasonable runtime.

15.4 Tessent MBIST

Tessent MBIST was used to implement Memory Built-In Self-Test (MBIST) for all embedded memory blocks present in the navigation chip. Memories are particularly vulnerable to manufacturing defects and require specialized test techniques beyond logic scan.

The MBIST logic generated and applied March-based test algorithms capable of detecting common memory faults such as stuck-at faults, transition faults, address decoder faults, and coupling faults. Memory testing was isolated from logic scan testing to ensure independent and thorough validation of memory structures.

Using Tessent MBIST ensured that the navigation chip’s memory components met reliability and quality standards expected in safety-critical applications.

15.5 QuestaSim (Mentor Graphics / Siemens EDA)

QuestaSim was used extensively for functional, scan, and ATPG pattern simulation. Simulation is a critical verification step that validates the correctness of DFT structures before silicon fabrication.

Using QuestaSim, scan shift and capture operations were simulated to ensure that scan chains behaved as expected. ATPG patterns generated by Tessent ATPG were applied in simulation to verify fault detection and response correctness. Both compressed and bypass mode patterns were validated.

Simulation helped identify and resolve issues such as incorrect scan enable behavior, clocking problems, and reset interactions, ensuring a robust DFT implementation.

16. Final Outcome and Conclusions

The Level-4 Navigation Chip project successfully demonstrates a complete, scalable, and industry-grade DFT implementation for a large SoC. Through the use of full scan insertion, aggressive scan compression, at-speed testing, and rigorous verification, the design was transformed into a fully testable and production-ready system.

High fault coverage was achieved despite the large flip-flop count, validating the effectiveness of the chosen DFT architecture. Test application time and tester memory requirements were significantly reduced through the use of EDT-based compression. At-speed testing enabled detection of timing-related defects critical for navigation applications.

Overall, this project provides strong practical experience in large-scale DFT planning, execution, and verification. It closely reflects real semiconductor industry workflows and demonstrates readiness for professional DFT engineering roles, particularly in high-performance and safety-critical SoC development.