AMIREDDY SIVANAGIREDDY

+91 7780323890 sivanagireddy.vlsi.dft@gmail.com portfoilo linkedin

SUMMARY

Extremely motivated graduate with strong logical, analytical, and technical skills, seeking an opportunity to contribute effectively to an organization while continuously enhancing my expertise and career growth.

PROFESSIONAL TRAINING

Design for Testability (DFT) Training – VLSI Guru Institute June 2025 – Dec 2025

- Gained hands-on experience in scan insertion and scan compression techniques.
- Developed practical knowledge of fault modeling, fault simulation, and ATPG.
- Built a strong foundation in digital design concepts relevant to ASIC testing.
- Acquired familiarity with the end-to-end ASIC design flow.
- Comfortable using GVIM for efficient RTL and script editing.
- Possess basic working knowledge of Linux commands for design and test environments.

TECHNICAL SKILLS

Design for Testability (DFT):

- Scan insertion and scan stitching
- Scan compression (EDT)
- ATPG and fault coverage analysis
- On-Chip Clock Controller (OCC)
- JTAG and Boundary Scan (IEEE 1149.1)
- Memory Built-In Self Test (MBIST)

Digital Design: Combinational and sequential logic design
Simulation & Verification: RTL and gate-level simulation using QuestaSim
Tools & Technologies: Mentor Graphics Tessent (Scan, ATPG, EDT, MBIST) ,Design Compiler (basic familiarity)
Operating Systems: Linux, Windows
Scripting & Editors: GVIM, Notepad, Basic TCL scripting
Productivity Tools: Microsoft Excel and Word

PROJECTS (DFT)

Design 1 – Communication Chip (~4K flip-flops, Hierarchical Design)

- Performed MBIST insertion and full scan stitching on a hierarchical design with parent and multiple child cores.
- Executed DFT DRC cleanup to ensure compliance with scan and test rules.
- Implemented EDT scan compression and On-Chip Clock Controller (OCC) insertion to support at-speed testing.
- Generated ATPG patterns and analyzed fault coverage to validate test quality.
- Verified scan integrity through serial and parallel scan simulations.

- Worked on multiple DFT test cases to validate scan chains, MBIST execution, ATPG pattern behavior, and overall test readiness.

Design 2 – Navigation Chip (~42K flip-flops)

- Implemented MBIST insertion and scan stitching on a medium-sized design.
- Resolved DFT DRC violations to achieve clean DFT signoff.
- Integrated EDT scan compression and OCC to enable compressed and at-speed testing.
- Performed ATPG coverage analysis to ensure adequate fault detection.
- Validated the design using multiple DFT test cases to confirm scan functionality, MBIST operation, and ATPG coverage correctness.

PROJECTS (B.TECH)

TITLE: ACCIDENT DETECTION AND NOTIFICATION SYSTEM
Description:

Designed and implemented an embedded accident detection system integrating multiple sensors (accelerometer, crash, alcohol, eye blink, ultrasonic) with microcontrollers (Arduino Uno, NodeMCU) for real-time monitoring and reporting. Developed and tested hardware–software interfaces, optimized signal acquisition, and implemented fault detection mechanisms to ensure reliable sensor data. Utilized ThingSpeak cloud and GPS for real-time location tracking and automated alert notifications.

1. Sensors continuously monitor vehicle movement and driver condition.
2. If abnormal conditions (crash, drowsiness, alcohol detection) are detected, system activates alerts.

EDUCATION

College	Degree	Duration	Percentage
MVR College of Engineering and Technology	Bachelor's degree -ECE	2021 – 2025	78%
Kamala – Junior College	Intermediate (10+2 class)	2019 – 2021	72%
Sri Chaitanya High School	Secondary School	2018 – 2019	95%

CERTIFICATIONS

Design For Testability - Issued by: VLSI Guru Institute Bengaluru

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Declaration

I hereby declare that the information furnished above is true and complete to the best of my knowledge and belief.