AMIREDDY SIVANAGIREDDY

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SUMMARY

Extremely motivated graduate seeking an opportunity to use my logical, analytical, and technical abilities to contribute to the organization which will help my career growth

PROFESSIONAL TRAINING

Design For Testability Training : VLSIGURU INSTITUTE — Jun 2025 – present

- Hands-on experience and good knowledge in scan insertion and scan compression.
- Good knowledge in fault modeling, fault simulation, and ATPG.
- Strong understanding of digital design concepts.
- Familiar with complete ASIC design flow and proficient in using GVIM for efficient code editing.
- Fundamental knowledge of programming language such as Linux.

PROJECTS (DFT)

MBIST and Scan Insertion in Ongoing Projects

Design (Communication Chip):
Working on small Hierarchical designs consisting of a Parent and multiple Child cores with flop count of ~4K. Performed MBIST Insertion, Scan Stitching and DRC Cleanup, EDT and OCC Insertion. Worked on ATPG Coverage analysis, Pattern generation and Serial & Parallel Scan pattern Simulation.

PROJECTS (B.TECH)

TITLE: ACCIDENT DETECTION AND NOTIFICATION SYSTEM

Description:

Designed and implemented an embedded accident detection system integrating multiple sensors (accelerometer, crash, alcohol, eye blink, ultrasonic) with microcontrollers (Arduino Uno, NodeMCU) for real-time monitoring and reporting. Developed and tested hardware–software interfaces, optimized signal acquisition, and implemented fault detection mechanisms to ensure reliable sensor data. Utilized ThingSpeak cloud and GPS for real-time location tracking and automated alert notifications.

1. Sensors continuously monitor vehicle movement and driver condition.

2. If abnormal conditions (crash, drowsiness, alcohol detection) are detected, system activates alerts.

3. GPS captures current location; Wi-Fi module sends data to ThingSpeak cloud.

TECHNICAL SKILLS

- **Design For Testability:** Scan Insertion, Scan Compression (EDT), ATPG, On-Chip Clock Controller, JTAG and Boundary Scan, Coverage Analysis, MBIST Insertion.
- **Digital Design:** Combinational Logic Design, Sequential Logic Design
- **Operating System:** Linux, Windows
- **Text Editors:** GVIM, Notepad
- **Tools and Technologies:** Mentor Graphics Tessent, Cygwin, QuestaSim, Design Compilers
- **MS Office:** Good working knowledge of Excel and Microsoft Word
- **Other Skills:** ASIC Flow, TCL, Communication Skills

CERTIFICATIONS

- **Design For Testability** - Issued by: VLSI Guru Institute Bengaluru

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EDUCATION

- **MVR College of Engineering and Technology** 2021 – 2025
  Bachelor's degree in Electronics and communication Engineering – 7.8 CGPA

- **Kamala – Junior College** 2019 – 2021
  Intermediate (10+2 class) – 7.2 CGPA

- **Sri Chaitanya High School** 2018 – 2019
  Secondary School (10^{th} class) – 9.5 CGPA

PERSONALITY TRAITS

- Adaptability
- Positive Attitude
- Time Management

DECLARATION

I hereby declare that the information provided above is true to the best of my knowledge. As a fresher, I am eager to apply my skills in VLSI and Design for Testability (DFT), adapt quickly to new technologies, and contribute to the growth and success of the organization.