Intel® Stratix® 10 Logic Array Blocks and Adaptive Logic Modules User Guide

UG-S10LAB
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Contents

1 Stratix® 10 LAB and ALM Overview

The logic array block (LAB) is composed of basic building blocks known as adaptive logic modules (ALMs). You can configure the LABs to implement logic functions, arithmetic functions, and register functions.

You can use a quarter of the available LABs in the Stratix® 10 devices as memory LABs (MLABs). Certain devices may have higher MLAB ratio.

The Quartus® Prime software and other supported third-party synthesis tools automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Related Links

HyperFlex Core Architecture, Stratix 10 Device Overview
    Provides more information about Hyper-Registers and the HyperFlex core architecture. Hyper-Registers are additional registers available in every interconnect routing segment throughout the core fabric, including the routing segments connected to the LAB inputs and outputs.

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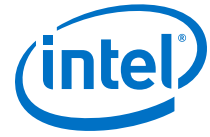
2 HyperFlex Register

The Stratix 10 device family introduces the HyperFlex™ core architecture. This architecture reduces the cost in your design by adding additional pipelining stages.

The Stratix 10 LAB contains HyperFlex registers and other features designed to facilitate retiming. HyperFlex registers are available in ALMs and carry chain. As shown in the Stratix 10 ALM Connection Details figure, the HyperFlex registers are located on the synchronous clear and clock enable inputs to increase or reduce effective path delay. All the HyperFlex registers can be enabled and are controlled by the Quartus Prime software during retiming.

3 Stratix 10 LAB and ALM Architecture and Features

The following sections describe the LAB and ALM for Stratix 10 devices.

3.1 LAB

The LABs are configurable logic blocks that consist of a group of logic resources. Each LAB contains dedicated logic for driving control signals to its ALMs. The MLAB is a superset of the LAB and includes all the LAB features. There are a total of 10 ALMs in each LAB, as shown in the LAB and MLAB Structure for Stratix 10 Devices figure.

Figure 1.   **Stratix 10 LAB Structure and Interconnects Overview**

This figure shows an overview of the Stratix 10 LAB and MLAB structure with the LAB interconnects.
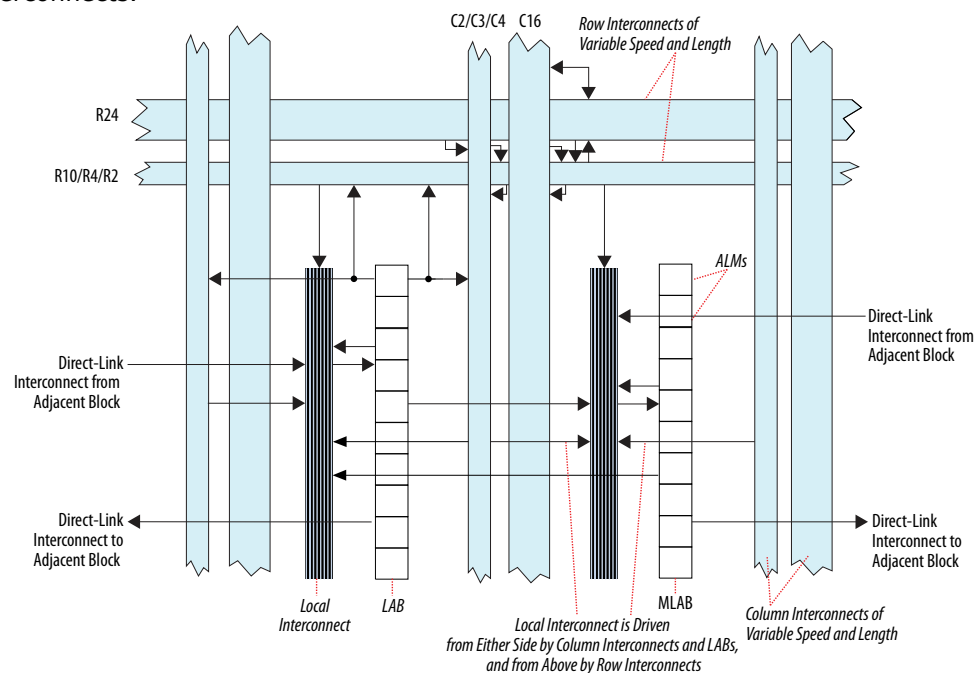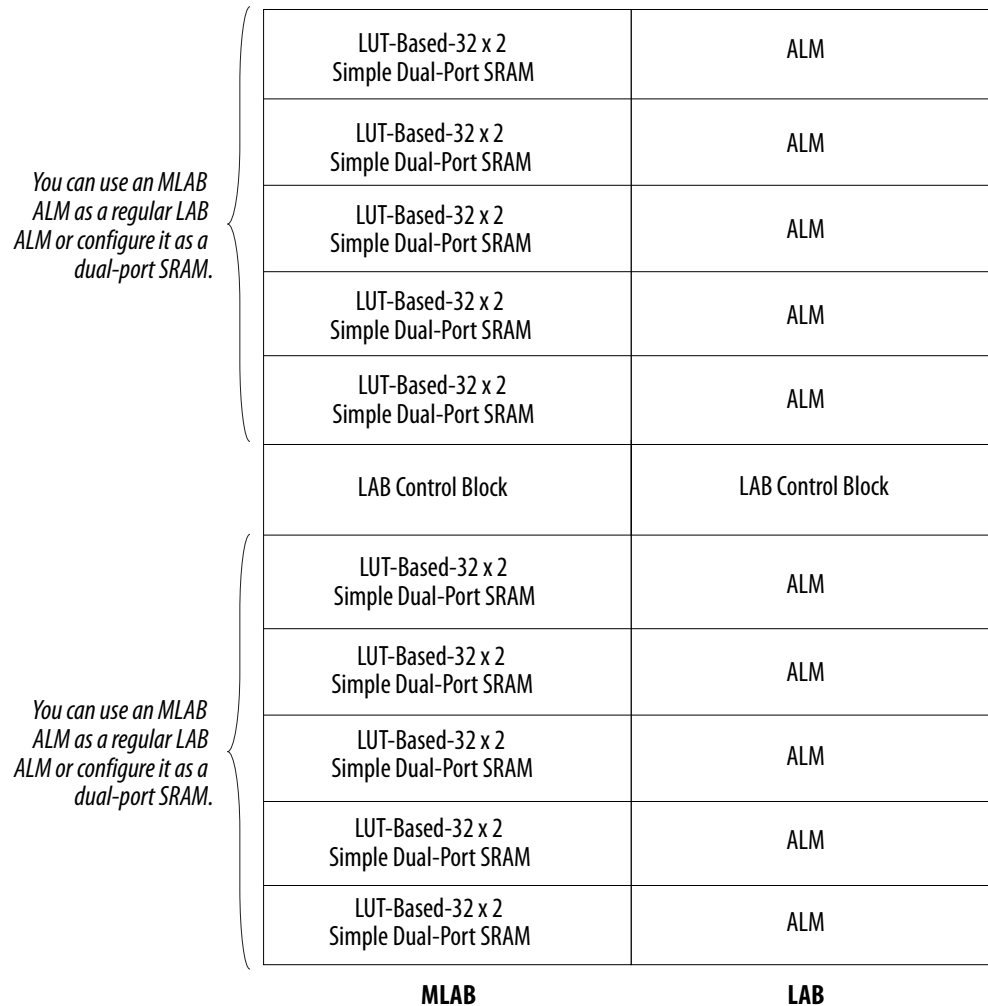

Related Links

3.1.1 MLAB

Each MLAB supports a maximum of 640 bits of simple dual-port SRAM. You can configure each ALM in an MLAB as a 32 (depth) x 2 (width) memory block, resulting in a configuration of 32 (depth) x 20 (width) simple dual-port SRAM block.

Figure 2. **Stratix 10 LAB and MLAB Structure**

You can use an MLAB ALM as a regular LAB ALM or configure it as a dual-port SRAM.

LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LAB Control Block	LAB Control Block
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
LUT-Based-32 x 2 Simple Dual-Port SRAM	ALM
MLAB	**LAB**

You can use an MLAB ALM as a regular LAB ALM or configure it as a dual-port SRAM.

3.1.2 Local and Direct Link Interconnects

Each LAB can drive out 40 ALM outputs. Two groups of 20 ALM outputs can drive the adjacent LABs directly through direct-link interconnects.

The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility.

The local interconnect drives the ALM inputs. ALM outputs, as well as column and row interconnects drive the local interconnect. Neighboring LABs, MLABs, M20K blocks, or digital signal processing (DSP) blocks from the left or right can also drive the LAB's local interconnect using the direct link connection.

Figure 3.   Stratix 10 LAB Local and Direct Link Interconnects
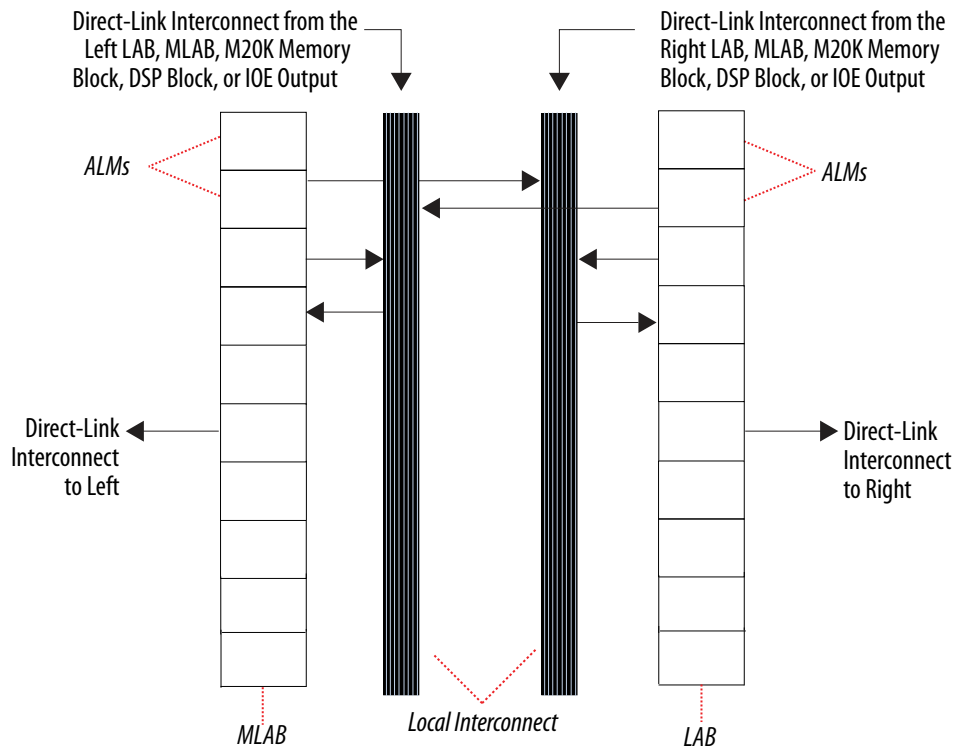
3.1.3 Carry Chain Interconnects

There is a dedicated carry chain path between the ALMs. Stratix 10 devices include an enhanced interconnect structure in LABs for routing carry chains for efficient arithmetic functions. These ALM-to-ALM connections bypass the local interconnect.

The HyperFlex registers are added to the carry chain to enable flexible retiming across a chain of LABs and the Quartus Prime Compiler automatically takes advantage of these resources to improve utilization and performance.

Figure 4.   Carry Chain Interconnects
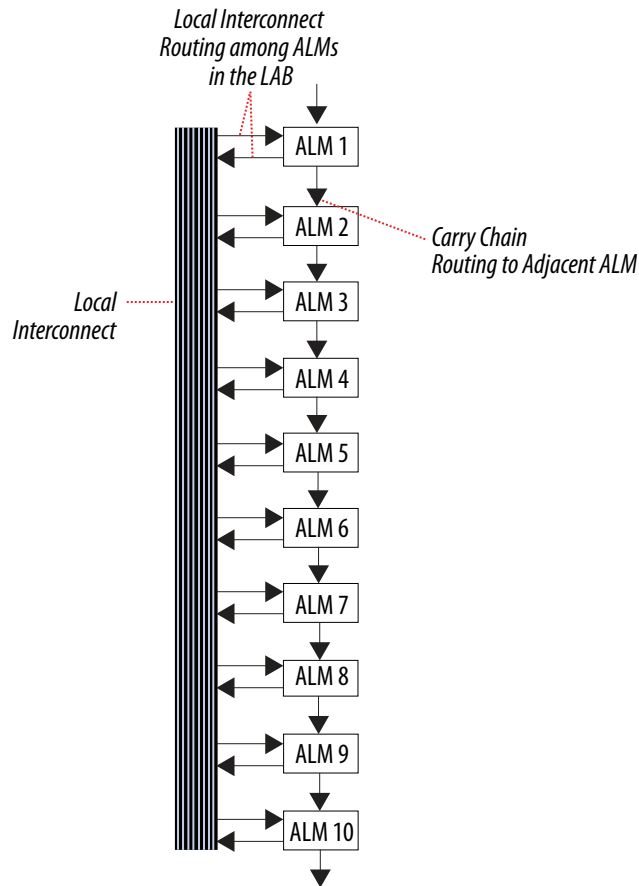
3.1.4 LAB Control Signals

Each LAB supports a single clock to drive the ALM registers in the LAB. The LAB supports two unique clock enable signals, as well as additional clear signals, for the ALM registers.

In addition, each LAB control block drives clock signals for the Hyper-Registers. There is a single clock for the Hyper-Registers on the local interconnect, and additional clocks for the Hyper-Registers located at the ALM inputs.

The LAB row clocks [5..0] and LAB local interconnects generate the LAB-wide control signals. A low skew clock network distributes global signals to the row clocks [5..0]. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for routing efficiency. The Quartus Prime Compiler automatically routes critical design paths on faster interconnects to improve design performance and optimizes the device resources.

3.1.4.1 Clear Logic Control

LAB-wide signals control the logic for the ALM register's clear signal. The ALM register directly supports both a synchronous and an asynchronous clear. Each LAB supports up to two synchronous clear signals and two asynchronous clear signals, provided that the total number of clear signals is no greater than three.

Stratix 10 devices provide a device-wide reset pin (DEV_CLRn) that resets all the registers in the device. You can enable the DEV_CLRn pin in the Quartus Prime software before compilation. The device-wide reset signal overrides all other control signals.

Figure 5. **Stratix 10 LAB-Wide Control Signals**
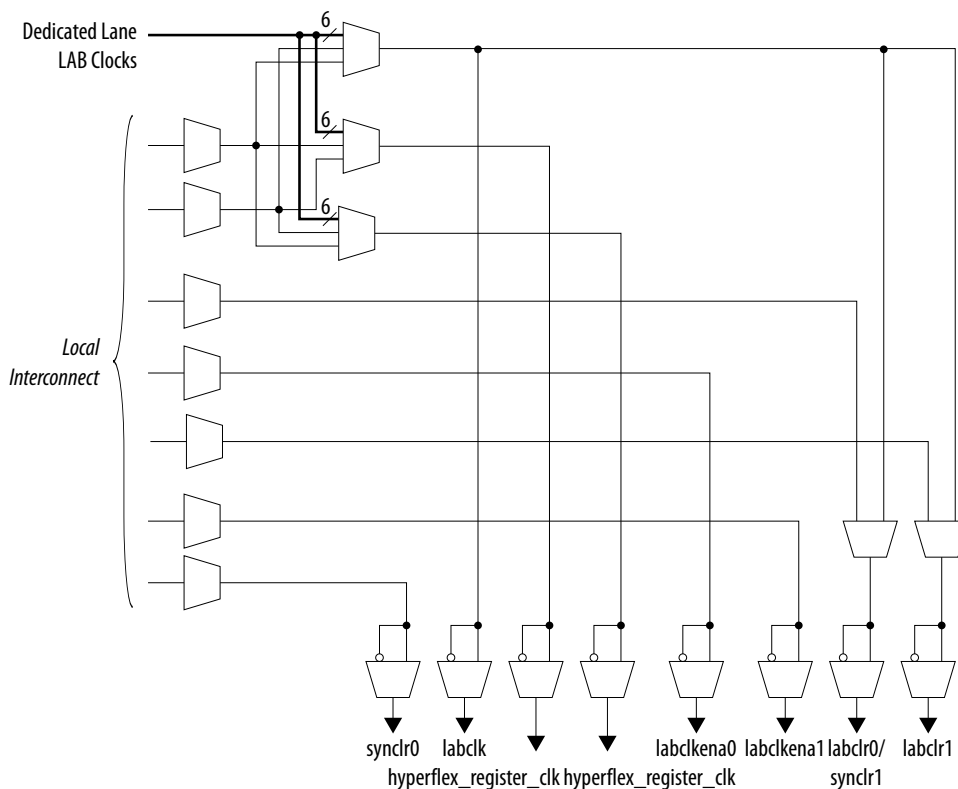
3.2 ALM

The following sections cover the ALM resources, ALM output, and ALM operating modes.

3.2.1 ALM Resources

Each ALM contains a variety of LUT-based resources that can be divided between two combinational adaptive LUTs (ALUTs), a two-bits full adder, and four registers.

With up to eight inputs for the two combinational ALUTs, one ALM can implement various combinations of two functions. This adaptability allows an ALM to be completely backward-compatible with four input LUT architectures. One ALM can also implement a subset of eight input functions.

One ALM contains four programmable registers. Each register has the following ports:

- Data in
- Data out
- Clock
- Clock enable
- Synchronous clear
- Asynchronous clear

Global signals, general-purpose I/O (GPIO) pins, or any internal logic can drive the clock enable signal, clock, and asynchronous or synchronous clear control signals of an ALM register. The clock enable signal has priority over synchronous reset signal.

For combinational functions, the registers are bypassed and the output of the look-up table (LUT) and adders drives directly to the outputs of an ALM.

Figure 6.   Stratix 10 ALM High-Level Block Diagram
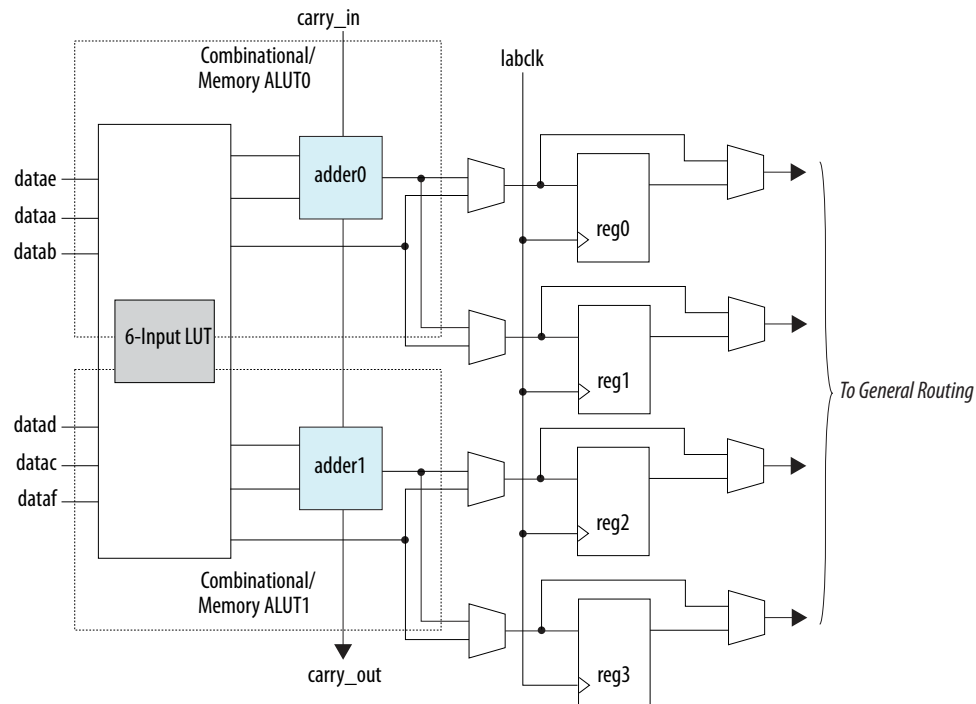
3.2.2 ALM Output

The general routing outputs in each ALM drive the local, row, and column routing resources. Four ALM outputs can drive column, row, or direct link routing connections.

The LUT, adder, or register output can drive the ALM outputs. Both the LUT or adder and the ALM register can drive out of the ALM simultaneously.

Register packing improves device utilization by allowing unrelated register and combinational logic to be packed into a single ALM. Another mechanism to improve fitting is to allow the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

The following figure shows the Stratix 10 ALM connectivity. In the Quartus Prime Resource Property Editor, the entire ALM connection is simplified. Some routing will be routed internally by the Quartus Prime software.

Figure 7.   Stratix 10 ALM Connection Details
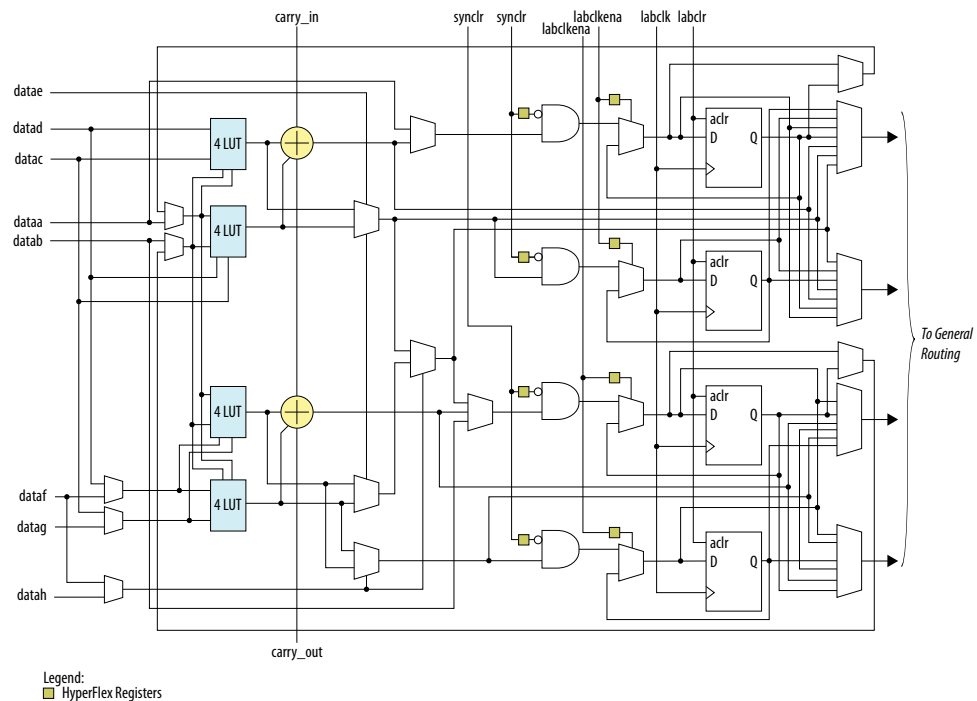
3.2.3 ALM Operating Modes

The Stratix 10 ALM operates in any of the following modes:

*   Normal mode
*   Extended LUT mode
*   Arithmetic mode

3.2.3.1 Normal Mode

Normal mode allows two functions to be implemented in one Stratix 10 ALM, or a single function of up to six inputs.

Up to eight data inputs from the LAB local interconnect are inputs to the combinational logic.

The ALM can support certain combinations of completely independent functions and various combinations of functions that have common inputs. The Quartus Prime Compiler automatically selects the inputs to the LUT. ALMs in normal mode support register packing.

The following figure shows a combination of different input connections for the LUT mode. In your design, the Quartus Prime software may assign different input namings during compilation.

Figure 8.   ALM in Normal Mode
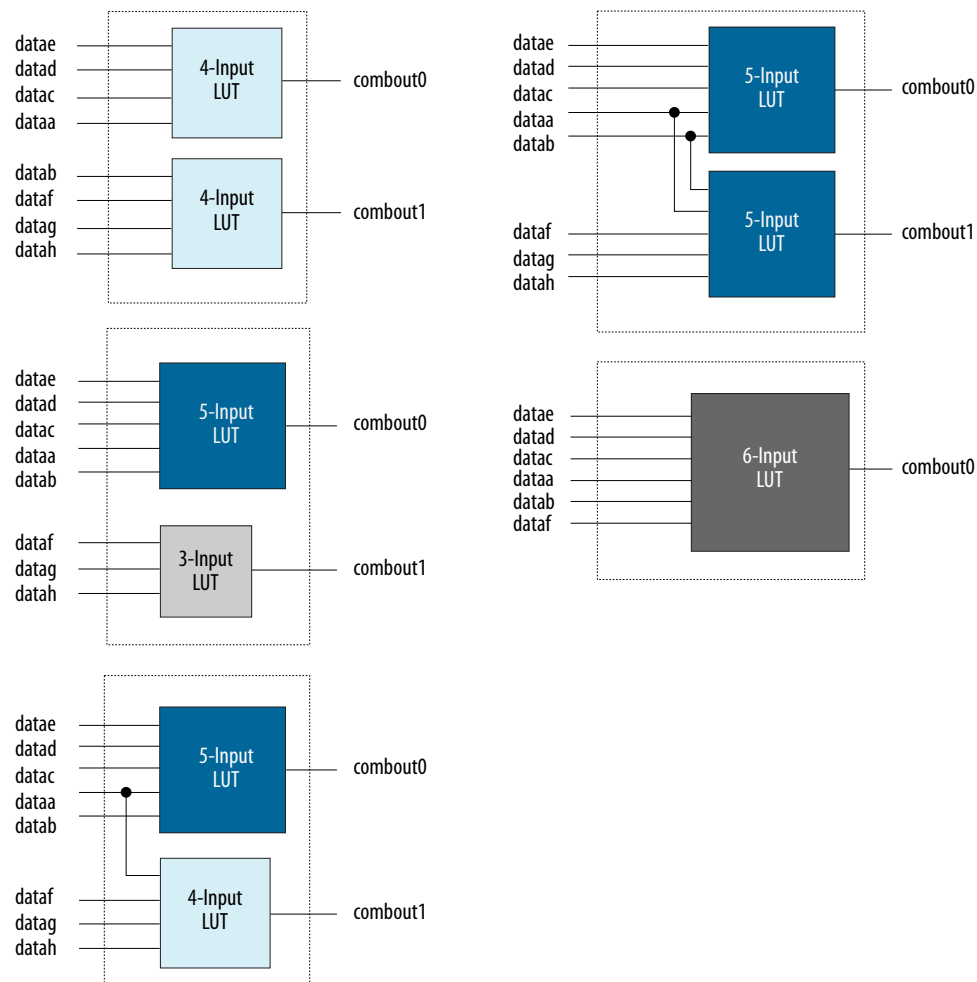
Combinations of functions with fewer inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported.

- 4 and 3
- 3 and 3
- 3 and 2
- 5 and 2

For the packing of two 5-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataa` and `datab`. The combination of a 4-input function with a 5-input function requires one common input (either `dataa` or `datab`).

In a sparsely used device, functions that could be placed in one ALM may be implemented in separate ALMs by the Quartus Prime software to achieve the best possible performance. As a device begins to fill up, the Quartus Prime software automatically uses the full potential of the Stratix 10 ALM. The Quartus Prime Compiler automatically searches for functions using common inputs or completely independent functions to be placed in one ALM to make efficient use of device resources. In addition, you can manually control resource use by setting location assignments.

Figure 9. **3-Input LUT Mode Function in Normal Mode**

`dataa` and `datab` are available for register packing.
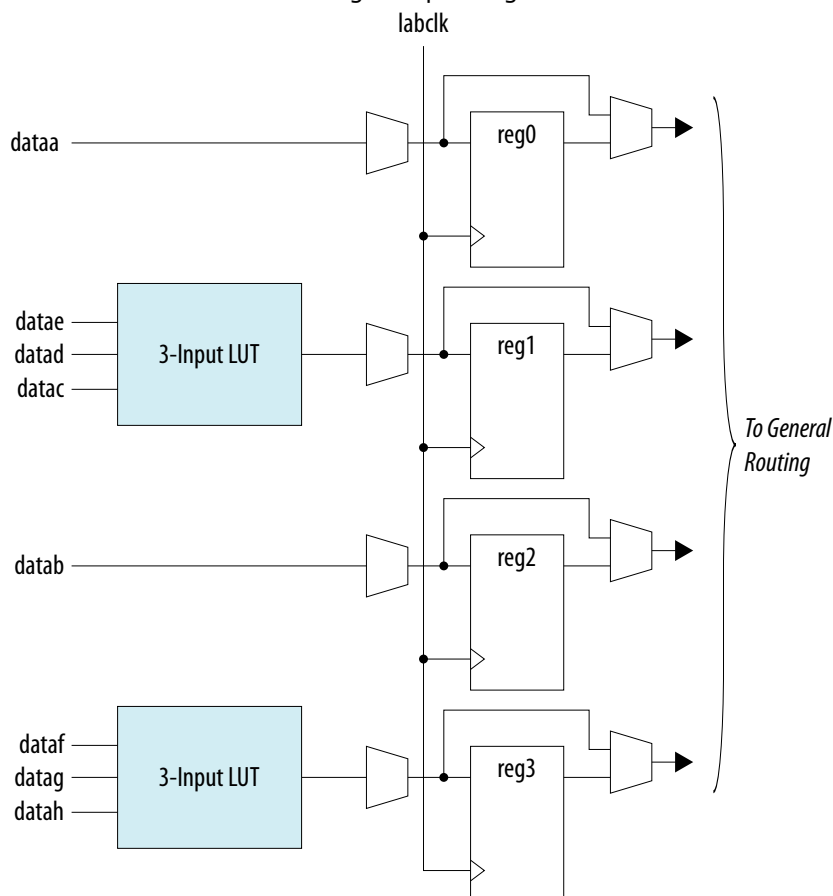
Note: The 3-LUT atom's inputs are named as `dataa`, `datab`, and `datac` regardless of which physical ALM data input that the Quartus Prime software selects to map it to.

You can implement any three to six input function using the following inputs:

- `datae`
- `datad`
- `datac`
- `datag`
- `datah`
- `dataf`
- `dataa` and `datab`—whereby `dataa` and `datab` are shared across both LUTs to provide flexibility to implement a different function in each LUT.

Both `dataa` and `datab` inputs support the register packing feature. If you enable the register packing feature, both `dataa` and `datab` inputs or either one of the inputs bypass the LUT and directly feed into the register, depending on the packed register mode used. For Stratix 10 devices, the following types of packed register modes are supported:

- 5-input LUT with 1 packed register path
- Two 3-input LUTs with 2 packed register paths

The 3-input LUT with 2 packed register paths is illustrated in the 3-Input LUT Mode Function in Normal Mode figure. For Stratix 10 devices, the 6-input LUT mode does not support the register packing feature.

3.2.3.2 Extended LUT Mode

Figure 10. Supported 8-Input Functions in the Extended LUT Mode
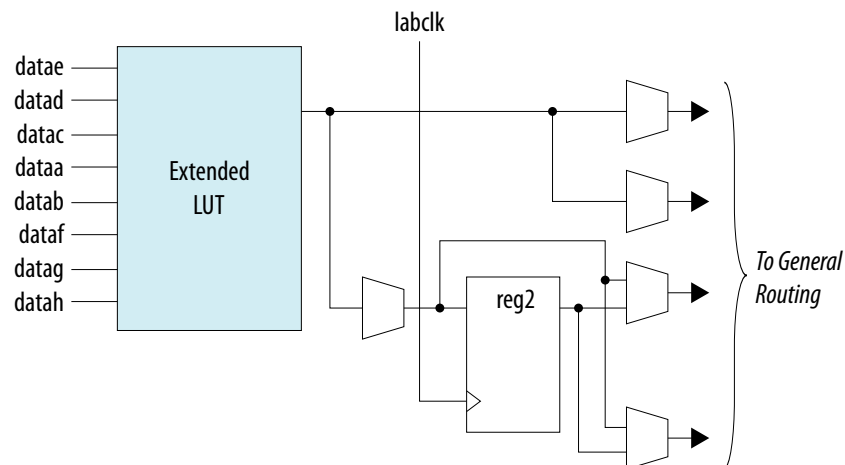
Certain 8-input functions can be implemented in a single ALM using all the LUT inputs:

- `datae`
- `datad`
- `datac`
- `dataa`
- `datab`
- `dataf`
- `datag`
- `datah`

In the 8-input extended LUT mode, the packed register mode is supported, provided that the packed register shares a `dataa` or `datab` input with the 8-input LUT.
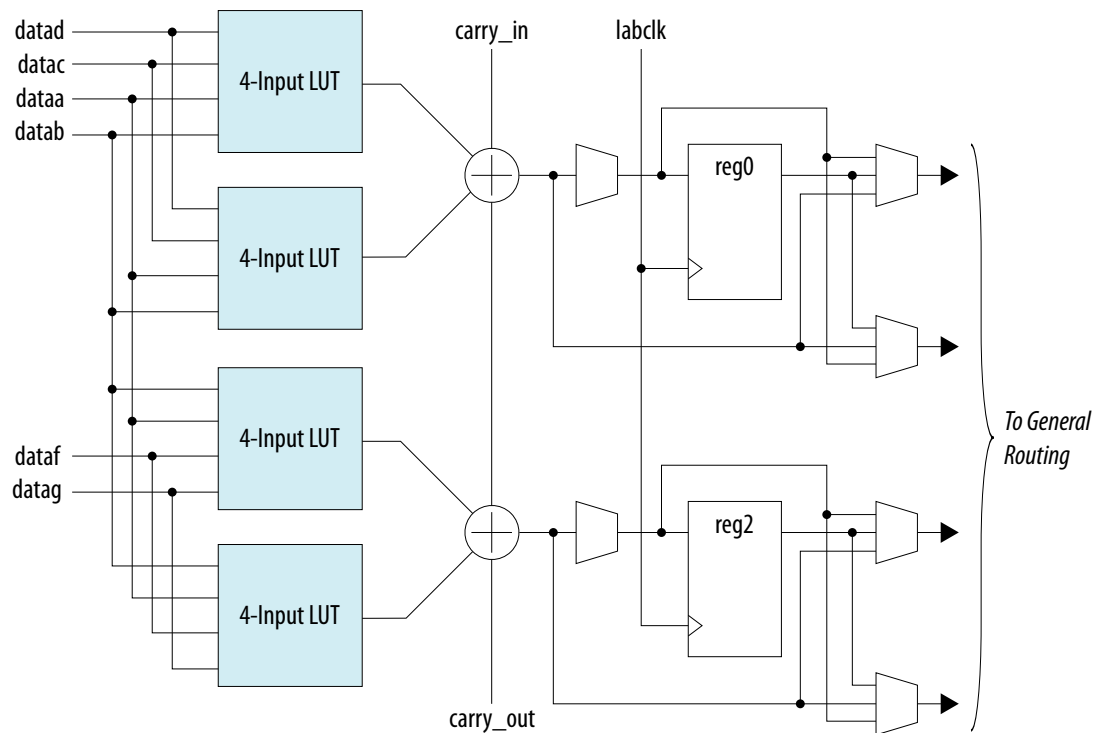
3.2.3.3 Arithmetic Mode

The ALM in arithmetic mode uses two sets of two 4-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to perform pre-adder logic. Therefore, each adder can add the output of two 4-input functions.

Arithmetic mode also offers clock enable, counter enable, synchronous up and down control, add and subtract control, and synchronous clear.

The clear and clock enable options are LAB-wide signals that affect all registers in the LAB. You can individually disable or enable these signals for each register. The Quartus Prime software automatically places any registers that are not used by the counter into other LABs.

Figure 11.   Stratix 10 ALM in Arithmetic Mode

3.2.3.3.1 Carry Chain

The carry chain provides a fast carry function between the dedicated adders in the arithmetic mode.

The 2-bit carry select feature in Stratix 10 devices splits the propagation delay of carry chains with the ALM. Carry chains can begin in either the first ALM or the sixth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only use the bottom half of the LAB before connecting to the next LAB. You can use the available top half of the ALMs in the LAB to implement narrower fan-in functions in the normal

mode. Carry chains that use the bottom five ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. The behavior is the same for both the LAB and the MLAB columns.

The Quartus Prime Compiler creates carry chains longer than 20 ALMs (10 ALMs in arithmetic) by linking LABs together. For an enhanced fitting, a long carry chain runs vertically, allowing fast horizontal connections to the TriMatrix memory and DSP blocks.
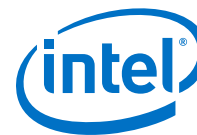
4 Document Revision History for Stratix 10 LAB and ALM User Guide

Date	Version	Changes
October 2016	2016.10.31	Initial release.

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