Encoder for (7,4) Cyclic Codes

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***Abstract*—This paper presents (7,4) Cyclic code Encoder.The encoder is implemented using a linear feedback shift register.The encoder accepts message bits and adds redundancy according to the feedback polynomial of LFSR.This encoder acts as a channel encoder in transmitter part of a communication system.**

I. Introduction

The encoding procedure for an (n,k) cyclic code in systematic form involves three steps:

- Multiplication of the message polynomial m(X) by X^{n-k},
- Division of $X^{n-k}m(X)$ by the generator polynomial g(X) to obtain the remainder b(X), and
- Addition of b(X) to $X^{n-k}m(X)$ to form the desired code polynomial

These three steps can be implemented by means of the encoder consisting of a linear feedback shift register with (n-k)stages. The boxes in the figure represent flip-flops, or unit-delay elements. The flip-flop is a device that resides in one of two possible states denoted by 0 and 1. An external clock controls the operation of all the flip-flops. Every time the clock ticks, the contents of the flip-flops (initially set to the state 0) are shifted out in the direction of the arrows. In addition to the flip-flops, the encoder of fig.1 includes a second set of logic elements, namely adders, which compute the modulo-2 sums of their respective inputs. Finally, the multipliers multiply their respective inputs by the associated coefficients. In particular, if the coefficient g_i=1, the multiplier is just a direct "connection." If, on the other hand, the coefficient g_i=0 , the multiplier is "no connection."

II. Design Implementation

Here the (7,4) cyclic Hamming code generated by the polynomial .

$$g(X) = 1 + X + X^3 \tag{1}$$

To illustrate the operation of this encoder, consider the message sequence (1001). The contents of the shift register are modified by the incoming message bits as in Table below. After four shifts, the contents of the shift register, and therefore the parity-check bits, are (011). Accordingly, appending these parity-check bits to the message bits (1001), we get the codeword (0111001);

III. Simulation

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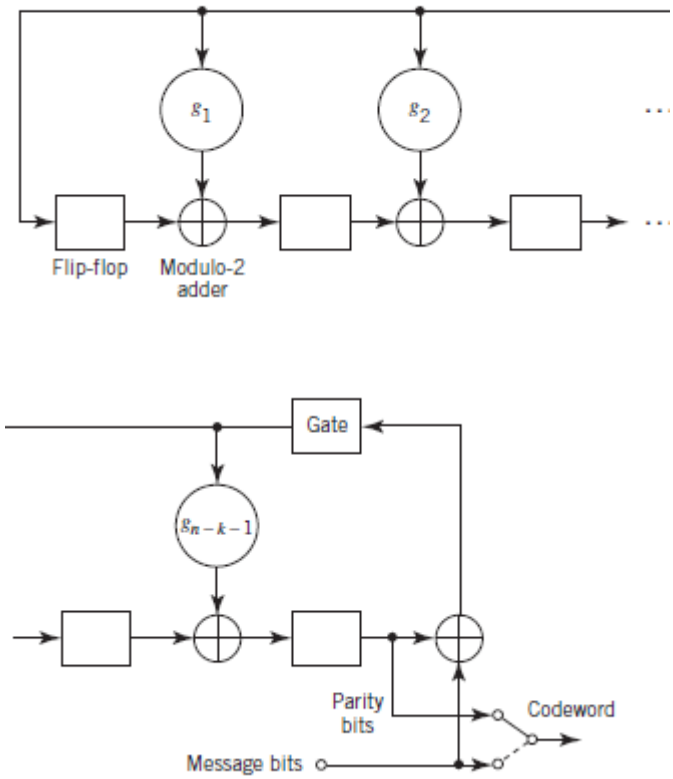

Fig. 1. Encoder for an(n,k) cyclic code

Shift	Input bit	Contents of shift register
		000 (initial state)
1	1	110
2	0	011
3	0	111
4	1	011

Fig. 2. Contents on the Register Encoder for Message Sequence(1001)

REFERENCES

[1] Simon Haykin ”Digital Communications” ,Wiley,2015

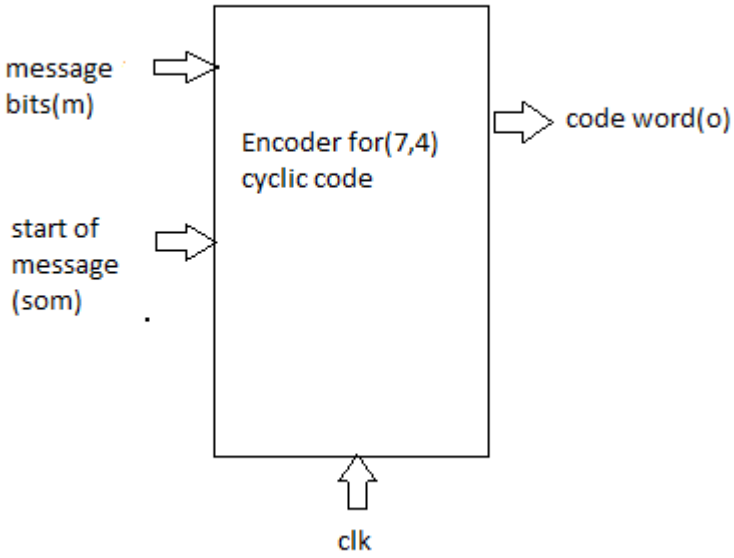

Fig. 3. Design Module

Fig. 4. Simulation for message bits(1001,1101)

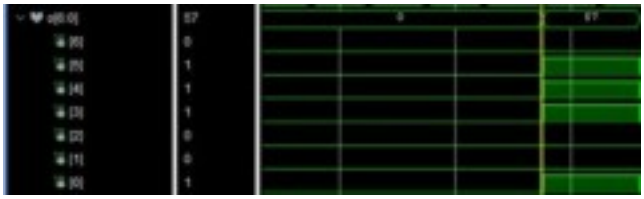

Fig. 5. zoomed out output for message bit(1001)