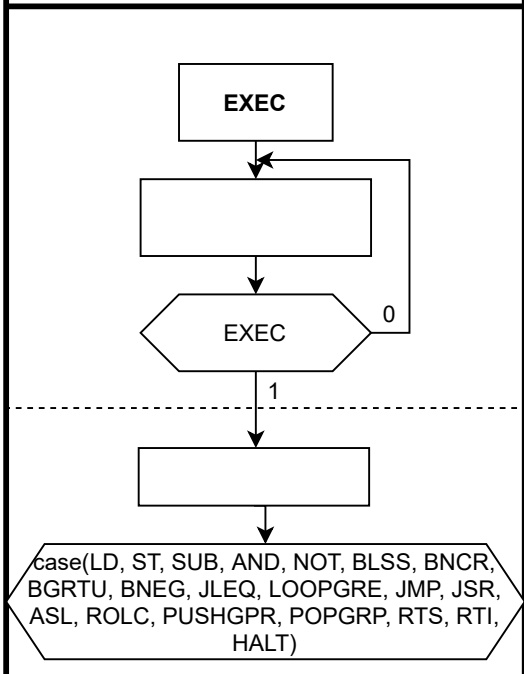
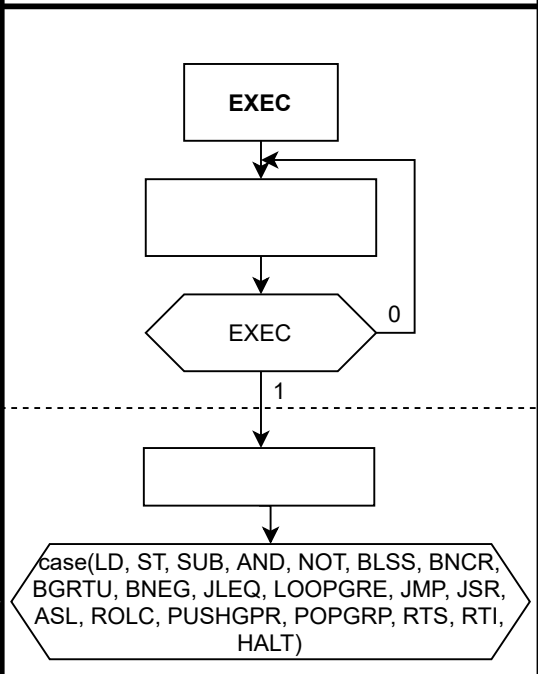
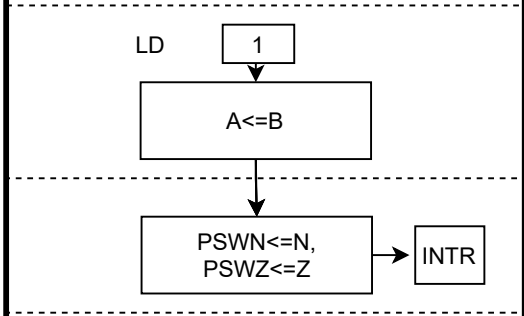
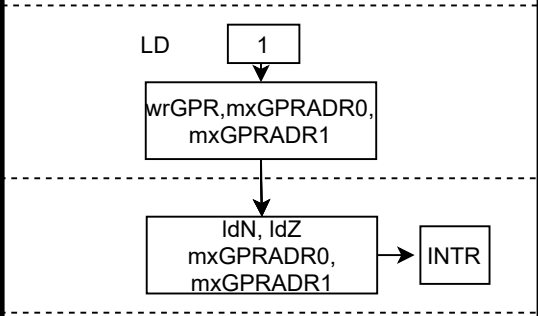
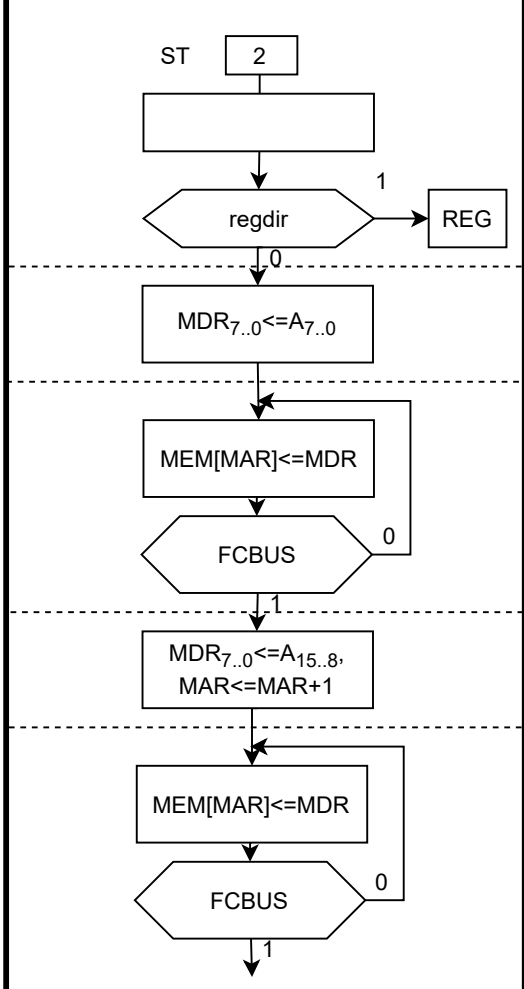
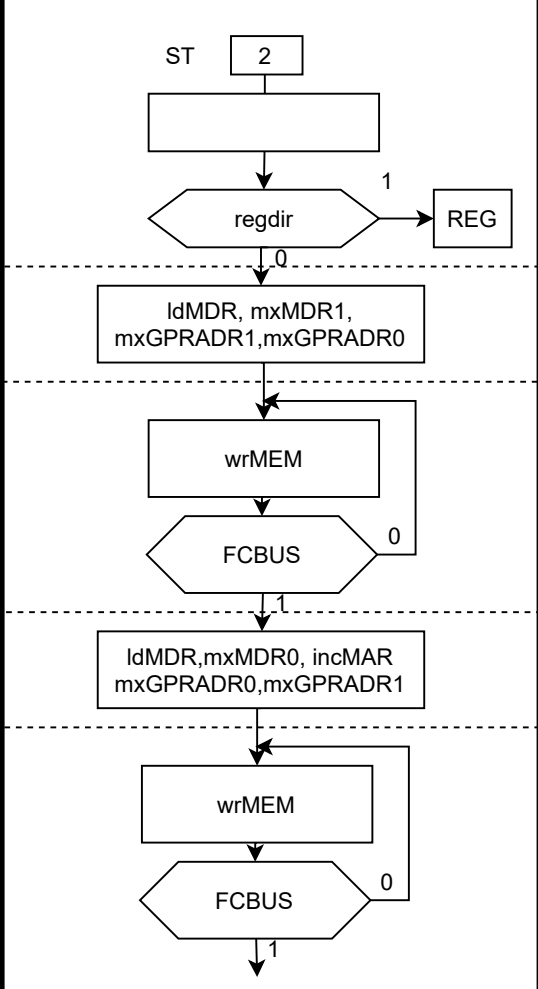
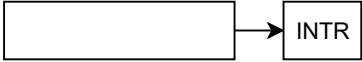
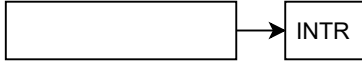

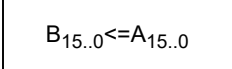

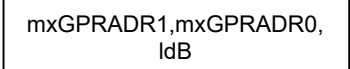
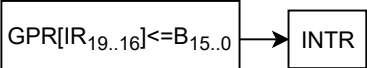
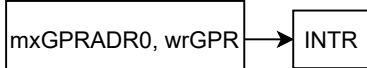

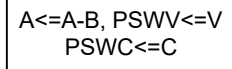

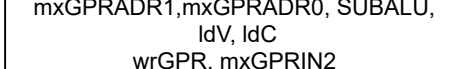
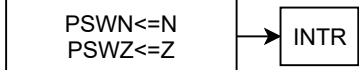


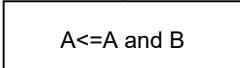

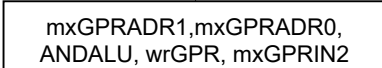
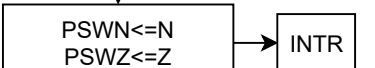


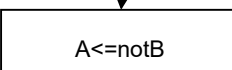

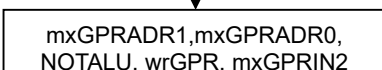
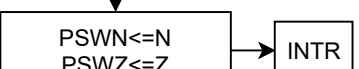
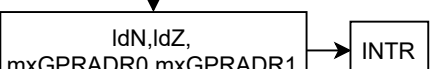
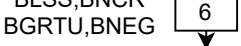
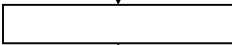
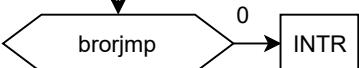
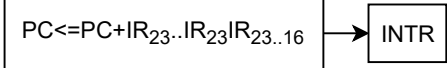
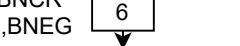
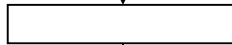
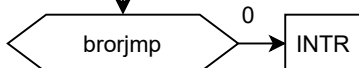

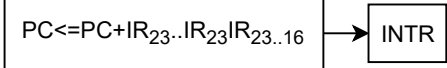


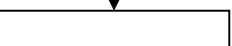
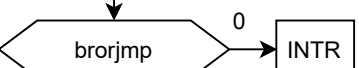
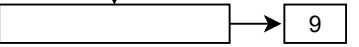

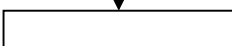
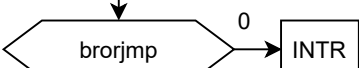
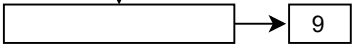
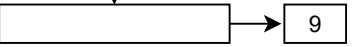
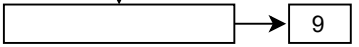


<div>Дијаграм тока микрооперација</div>	<div>Дијаграм тока управљачких сигнала</div>	<div>Секвенца управљачких сигнала</div>
		<div>step00 => br(if notEXEC then step00)</div> <div>step01 => br(case(LD, ST, SUB, AND, NOT, BLSS, BNCR, BGRTU, BNEG, JLEQ, LOOPGRE, JMP, JSR, ASL, ROLC, PUSHGPR, POPGRP, RTS, RTI, HALT) then (LD,step02),(ST,step04),(SUB,step0C),(AND,step0E),(NOT,step10),(BLSS,BNCR,BGRTU,BNEG, step12),(JLEQ, step14),(LOOPGRE, step16),(JMP, step1B),(JSR, step1C),(ASL,ROLC,step25),(RTS,step29),(RTI, step2F),(PUSHGPR, step3C),(POPGPR,step47),(HALT,step50))</div>
<div>LD 1</div> 	<div>LD 1</div> 	<div>step02 => wrGPR,mxGPRADR0, mxGPRADR1</div> <div>step03 => ldN, ldZ mxGPRADR0, mxGPRADR1 br step51</div>
<div>ST 2</div> 	<div>ST 2</div> 	<div>step04 => br(if regdir then step0A)</div> <div>step05 => ldMDR, mxMDR1, mxGPRADR1, mxGPRADR0</div> <div>step06 => wrMEM, br(if notFCBUS then step06)</div> <div>step07 => ldMDR, mxMDR0, incMAR mxGPRADR0, mxGPRADR1</div> <div>step08 => wrMEM, br(if notFCBUS then step08)</div>
<div>Име, презиме и број индекса</div> <div>Иван Цветић 2019/0183</div> <div>Славица Митровић 2019/0324</div>	<div>Потпис</div>	<div>Назив: Основи рачунарске технике 2</div> <div>Датум: 27.02.2021.</div> <div>Задатак 19: Фаза извршавања операција, страна 1/7</div>

Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step09 => br step51
 	 	step0A => mxGPRADR1, mxGPRADR0, IdB
		step0B => mxGPRADR0, wrGPR, br step51
 	 	step0C => mxGPRADR1, mxGPRADR0, SUBALU, IdV, IdC, wrGPR, mxGPRIN2
		step0D => IdN, IdZ, mxGPRADR0, mxGPRADR1, br step51
 	 	step0E => mxGPRADR1, mxGPRADR0, ANDALU, wrGPR, mxGPRIN2
		step0F => IdN, IdZ, mxGPRADR0, mxGPRADR1, br step51
 	 	step10 => mxGPRADR1, mxGPRADR0, NOTALU, wrGPR, mxGPRIN2
		step11 => IdN, IdZ, mxGPRADR0, mxGPRADR1, br step51
   	   	step12 => br(if notbrorjmp then step51)
		step13 => IdPC, mxGPRIN0, br step51
   	   	step14 => br(if notbrorjmp then step51)
		step15 => br step1B

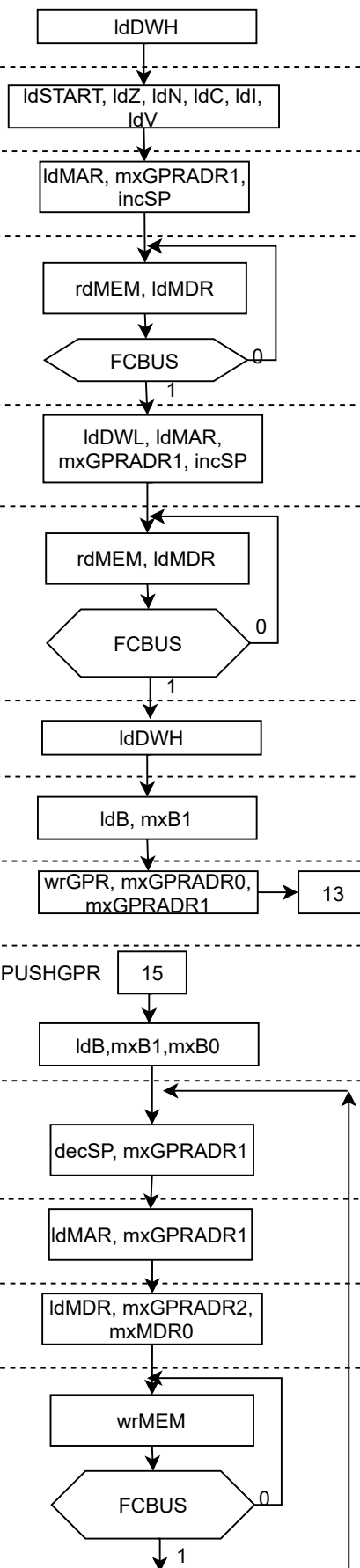
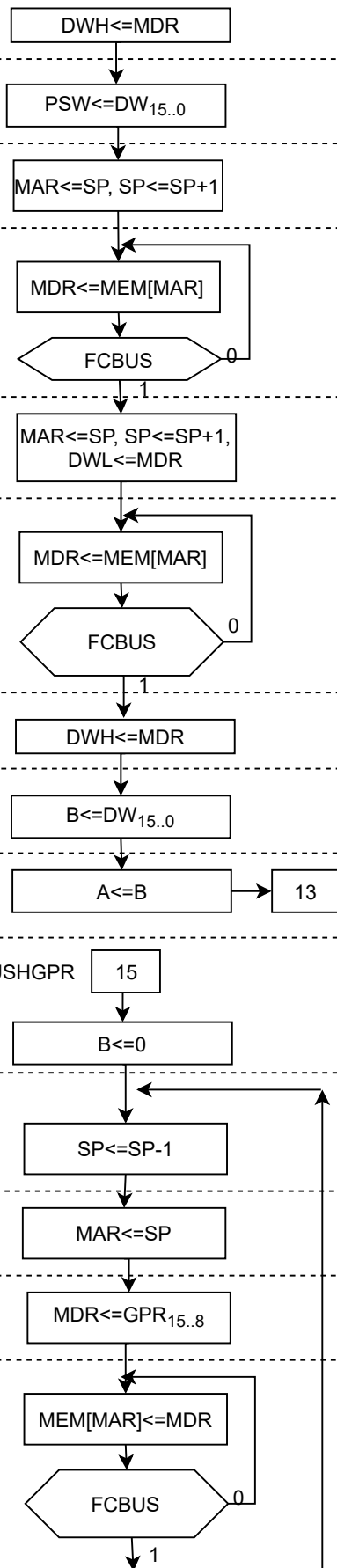
Дијаграм тока микрооперација		Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
<p>LOOPGRE 8</p>		<p>step16 => br(if notbrorjmp then step51)</p>	
		<p>step17 => ldB,mxGPRADR1,mxGPRADR0</p>	
		<p>step18 => decB, ldC</p>	
		<p>step19 => mxGPRADR0,mxGPRADR1 wrGPR,ldV</p>	
		<p>step1A => ldN,ldZ, mxGPRADR0,mxGPRADR1 (br step1B)</p>	
<p>JMP 9</p>		<p>step1B => ldPC, mxGPRIN1, br step51</p>	
<p>JSR 10</p>		<p>step1C => decSP,mxGPRADR1</p>	
		<p>step1D => ldMDR, mxMDR0</p>	
		<p>step1E => ldMAR, mxGPRADR1</p>	
		<p>step1F => wrMEM, br (if notFCBUS then step1F)</p>	
		<p>step20 => decSP,mxGPRADR1</p>	
		<p>step21 => ldMDR, mxMDR1</p>	
		<p>step22 => ldMAR,mxGPRADR1</p>	
		<p>step23 => wrMEM, br (if notFCBUS then step23)</p>	
		<p>step24 => ldPC, mxGPRIN1, br step51</p>	

<div>Дијаграм тока микрооперација</div>	<div>Дијаграм тока управљачких сигнала</div>	<div>Секвенца управљачких сигнала</div>
<div>ASL, ROLC 11,12</div> <div>B<=A</div> <div>B_{15..0}<=B_{14..0}, PSWC<=B₁₅</div> <div>A<=B</div> <div>PSWN<=N, PSWZ<=Z → INTR</div>	<div>ASL, ROLC 11,12</div> <div>ldB,mxGPRADR0,mxGPRADR1</div> <div>slB, ldC</div> <div>wrGPR,mxGPRADR0,mxGPRADR1</div> <div>ldN,ldZ mxGPRADR0,mxGPRADR1 → INTR</div>	<div>step25 => ldB,mxGPRADR0,mxGPRADR1</div> <div>step26 => slB, ldC</div> <div>step27 => wrGPR,mxGPRADR0,mxGPRADR1</div> <div>step28 => ldN,ldZ mxGPRADR0,mxGPRADR1, br step51</div>
<div>RTS 13</div> <div>MAR<=SP, SP<=SP+1</div> <div>MDR<=MEM[MAR]</div> <div>FCBUS 0</div> <div>MAR<=SP, SP<=SP+1, DWL<=MDR</div> <div>MDR<=MEM[MAR]</div> <div>FCBUS 0</div> <div>DWH<=MDR</div> <div>PC<=DW_{15..0} → INTR</div>	<div>RTS 13</div> <div>ldMAR, mxGPRADR1 incSP</div> <div>rdMEM, ldMDR</div> <div>FCBUS 0</div> <div>ldDWL, ldMAR, mxGPRADR1, incSP</div> <div>rdMEM, ldMDR</div> <div>FCBUS 0</div> <div>ldDWH</div> <div>ldPC, mxGPRIN0, mxGPRIN1 → INTR</div>	<div>step29 => ldMAR, mxGPRADR1 incSP</div> <div>step2A => rdMEM, ldMDR, br(if notFCBUS then step2A)</div> <div>step2B => ldDWL, ldMAR, mxGPRADR1, incSP</div> <div>step2C => rdMEM, ldMDR, br(if notFCBUS then step2C)</div> <div>step2D => ldDWH</div> <div>step2E => ldPC, mxGPRIN0, mxGPRIN1 br step51</div>
<div>RTI 14</div> <div>MAR<=SP, SP<=SP+1</div> <div>MDR<=MEM[MAR]</div> <div>FCBUS 0</div> <div>MAR<=SP, SP<=SP+1, DWL<=MDR</div> <div>MDR<=MEM[MAR]</div> <div>FCBUS 0</div>	<div>RTI 14</div> <div>ldMAR,mxGPRADR1, incSP</div> <div>rdMEM, ldMDR</div> <div>FCBUS 0</div> <div>ldDWL, ldMAR, mxGPRADR1, incSP</div> <div>rdMEM, ldMDR</div> <div>FCBUS 0</div>	<div>step2F => ldMAR,mxGPRADR1, incSP</div> <div>step30 => rdMEM, ldMDR, br(if notFCBUS then step30)</div> <div>step31 => ldDWL, ldMAR, mxGPRADR1, incSP</div> <div>step32 => rdMEM, ldMDR, br(if notFCBUS then step32)</div>
<div>Име, презиме и број индекса</div> <div>Иван Цветић 2019/0183</div> <div>Славица Митровић 2019/0324</div>	<div>Потпис</div>	<div>Назив: Основи рачунарске технике 2</div> <div>Датум: 27.02.2021.</div> <div>Задатак 19: Фаза извршавања операција, страна 4/7</div>

Дијаграм тока микрооперација

Дијаграм тока управљачких сигнала

Секвенца управљачких сигнала



step33 => IdDWH

step34 => IdSTART, IdZ, IdN, IdC, IdI, IdV

step35 => IdMAR, mxGPRADR1, incSP

step36 => rdMEM, IdMDR, br (if notFCBUS then step36)

step37 => IdDWL, IdMAR, mxGPRADR1, incSP

step38 => rdMEM, IdMDR, br (if notFCBUS then step38)

step39 => IdDWH

step3A => IdB, mxB1

step3B => wrGPR, mxGPRADR0, mxGPRADR1, br step29

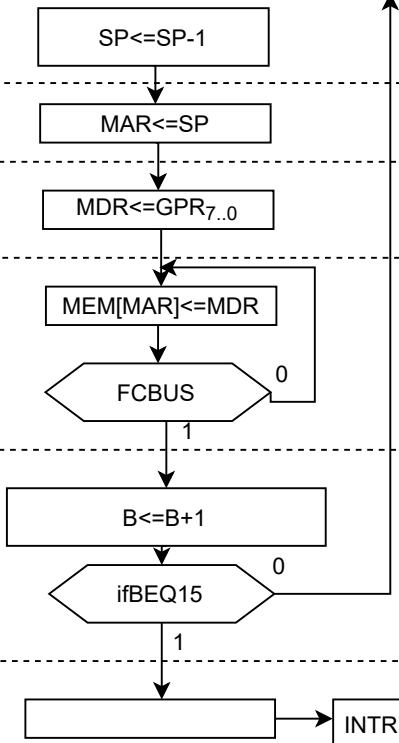
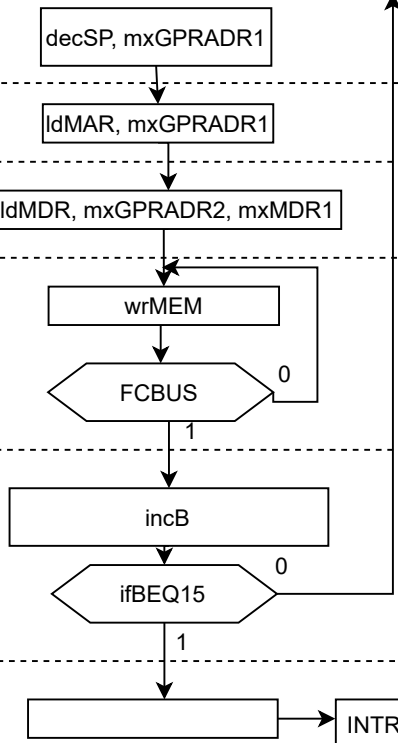
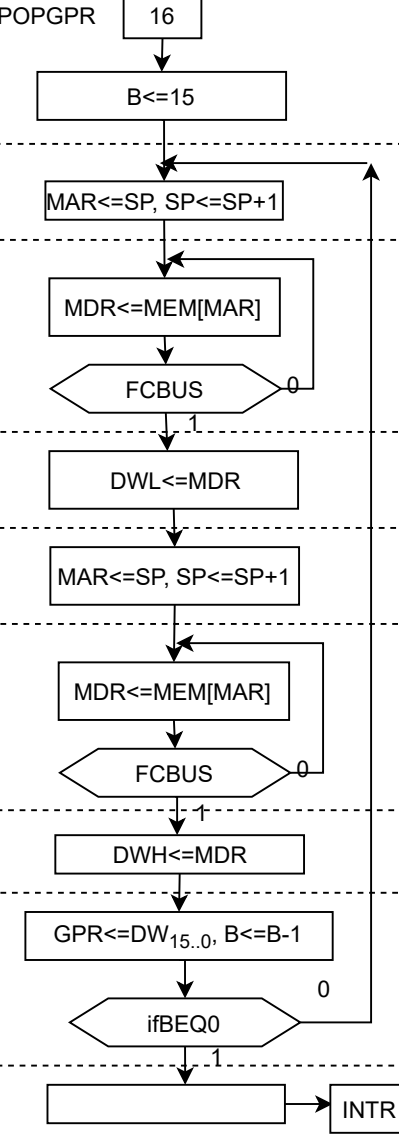
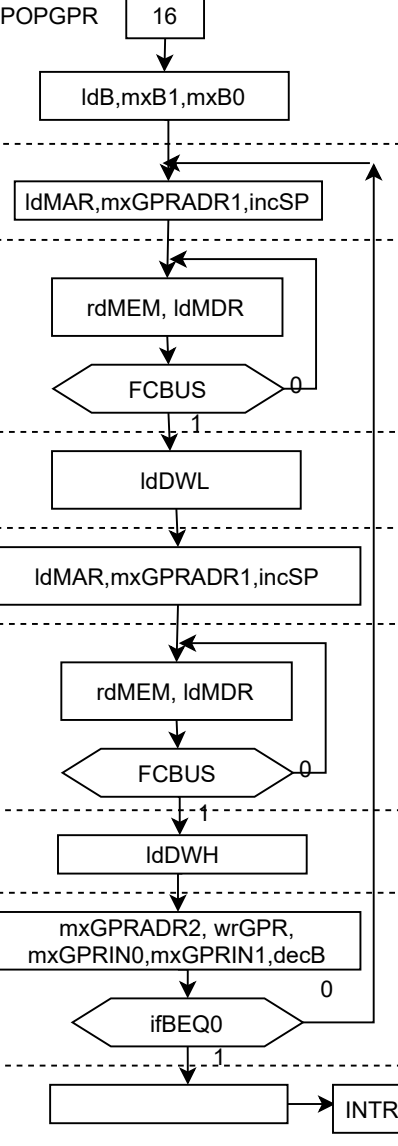
step3C => IdB, mxB1, mxB0

step3D => decSP, mxGPRADR1

step3E => IdMAR, mxGPRADR1

step3F => IdMDR, mxGPRADR2, mxMDR0

step40 => wrMEM, br (if notFCBUS then step40)

Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
 <pre> graph TD A[SP <= SP-1] --> B[MAR <= SP] B --> C[MDR <= GPR7..0] C --> D[MEM[MAR] <= MDR] D --> E{FCBUS} E -- 0 --> A E -- 1 --> F[B <= B+1] F --> G{ifBEQ15} G -- 0 --> A G -- 1 --> H[] H --> I[INTR] </pre>	 <pre> graph TD A[decSP, mxGPRADR1] --> B[ldMAR, mxGPRADR1] B --> C[ldMDR, mxGPRADR2, mxMDR1] C --> D[wrMEM] D --> E{FCBUS} E -- 0 --> A E -- 1 --> F[incB] F --> G{ifBEQ15} G -- 0 --> A G -- 1 --> H[] H --> I[INTR] </pre>	<div>step41 => decSP, mxGPRADR1</div> <div>step42 => ldMAR, mxGPRADR1</div> <div>step43 => ldMDR, mxGPRADR2, mxMDR1</div> <div>step44 => wrMEM, br(if notFCBUS then step44)</div> <div>step45 => incB br(if notifBEQ15 then step3D)</div> <div>step46 => br step51</div>
 <pre> graph TD A[POPGPR 16] --> B[B <= 15] B --> C[MAR <= SP, SP <= SP+1] C --> D[MDR <= MEM[MAR]] D --> E{FCBUS} E -- 0 --> B E -- 1 --> F[DWL <= MDR] F --> G[MAR <= SP, SP <= SP+1] G --> H[MDR <= MEM[MAR]] H --> I{FCBUS} I -- 0 --> B I -- 1 --> J[DWH <= MDR] J --> K[GPR <= DW15..0, B <= B-1] K --> L{ifBEQ0} L -- 0 --> B L -- 1 --> M[] M --> N[INTR] </pre>	 <pre> graph TD A[POPGPR 16] --> B[ldB, mxB1, mxB0] B --> C[ldMAR, mxGPRADR1, incSP] C --> D[rdMEM, ldMDR] D --> E{FCBUS} E -- 0 --> B E -- 1 --> F[ldDWL] F --> G[ldMAR, mxGPRADR1, incSP] G --> H[rdMEM, ldMDR] H --> I{FCBUS} I -- 0 --> B I -- 1 --> J[ldDWH] J --> K[mxGPRADR2, wrGPR, mxGPRIN0, mxGPRIN1, decB] K --> L{ifBEQ0} L -- 0 --> B L -- 1 --> M[] M --> N[INTR] </pre>	<div>step47 => ldB, mxB1, mxB0</div> <div>step48 => ldMAR, mxGPRADR1, incSP</div> <div>step49 => rdMEM, ldMDR, br(if notFCBUS then step49)</div> <div>step4A => ldDWL</div> <div>step4B => ldMAR, mxGPRADR1, incSP</div> <div>step4C => rdMEM, ldMDR, br(if notFCBUS then step4C)</div> <div>step4D => ldDWH</div> <div>step4E => mxGPRADR2, wrGPR, mxGPRIN0, mxGPRIN1, decB, br(if notifBEQ0 then step48)</div> <div>step4F => br step4A</div>

Дијаграм тока микрооперација		Дијаграм тока управљачких сигнала		Секвенца управљачких сигнала	
<div>HALT<div>17</div><div>PSWSTART<=0</div><div>INTR</div></div> <div>INTR<div>INTR<=1 EXEC<=0</div><div>EXEC</div></div>		<div>HALT<div>17</div><div>cIPSWSTART</div><div>INTR</div></div> <div>INTR<div>stINTR, cIEXEC</div><div>EXEC</div></div>		<div>step50 => cIPSWSTART, (br step51)</div> <div>step51 => stINTR, cIEXEC, br step00</div>	