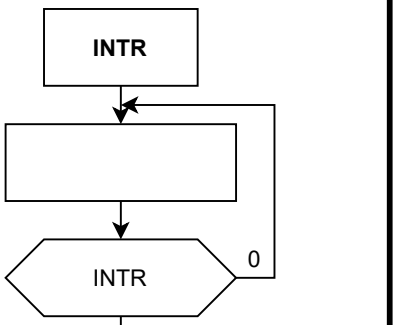
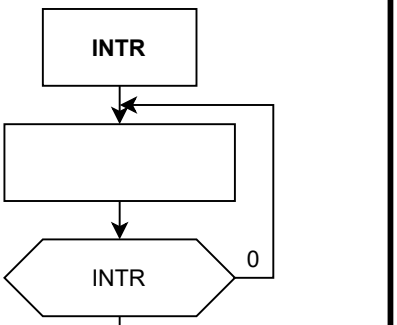
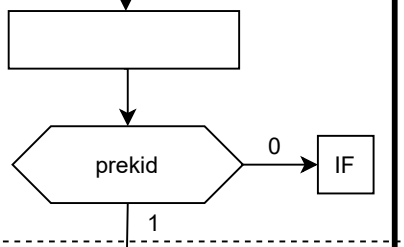
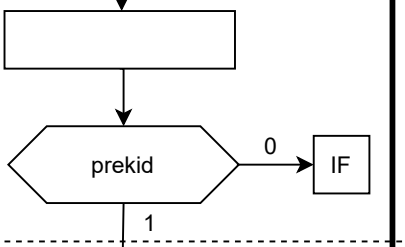
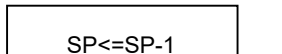
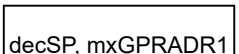
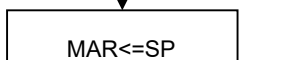
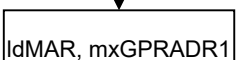
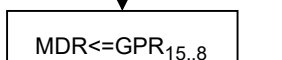
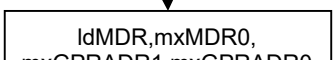
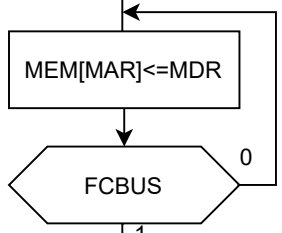
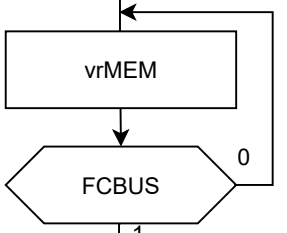
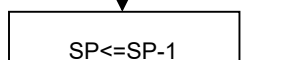
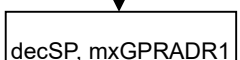
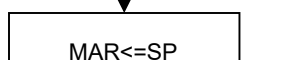
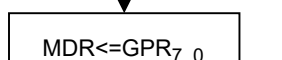
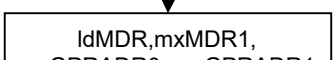
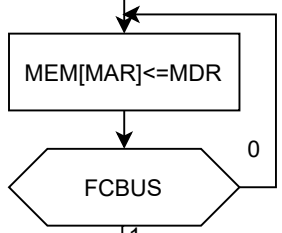
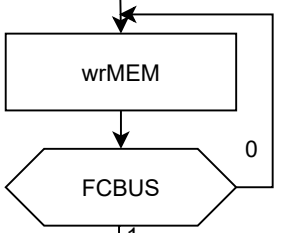
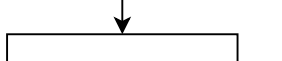
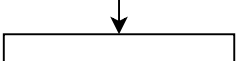
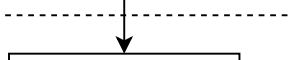
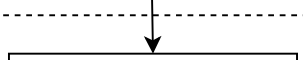
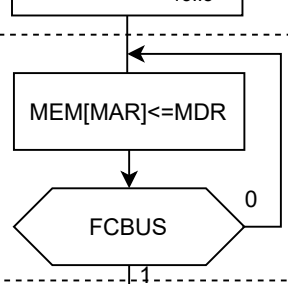
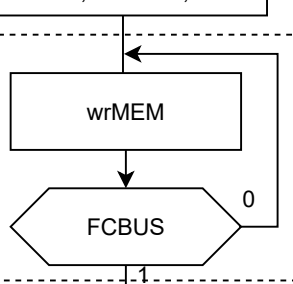
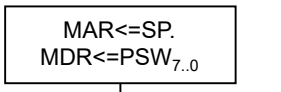
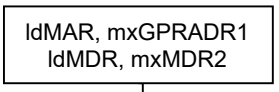
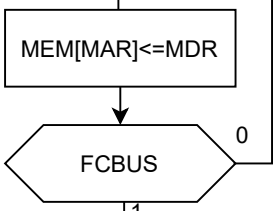
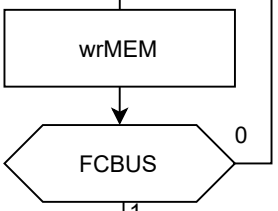
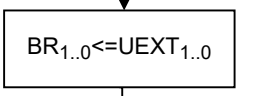
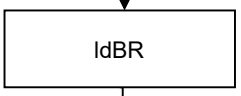
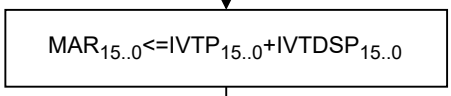
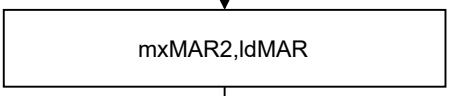
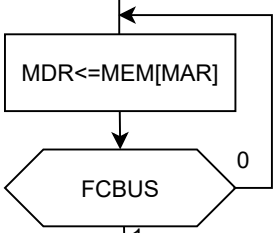
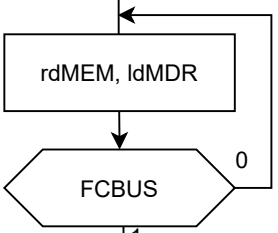
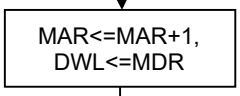
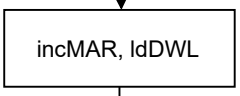
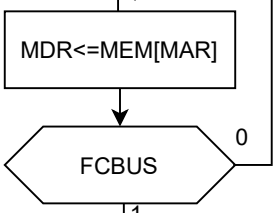
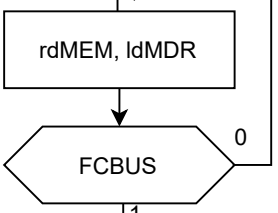
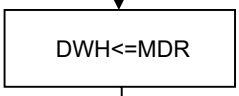
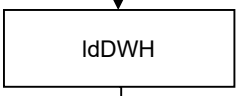
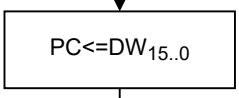
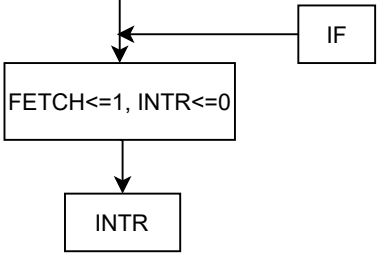
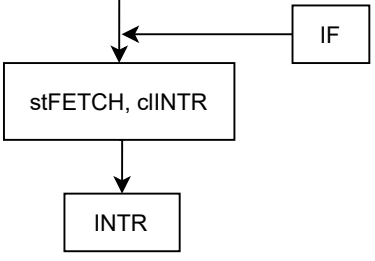
Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step00 => br(if notINTR then step00)
		step01 => br(if notprekid then step1F)
SP<=SP-1	decSP, mxGPRADR1	step02 => decSP, mxGPRADR1
MDR<=$PC_{15..8}$	ldMDR, mxMDR0	step03 => ldMDR, mxMDR0
MAR<=SP	ldMAR, mxGPRADR1	step04 => ldMAR, mxGPRADR1
MEM[MAR]<=MDR FCBUS 0 1	wrMEM FCBUS 0 1	step05 => wrMEM, br(if notFCBUS then step05)
SP<=SP-1	decSP, mxGPRADR1	step06 => decSP, mxGPRADR1
MDR<=$PC_{7..0}$	ldMDR, mxMDR1	step07 => ldMDR, mxMDR1
MAR<=SP	ldMAR, mxGPRADR1	step08 => ldMAR, mxGPRADR1
MEM[MAR]<=MDR FCBUS 0 1	vrMEM FCBUS 0 1	step09 => wrMEM, br(if notFCBUS then step09)

Име, презиме и број индекса	Иван Цветић 2019/0183 Славица Митровић 2019/0324	Потпис	**Назив:** Основи рачунарске технике 2 **Датум:** 27.02.2021. **Задатак 19:** Фаза опслуживања прекида, страна 1/3

Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step0A => decSP, mxGPRADR1
		step0B => ldMAR, mxGPRADR1
		step0C => ldMDR, mxMDR0, mxGPRADR1, mxGPRADR0
		step0D => wrMEM, br(if notFCBUS then step0D)
		step0E => decSP, mxGPRADR1
		step0F => ldMAR, mxGPRADR1
		step10 => ldMDR, mxMDR1 mxGPRADR0, mxGPRADR1
		step11 => wrMEM, br(if notFCBUS then step11)
		step12 => decSP, mxGPRADR1
		step13 => ldMAR, mxGPRADR1 mxMDR0, mxMDR1, ldMDR
		step14 => wrMEM, br(if notFCBUS then step14) step15 => decSP, mxGPRADR1

Име, презиме и број индекса	Иван Цветић 2019/0183 Славица Митровић 2019/0324	Потпис	**Назив:** Основи рачунарске технике 2 **Датум:** 27.02.2021. **Задатак 19:** Фаза опслуживања прекида, страна 2/3

Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step16 => ldMAR, mxGPRADR1, ldMDR, mxMDR2
		step17 => wrMEM, br(if notFCBUS then step17)
		step18 => ldBR
		step19 => ldMAR, mxMAR2
		step1A => rdMEM, ldMDR, br(if notFCBUS then step1A)
		step1B => incMAR, ldDWL
		step1C => rdMEM, ldMDR, br(if notFCBUS then step1C)
		step1D => ldDWH
		step1E => mxGPRIN0, mxGPRIN1, ldPC
		step1F => stFETCH, clINTR br step00

Име, презиме и број индекса	Иван Цветић 2019/0183 Славица Митровић 2019/0324	Потпис	**Назив:** Основи рачунарске технике 2 **Датум:** 27.02.2021. **Задатак 19:** Фаза опслуживања прекида, страна 3/3