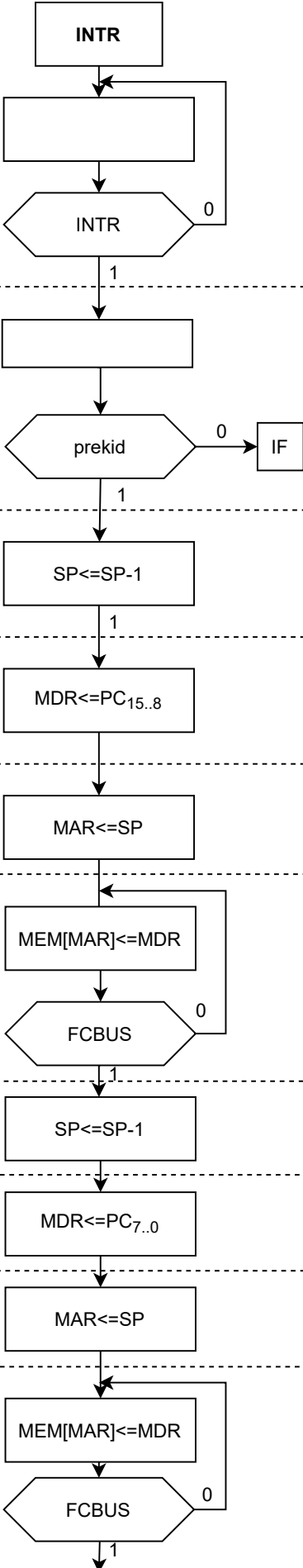
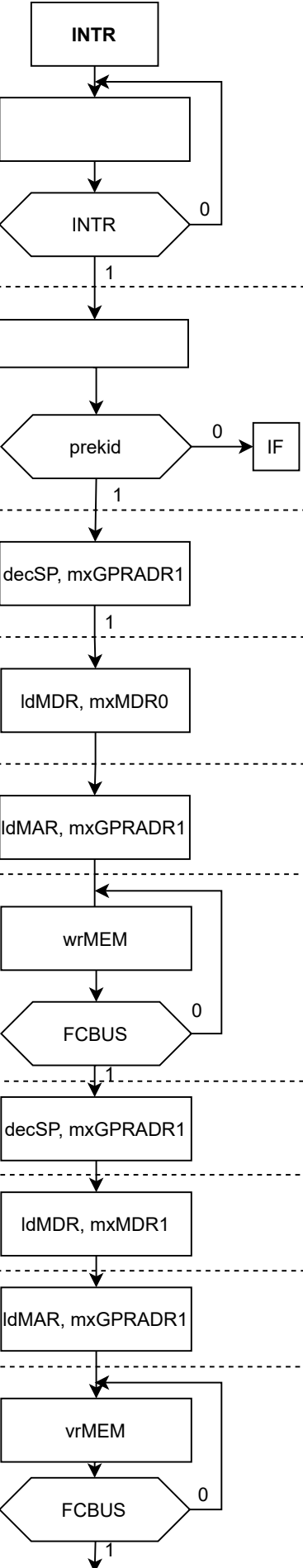


<div>Дијаграм тока микрооперација</div>	<div>Дијаграм тока управљачких сигнала</div>	<div>Секвенца управљачких сигнала</div>
 <pre> graph TD INTR1[INTR] --> Box1[] Box1 -- 0 --> INTR1 Box1 -- 1 --> INTR2{{INTR}} INTR2 -- 0 --> IF1[IF] INTR2 -- 1 --> SP1[SP ≤ SP-1] SP1 -- 1 --> MDR1[MDR ≤ PC15..8] MDR1 --> MAR1[MAR ≤ SP] MAR1 --> MEM1[MEM[MAR] ≤ MDR] MEM1 -- 0 --> FCBUS1{{FCBUS}} FCBUS1 -- 1 --> SP2[SP ≤ SP-1] SP2 --> MDR2[MDR ≤ PC7..0] MDR2 --> MAR2[MAR ≤ SP] MAR2 --> MEM2[MEM[MAR] ≤ MDR] MEM2 -- 0 --> FCBUS2{{FCBUS}} FCBUS2 -- 1 --> End1[] </pre>	 <pre> graph TD INTR3[INTR] --> Box3[] Box3 -- 0 --> INTR3 Box3 -- 1 --> INTR4{{INTR}} INTR4 -- 0 --> IF3[IF] INTR4 -- 1 --> decSP1[decSP, mxGPRADR1] decSP1 -- 1 --> ldMDR0[ldMDR, mxMDR0] ldMDR0 --> ldMAR1[ldMAR, mxGPRADR1] ldMAR1 --> wrMEM1[wrMEM] wrMEM1 -- 0 --> FCBUS3{{FCBUS}} FCBUS3 -- 1 --> decSP2[decSP, mxGPRADR1] decSP2 --> ldMDR1[ldMDR, mxMDR1] ldMDR1 --> ldMAR2[ldMAR, mxGPRADR1] ldMAR2 --> vrMEM1[vrMEM] vrMEM1 -- 0 --> FCBUS4{{FCBUS}} FCBUS4 -- 1 --> End3[] </pre>	<div>step00 => br(if notINTR then step00)</div> <div>step01 => br(if notprekid then step1F)</div> <div>step02 => decSP, mxGPRADR1</div> <div>step03 => ldMDR, mxMDR0</div> <div>step04 => ldMAR, mxGPRADR1</div> <div>step05 => wrMEM, br(if notFCBUS then step05)</div> <div>step06 => decSP, mxGPRADR1</div> <div>step07 => ldMDR, mxMDR1</div> <div>step08 => ldMAR, mxGPRADR1</div> <div>step09 => vrMEM, br(if notFCBUS then step09)</div>
<div>Име, презиме и број индекса</div> <div>Иван Цветић 2019/0183</div> <div>Славица Митровић 2019/0324</div>	<div>Потпис</div>	<div>Назив: Основи рачунарске технике 2</div> <div>Датум: 27.02.2021.</div> <div>Задатак 19: Фаза опслуживања прекида, страна 1/3</div>

Дијаграм тока микрооперација		Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
<div>SP<=SP-1</div>		<div>decSP, mxGPRADR1</div>	step0A => decSP, mxGPRADR1
<div>MAR<=SP</div>		<div>ldMAR, mxGPRADR1</div>	step0B => ldMAR, mxGPRADR1
<div>MDR<=GPR_{15..8}</div>		<div>ldMDR,mxMDR0, mxGPRADR1,mxGPRADR0</div>	step0C => ldMDR, mxMDR0, mxGPRADR1, mxGPRADR0
<div>MEM[MAR]<=MDR</div>		<div>vrMEM</div>	step0D => wrMEM, br(if notFCBUS then step0D)
<div>FCBUS</div>		<div>FCBUS</div>	
<div>SP<=SP-1</div>		<div>decSP, mxGPRADR1</div>	step0E => decSP, mxGPRADR1
<div>MAR<=SP</div>		<div>ldMAR, mxGPRADR1</div>	step0F => ldMAR, mxGPRADR1
<div>MDR<=GPR_{7..0}</div>		<div>ldMDR,mxMDR1, mxGPRADR0, mxGPRADR1</div>	step10 => ldMDR, mxMDR1 mxGPRADR0, mxGPRADR1
<div>MEM[MAR]<=MDR</div>		<div>wrMEM</div>	step11 => wrMEM, br(if notFCBUS then step11)
<div>FCBUS</div>		<div>FCBUS</div>	
<div>SP<=SP-1</div>		<div>decSP, mxGPRADR1</div>	step12 => decSP, mxGPRADR1
<div>MAR<=SP. MDR<=PSW_{15..8}</div>		<div>ldMAR,mxGPRADR1 mxMDR0,mxMDR1,ldMDR</div>	step13 => ldMAR, mxGPRADR1 mxMDR0, mxMDR1, ldMDR
<div>MEM[MAR]<=MDR</div>		<div>wrMEM</div>	step14 => wrMEM, br(if notFCBUS then step14)
<div>FCBUS</div>		<div>FCBUS</div>	
<div>SP<=SP-1</div>		<div>decSP, mxGPRADR1</div>	step15 => decSP, mxGPRADR1

Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
<pre> graph TD A[MAR<=SP, MDR<=PSW7..0] --> B[MEM[MAR]<=MDR] B --> C{FCBUS} C -- 0 --> B C -- 1 --> D[BR1..0<=UEXT1..0] D --> E[MAR15..0<=IVTP15..0+IVTDSP15..0] E --> F[MDR<=MEM[MAR]] F --> G{FCBUS} G -- 0 --> F G -- 1 --> H[MAR<=MAR+1, DWL<=MDR] H --> I[MDR<=MEM[MAR]] I --> J{FCBUS} J -- 0 --> I J -- 1 --> K[DWH<=MDR] K --> L[PC<=DW15..0] L --> M[IF] M --> N[FETCH<=1, INTR<=0] N --> O[INTR] </pre>	<pre> graph TD A[ldMAR, mxGPRADR1, ldMDR, mxMDR2] --> B[wrMEM] B --> C{FCBUS} C -- 0 --> B C -- 1 --> D[ldBR] D --> E[mxMAR2, ldMAR] E --> F[rdMEM, ldMDR] F --> G{FCBUS} G -- 0 --> F G -- 1 --> H[incMAR, ldDWL] H --> I[rdMEM, ldMDR] I --> J{FCBUS} J -- 0 --> I J -- 1 --> K[ldDWH] K --> L[mxGPRIN0, mxGPRIN1, ldPC] L --> M[IF] M --> N[stFETCH, clINTR] N --> O[INTR] </pre>	<p>step16 => ldMAR, mxGPRADR1, ldMDR, mxMDR2</p> <p>step17 => wrMEM, br(if notFCBUS then step17)</p> <p>step18 => ldBR</p> <p>step19 => ldMAR, mxMAR2</p> <p>step1A => rdMEM, ldMDR, br(if notFCBUS then step1A)</p> <p>step1B => incMAR, ldDWL</p> <p>step1C => rdMEM, ldMDR, br(if notFCBUS then step1C)</p> <p>step1D => ldDWH</p> <p>step1E => mxGPRIN0, mxGPRIN1, ldPC</p> <p>step1F => stFETCH, clINTR br step00</p>