

Cite this: *Lab Chip*, 2015, **15**, 1360

## Scaling of pneumatic digital logic circuits†

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The scaling of integrated circuits to smaller dimensions is critical for achieving increased system complexity and speed. Digital logic circuits composed of pneumatic microfluidic components have to this point been limited to a circuit density of  $2\text{--}4 \text{ gates cm}^{-2}$ , constraining the complexity of the digital systems that can be achieved. We explored the use of precision machining techniques to reduce the size of pneumatic valves and resistors, and to achieve more accurate and efficient placement of ports and vias. In this way, we attained an order of magnitude increase in circuit density, reaching as high as  $36 \text{ gates cm}^{-2}$ . A 12-bit binary counter circuit composed of 96 gates was realized in an area of  $360 \text{ mm}^2$ . The reduction in size also brought an order of magnitude increase in speed. The frequency of a 13-stage ring oscillator increased from 2.6 Hz to 22.1 Hz, and the maximum clock frequency of a binary counter increased from 1/3 Hz to 6 Hz.

Received 6th September 2014,  
Accepted 29th December 2014

DOI: 10.1039/c4lc01048e

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### Introduction

It is envisioned that the next generation of lab-on-a-chip devices will contain embedded controls built out of microfluidic circuits instead of electronics.<sup>1</sup> This strategy could reduce or eliminate the need for off-chip controllers while preserving low cost of manufacturing, both of which are valuable for encouraging the widespread dissemination of lab-on-a-chip technologies in applications such as point-of-care diagnostics. Embedded controls have previously been demonstrated for directing fundamental liquid handling operations such as flow control, metering, and mixing.<sup>2–4</sup> In order for microfluidic digital logic to progress beyond the proof-of-concept stage, a number of technology limitations must first be overcome. One important challenge is achieving the circuit density required to enable the construction of digital systems with sufficient complexity to perform useful control tasks.

Normally closed pneumatic membrane valves<sup>5</sup> have proven very effective as the basis for static digital logic circuits. Logic

gates built with such valves benefit from a sharply non-linear transfer function that entails good noise buffering.<sup>3,6</sup> This class of technology has been utilized to build memory latches,<sup>2</sup> adders,<sup>7</sup> shift-registers,<sup>3</sup> ring oscillators,<sup>6</sup> peristaltic pump controllers,<sup>6</sup> and counters.<sup>6</sup> However, the circuit density demonstrated in these previous reports has been limited. Defining a gate as a single valve plus the associated resistors and wiring, pneumatic circuits have been reported with densities ranging from  $2 \text{ gates cm}^{-2}$  in a wet-etched glass process<sup>2,6,7</sup> to  $4 \text{ gates cm}^{-2}$  in a soft-lithography process.<sup>3</sup>

In this report, we utilized machining by computer numerical control (CNC) and laser cutting to develop a new fabrication process for pneumatic digital logic circuits. Fabrication of multiple channel depths allowed a sharp reduction in resistor die area. Different valve geometries were explored in order to optimize both noise margins and valve area. Finally, precise drilling of ports and vias enabled more efficient packing. We thereby achieved an order-of-magnitude improvement in circuit density over previous pneumatic logic technologies, and concurrently, also achieved an order-of-magnitude increase in speed.

### Materials and methods

Pneumatic digital logic devices consisted of an elastomeric sheet sandwiched between two layers of either glass or plastic (Fig. 2A). Prior to device assembly, microfluidic channels were patterned into the glass or plastic, and through holes were cut in each of the three layers.

#### First-generation process: etching of channels in glass

Glass devices were constructed as previously described.<sup>5</sup> Photomask blanks (4" square borosilicate glass with chrome

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† Electronic supplementary information (ESI) available: Fig. S1. Timing diagram of 8-bit counter circuit. Fig. S2. Timing diagram of 12-bit counter circuit. Movie 1. 6-bit counter circuit fabricated in the first-generation glass process. The two rows of valves in the middle indicate the state of the 6 bits. A light reflection is visible when the valve is open and the bit value is high. This circuit operates at a maximum clock rate of 1/3 Hz. Movie 2. 8-bit counter circuit fabricated in the second-generation plastic process. The row of larger valves along the top indicate the state of the 8 bits. This circuit operates at a maximum clock rate of 6 Hz. Movie 3. 12-bit counter circuit fabricated in the second-generation plastic process. The row of larger valves along the top indicate the state of the 12 bits. There are two input connections visible to the lower right. One provides vacuum power to the entire circuit, and the other provides the clock reference signal. This circuit operates at a maximum clock rate of 3 Hz. Cycling through all states of the counter at 3 Hz takes 20 minutes, and so only selected portions of the video are shown here. See DOI: 10.1039/c4lc01048e

and AZ 1500 photoresist, Telic, Valencia CA) were exposed to ultraviolet light through a printed mask (FineLine Imaging, Colorado Springs CO) and developed in Shipley Microposit MF-319 followed by Transene Chromium Mask Etchant CE-5M. Channels were etched into the glass with concentrated hydrofluoric acid to a depth of 45–50 µm. The remaining photoresist and chromium were removed in acetone followed by chromium etchant, and the patterned glass wafer was diced with a diamond scribe (3543A31, McMaster-Carr, Santa Fe Springs CA). Ports through the glass were drilled by hand using a diamond-grinding point (4376A11, McMaster-Carr) and a rotary tool attached to a bench press (Dremel 400XPR, Robert Bosch Tool, Mount Prospect IL).

### Second-generation process: precision milling of channels in plastic

Sheets of polymethyl methacrylate (8560K171, McMaster-Carr) were cut into individual die with a CO<sub>2</sub> laser (VLS2.30, Universal Laser Systems, Scottsdale AZ) and mounted on a computer numerical control (CNC) milling platform (Mini Mill, Haas Automation Inc., Oxnard CA). Accurate control of surface planarity was critical in order to machine exact channel depths, and thus a diamond-tipped fly cutter (3316A32, McMaster-Carr) was employed to planarize the surface of the die prior to machining. However, the fly cut surface was not perfectly aligned to the horizontal axes of the machine, thus additional adjustment was required. Circuit designs were drawn in AutoCAD (Autodesk) and converted into G-code using a custom AutoLisp program. Data on surface irregularities were measured as described below and fed into this program, which modulated cutting depth to accommodate for surface variation and thereby control channel depth accurately.

Each milling tool was aligned to the die surface in a two-step process prior to each fabrication run. Polydimethylsiloxane (PDMS) sheets with a thickness of 254 µm (HT-6240, Rogers Corp, Rogers CT) were sputter coated with 30 nm of gold. This conductive sheet was placed on the surface of the die. As each tool was lowered, a multimeter was used to measure the conductivity between the tool and the sheet in order to detect the moment of contact. This achieved a vertical alignment accuracy of about 25 µm without damaging the small fragile tools, as might occur with shim methods. Once this initial alignment was completed, fine alignment was performed by positioning each tool at a nominal position of 100 µm above the substrate surface and then translating the active tool downwards at a shallow angle (1.414 mm lateral and 200 µm vertical). Measuring the length of the resulting cut allowed the vertical offset of the tool to be determined and corrected. Further, by measuring the vertical offset at multiple points across the die, this technique was also employed to measure the horizontal alignment of the die surface after fly cutting.

In this study, we used tools ranging from 50.8 µm to 1450 µm in diameter. Miniature end mills are commercially

available as small as 25.4 µm. Specifically, we used the following tools: 0.002" end mill (Microcut USA 82002), 0.003" end mill (Microcut USA 82003), 0.004" end mill (Microcut USA 82004), 0.006" end mill (Microcut USA 82006), 0.008" end mill (Microcut USA 82008), 0.02" end mill (Microcut USA 82020), 0.03" end mill (Microcut USA 82030), 0.04" end mill (Microcut USA 82040), and a #52 drill bit (0.0635", McMaster-Carr 8856A54). Small tools are fragile and susceptible to breakage. Specifically, 35 of 59 tools smaller than 0.01" were broken over the course of 3 years. Ports through the plastic were bored directly on the CNC mill, giving much better precision than the manual method used in the first-generation glass process.

### Laser patterning of holes in elastomeric sheets

Polydimethylsiloxane (PDMS) sheets at a thickness of 254 µm (0.01 inch) were either purchased (HT-6240, Rogers Corp, Rogers CT) or cast in CNC machined molds (Sylgard 184, Dow-Corning, Midland MI). Cast sheets displayed less thickness variation and were more reliable for use in large circuits such as binary counters. In the first-generation process, *via* holes were manually punched with a blunt hollow needle. In the second-generation process, laser cutting was employed instead. The HT-6240 sheets are shipped covered on both sides with Mylar film. The Mylar was removed to release residual stress in the PDMS and then reapplied. The shielded PDMS was then glued to a glass slide with liquid Super Glue to keep the sheet flat during laser ablation. A 25 W CO<sub>2</sub> laser (VLS2.30, Universal Laser Systems, Scottsdale AZ) was used to pattern 100 µm *via* holes into the PDMS sheets. Cutting was performed at 30% power and 20% speed. The machine was tuned to generate a single laser pulse for each hole in order to achieve optimal hole uniformity. Char produced during laser ablation was removed by blowing with compressed air, mechanically brushing the remaining char with tweezers, and rinsing with distilled water followed by 100% ethanol. The protective Mylar layers were then removed to yield a largely debris-free PDMS membrane. If particulates were later introduced during handling, the membranes were cleaned in ethanol in an ultrasonic bath. Following this treatment, care must be taken to evaporate all ethanol from the PDMS, otherwise the absorbed ethanol can impact mechanical properties.

### Device assembly

Devices were cleaned immediately prior to assembly. Glass devices were cleaned by rinsing with 100% ethanol and drying with compressed air. Plastic devices were cleaned by rinsing in detergent (Versa-Clean, Fisher Scientific), then distilled water, and finally 100% ethanol before drying with compressed air. Any visible burrs were carefully removed with tweezers. For the first-generation process, the elastomeric sheet was first aligned onto the bottom glass layer by hand using a dissection microscope. The top glass layer was then aligned in the same way, and all three layers were pressed together. For the second-generation process, alignment holes

(#52 drill bit) were included at the four corners of each layer during fabrication. Each layer was then aligned by fitting the holes onto tapered stainless steel pins (90681A002, McMaster-Carr). The alignment of the elastomeric sheet was verified by microscope prior to assembly of the top plastic layer. In some cases, assembled devices were physically clamped with office binder clips for tighter sealing. This was generally important for larger and more complicated devices. For example, a 12-bit counter required clamping to function properly (Fig. 3D), while an 8-bit counter did not.

### Measurement of inverter transfer function

In order to measure the transfer function of an inverter, the input and output of the device were each connected to a separate pressure sensor (PX100-39, Omega Instruments, Stamford CT). Input pressure was controlled with a vacuum regulator (V-800-30-W/K, Coast Pneumatics), and vacuum was supplied by an electrical pump (4176K11, McMaster-Carr). Output pressure was recorded as the input pressure was swept from atmospheric pressure to 2.7 psia and back. Each point of the transfer function was measured at steady state.

### Frequency measurement

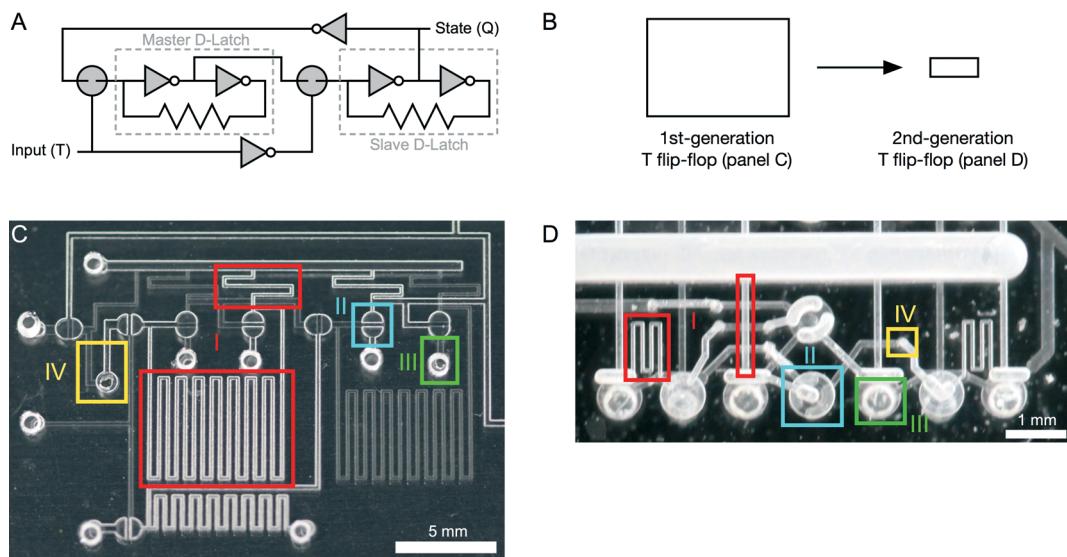
Oscillator frequencies were measured by laser deflection as previously described<sup>6</sup> or by high-speed video microscopy. Laser deflection was performed on glass oscillators by shining a laser through an inverter valve of the oscillator and recording the light output with a photodiode. In the plastic devices,

the smaller milled valves resulted in too much light scattering for the laser deflection measurement. Instead, the motion of the valves was captured by high-speed camera (EX-FH100, Casio Computer Co.), and the oscillation frequency was extracted from the video.

## Results and discussion

The circuit scaling strategies that were pursued in this study are summarized in Fig. 1, which illustrates T flip-flop circuits fabricated in two different processes. The first-generation process defines circuit features by wet etching of a glass substrate and has been successfully employed in the past to build a variety of digital logic circuits.<sup>2,5–7</sup> The second-generation, higher density process was developed over the course of this study and defines circuit features by precision milling of a plastic substrate.

In the first-generation glass process, all features were etched to an identical depth of about 50 µm. Since the etch is isotropic, features were also broadened by 100 µm during this etch. The wet etch thus defines a minimum channel cross section. Consequently, high resistance circuit elements required long channels, which occupied large amounts of die area (Fig. 1C). In contrast, the second-generation plastic process allowed high resistance channels to be milled at 51 µm wide by 15 µm deep, thus much shorter lines were required to achieve similar resistances. Milling allowed high resistance channels (51 µm × 15 µm), moderate resistance channels (203 µm × 203 µm), and low resistance bus lines

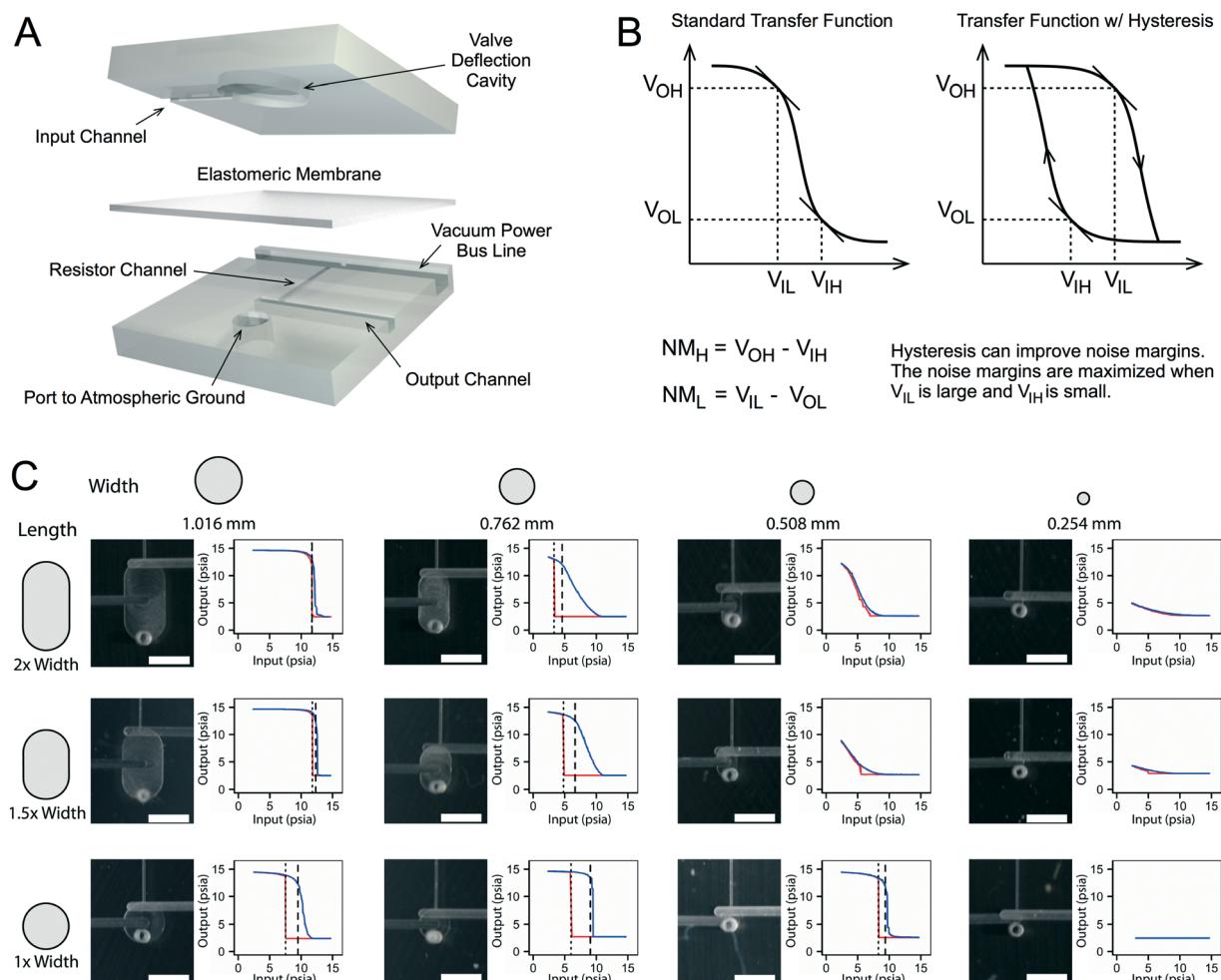


**Fig. 1** Scaling strategies. A. Schematic of T flip-flop. The circuit contains two D latches in a master-slave configuration. B. Pneumatic T flip-flops scale from 420 mm<sup>2</sup> in the first-generation etched glass process (C) to 22 mm<sup>2</sup> in the second-generation machined plastic process (D). I. Resistor cross section scales from 150 × 50 µm<sup>2</sup> down to as small as 51 × 15 µm<sup>2</sup>, allowing resistor lengths to shrink from 96 mm to 3.9 mm and from 9.0 mm to 1.7 mm in this circuit. II. Valve area is reduced from 1.5 × 1.1 mm<sup>2</sup> to 0.76 × 0.76 mm<sup>2</sup>. III. In the first-generation process, ports to atmospheric ground are manually drilled, requiring a significant buffer margin to be placed between ports and other features. In the second-generation process, ports are precision machined, allowing ground holes to be placed directly under valves to conserve space. IV. Via ports through the membrane layer are manually cored in the first-generation process, again requiring a significant buffer margin around vias. In the second-generation process, laser etching of vias allows smaller holes with high precision placement for denser packing.

( $762\text{ }\mu\text{m} \times 1016\text{ }\mu\text{m}$ ) to be employed concurrently on a single die. The use of multiple channel depths to vary resistance in pneumatic circuits was previously employed by Rhee *et al.* in a soft lithography process,<sup>3</sup> helping to achieve the highest density pneumatic circuits that have been reported prior to this study.

Next, we explored modifying the design of the valves (Fig. 2). The original design from the Mathies group is a circular or pill-shaped valve with a diameter of roughly 1 mm.<sup>2,5</sup> For the purposes of this study, we fixed the thickness of the elastomeric membrane layer at 254  $\mu\text{m}$  and sought to optimize valve size and performance given this constraint. This membrane dimension is convenient because rolls of silicone sheets can be purchased at this thickness, thus expediting device fabrication. Digital inverter gates were fabricated with a range of valve shapes and sizes, as shown in Fig. 2, and the transfer function of each gate was

measured. The specific valve sizes that we examined were chosen to match the sizes of the tool bits that we had available; finer optimization may still be possible. The circular valve design was found to be optimal for maximizing the high and low noise margins (Fig. 2B–C). In the digital paradigm, circuit variations and environmental fluctuations may generate noise, but as long as the sum of the noise contributions remains below the noise margin, there is no detrimental effect on circuit function. Higher noise margins are thus desirable, as they contribute to greater robustness. As size was reduced, circular valves remained functional at diameters of 1.016 mm, 0.762 mm, and 0.508 mm, but the 0.254 mm circular valve was too small to open. Additionally, in the 0.508 mm design, the resistance of the open valve was considerably higher than in the larger valves. As previously described,<sup>3</sup> the inverter design requires the pull-up resistor to be roughly ten times greater than the resistance of the



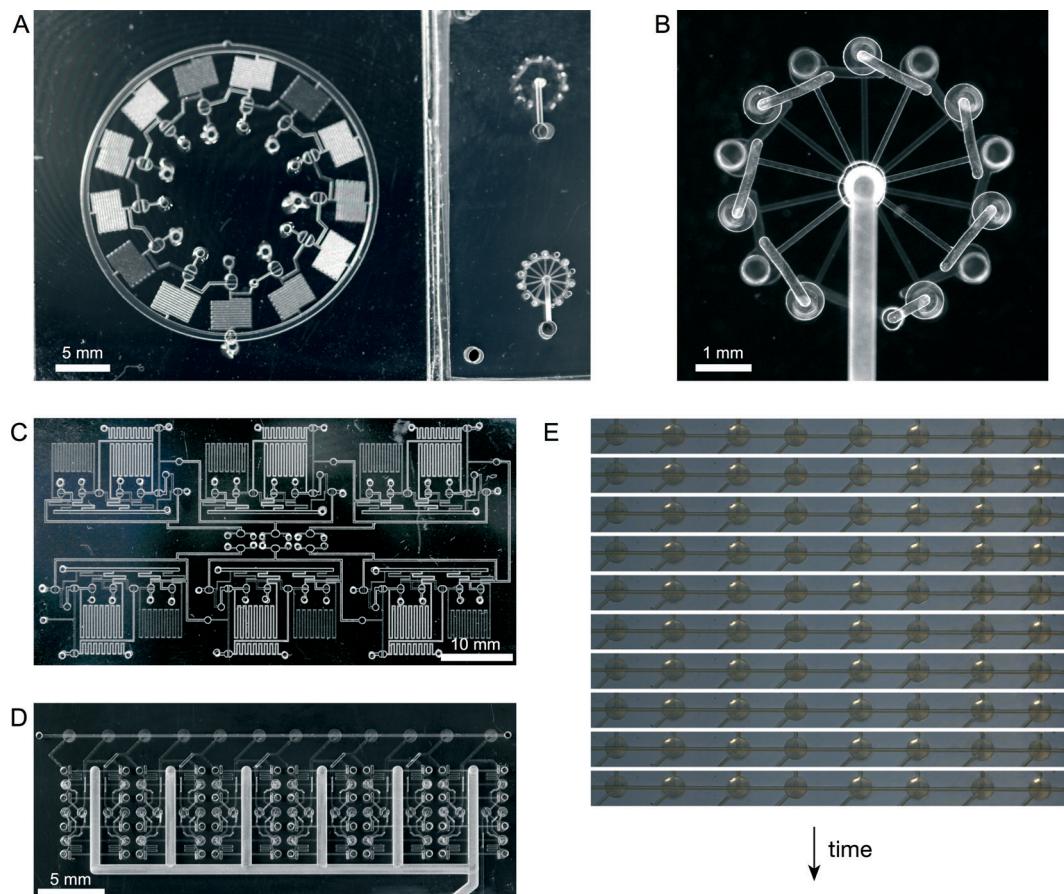
**Fig. 2** Optimization of valve design. **A.** Exploded view diagram of pneumatic inverter gate. Vacuum input deflects the membrane to connect output to ground. With the valve closed under atmospheric input, the gate outputs vacuum pressure. **B.** Definitions of high and low noise margins (NM). The pneumatic membrane valve exhibits hysteresis that actually improves the noise margins. **C.** Transfer function characteristics for the pneumatic inverter gate as the size and shape of the valve deflection cavity are varied. The opening curve is shown in red, and the closing curve is shown in blue. Dotted lines are drawn to indicate the positions of  $V_{IH}$  (red) and  $V_{IL}$  (blue). In order to maximize the noise margins,  $V_{IH}$  should be low and  $V_{IL}$  should be high. Not all designs were functional. A round shape with 0.762 mm diameter was chosen as the optimal valve design. Scale bars are 1 mm.

open valve. Hence, the high resistance of the 0.508 mm valve required the valve to be paired with larger pull-up resistors, which negated the size advantage of the smaller valve and also reduced circuit speed.<sup>6</sup> Taking all factors into account, the circular valve design with a diameter of 0.762 mm was chosen as the best mix of size and performance out of the variations that we explored.

The boring of ports and vias was another area that was targeted for improvement. In the first-generation glass process, photolithography was only used to define the valves and channels. Manual drilling was subsequently required in order to bore ports through the glass. Due to the inaccuracy of manual drilling, ports had to be separated from other circuit elements by a buffer of 0.5 mm in order to prevent damage to the circuit during the drilling process (Fig. 1C). In contrast, the second-generation plastic process allowed ports to be precisely bored as part of the milling procedure. In many cases, ports to atmospheric ground could be placed directly underneath a valve, thus contributing zero footprint (Fig. 1D).

Similarly, in the first-generation process, *via* ports through the elastomeric membrane layer were formed by manual punching. Due to the inaccuracy of this process, vias had to be spaced apart from other circuit elements by 0.5 mm, and channels had to be widened where they connected to vias (Fig. 1C). In the second-generation process, we introduced the boring of vias by laser cutting, allowing small holes to be formed and placed accurately. The use of alignment pins was also added in order to assist in the accurate alignment of vias and channels. These techniques combined to produce a significant reduction in the area consumed by *via* ports (Fig. 1D).

All together, these scaling strategies resulted in an order-of-magnitude improvement in circuit density. Specifically, the T flip-flop circuit was reduced from a die area of 420 mm<sup>2</sup> in the first-generation process to 22 mm<sup>2</sup> in the second-generation process. Since this T flip-flop design contains 8 individual gates, this equates to a density of 36 gates cm<sup>-2</sup>. In the case of a 13-stage ring oscillator, circuit area was reduced from 571 mm<sup>2</sup> to 29.3 mm<sup>2</sup> (Fig. 3A, B). An



**Fig. 3** Scaling reduces die area and increases speed. A. 13-stage ring oscillator fabricated in the first-generation etched glass process (left) and in the second-generation milled plastic process (right). Side-by-side, the size difference is apparent. Device area decreases from 571 mm<sup>2</sup> to 29.3 mm<sup>2</sup>, while the oscillation frequency increases from 2.6 Hz to 22.1 Hz. B. Higher magnification image of the second-generation 13-stage ring oscillator. C. 6-bit asynchronous counter circuit in first-generation process. This circuit occupies 2100 mm<sup>2</sup> and runs at a maximum clock rate of 1/3 Hz. D. 12-bit asynchronous counter circuit in second-generation process. This circuit occupies 360 mm<sup>2</sup> and runs at a maximum clock rate of 3 Hz. E. Time course images illustrate the operation of a second-generation 8-bit counter circuit operating at 6 Hz. In these images, the counter increments from 01100100 to 01101101.

important advantage of higher density circuits is that they allow more complex designs to be realized. For example, T flip-flops may be cascaded to form asynchronous counter circuits, with each bit of the counter requiring a single T flip-flop. In the first-generation process, a 6-bit counter required 2100 mm<sup>2</sup> of die area (Fig. 3C), approaching the practical limit for total device area given our typical defect density. In the second-generation process, it was possible to build a fully functional 12-bit counter in an area of only 360 mm<sup>2</sup> (Fig. 3D). Since the second-generation plastic process offers low-resistance bus lines, this 12-bit counter required only a single vacuum connection to supply power to 108 gates. In contrast, the first-generation glass 6-bit counter required 12 separate power connections, with two connections required for each T flip-flop. Achieving a 12-bit counter is a significant milestone, as the circuit may be coupled with a 1 Hz clock<sup>6</sup> to provide timing control for an hour-long process with a resolution of 1 second.

It should be noted that direct milling is a serial process that is not appropriate for mass manufacturing. However, the geometries and dimensions of the milled plastic layers in our second-generation technology are well suited for production by injection molding. In this scenario, molds would initially be defined by CNC milling and then reused to produce large numbers of devices at a very low cost per unit.<sup>8</sup> Molding may also be advantageous for minimizing device-to-device variability in manufacturing.<sup>9</sup>

In microelectronics, transistor scaling typically has brought an increase in switching speed due to the decrease in gate capacitance for smaller transistors. Though the relationship is not exact, volume in pneumatic circuits is fairly analogous to capacitance in electrical circuits.<sup>6</sup> Thus, the decrease in circuit volume that occurs as die area is reduced should be expected to produce an increase in speed. Indeed, shrinking a 13-stage ring oscillator increased its oscillation frequency from 2.6 Hz to 22.1 Hz. Likewise, a first-generation glass 6-bit counter could be operated at a maximum clock frequency of 1/3 Hz (ESI,† Movie 1), while a second-generation plastic 12-bit counter could be operated at up to 3 Hz (ESI,† Fig. S2, Movie 3), and a 8-bit counter could be operated at up to 6 Hz (ESI,† Fig. S1, Movie 2).

Thus, the fabrication process developed in this study brings order-of-magnitude increases in both circuit density and speed compared to previous pneumatic logic technologies. In addition, our process brings pneumatic logic technology to a similar level of density as hydraulic logic technologies. A single D-latch occupies 5 mm<sup>2</sup> in our pneumatic technology, which is equal to the 5 mm<sup>2</sup> reported by Weaver *et al.*<sup>10</sup> but

not quite as good as the 2.4 mm<sup>2</sup> reported by Devaraju *et al.*<sup>11</sup> These hydraulic logic technologies were fabricated with modified soft lithography processes that utilized a significantly thinner membrane layer (45 µm)<sup>11</sup> compared to our process (254 µm). In our pneumatic logic technology, we found the optimum valve diameter to be about 3 times the thickness of the valve membrane. It is likely that valve diameter can decrease as membrane thickness is decreased, not unlike the decrease in gate dielectric thickness that is required for transistor scaling. Thus, considerable opportunities remain for further scaling of pneumatic digital logic technology, and the circuit density reported in this study should not be interpreted as representing an ultimate limit.

## Acknowledgements

This work was supported by the National Science Foundation under grant no. ECCS-1102397 and by the Defense Advanced Research Projects Agency (DARPA) N/MEMS S&T Fundamentals Program under grant no. N66001-1-4003 issued by the Space and Naval Warfare Systems Center Pacific (SPAWAR) to the Micro/nano Fluidics Fundamentals Focus (MF3) Center. S.A. was supported by NSF IGERT fellowship #0549479 (LifeChips).

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