CMOS-based NAND Logic Gate

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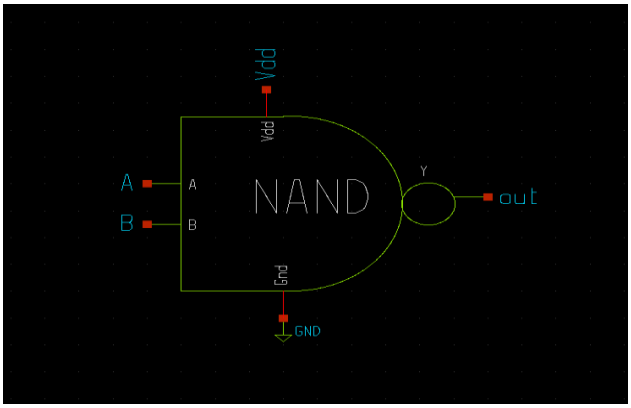
ABSTRACT: Real-world signals are mostly based on Boolean operators. In simple language, Boolean operators are logic gates, which are the building blocks of any circuit. There are different types of logic gates like AND, OR, NOT, NAND, NOR, XOR, and XNOR. These all-logic gates are implemented using a Boolean function. All these logic gates internally are implemented using diodes and transistors. In this paper, we are going to analyze NAND GATE using CMOS in skywater 130 nm technology. We will simulate the proposed design of NAND Gate in Xschem Software, an EDA tool.

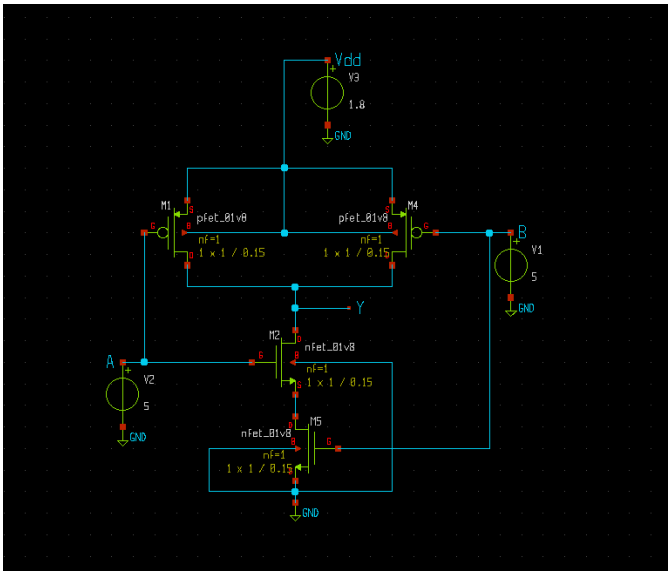
INTRODUCTION

For the implementation of NAND Gate using CMOS, we have to connect Both P-MOS in parallel with each other and N-MOS in series with each other. Let us name the first P-MOS as M1, Second PMOS as M2 one N-MOS as M3, and other N-MOS as M4. Vcc1 is the high voltage and GND is taken as Ground. As in this circuit, we are going to analyze 2 input NAND Gate using 180nm technology which is performed in eSim. There are two input A and B which is going into both P-MOS and N-MOS. And output of this proposed NAND Gate is obtained at Yout.

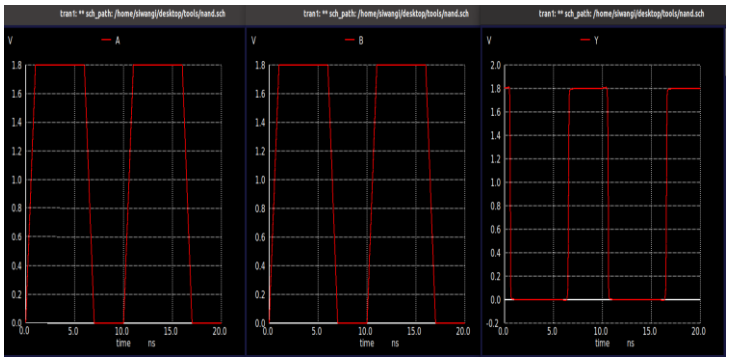
Block Diagram



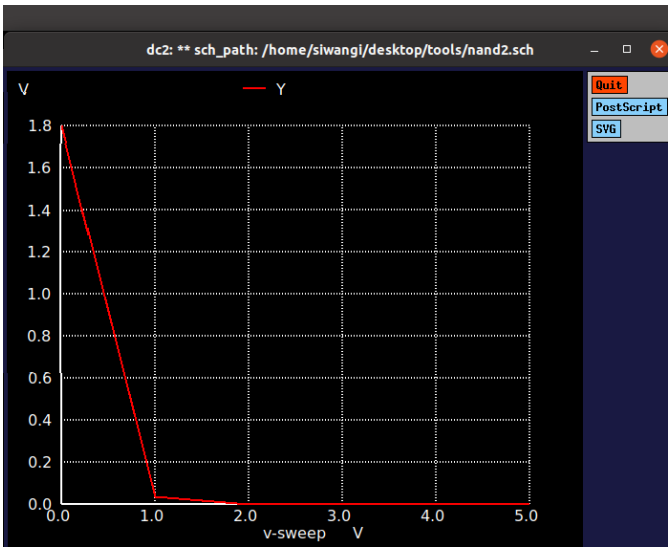
Circuit Design



Transient Plot



DC Plot



CONCLUSION

NAND gate is designed and plotted successfully.

Open Source Tools:

1) *NGspice*
2) *Xschem*