CMOS-based NAND Logic Gate

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ABSTRACT: Real-world signals are mostly based on Boolean operators. In simple language, Boolean operators are logic gates, which are the building blocks of any circuit. There are different types of logic gates like AND, OR, NOT, NAND, NOR, XOR, and XNOR. These all-logic gates are implemented using a Boolean function. All these logic gates internally are implemented using diodes and transistors. In this paper, we are going to analyze NAND GATE using CMOS in skywater 130 nm technology. We will simulate the proposed design of NAND Gate in Xschem Software, an EDA tool.

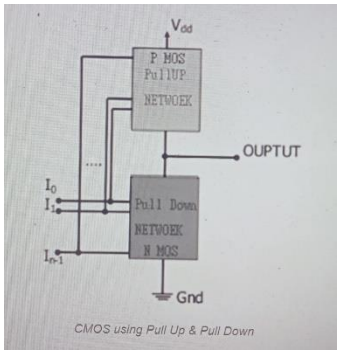
INTRODUCTION

Logic family is a type of method that is used for the implementation of different types of logic gates in the VLSI industry. And logic family is classified into two types that is Bipolar Logic Family and the Unipolar Logic Family. The bipolar logic family is classified into two types Saturated and unsaturated logic family. The unipolar logic family is classified into three types P-MOS (P- P-channel Metal Oxide semiconductor), N-MOS (N-channel Metal Oxide Semiconductor), and CMOS (Complementarily Metal Oxide Semiconductor). As we know CMOS consists of both p- p-channel and n-channel MOSFET (Metal Oxide Semiconductor Field Effect Transistor) which are connected in series with each other. For the implementation of NAND Gate using CMOS, we have to connect Both P-MOS in parallel with each other and N-MOS in series with each other. Let us name the first P-MOS as M1, Second PMOS as M2 one N-MOS as M3, and other N-MOS as M4. Vcc1 is the high voltage and GND is taken as Ground. As in this circuit, we are going to analyze 2 input NAND Gate using 180nm technology which is performed in eSim. There are two input A and B which is going into both P-MOS and N-MOS. And output of this proposed NAND Gate is obtained at Yout.

PRINCIPLE OF GENERATION

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal that turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

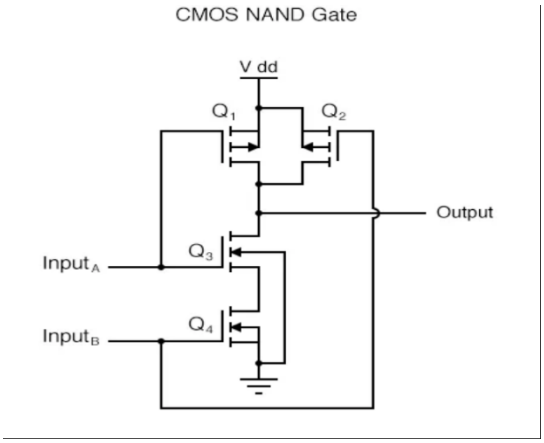
In CMOS Logic gate collection of n-type MOSFETs is arranged in a pull-down network between the output and the low-voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd). Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure.



CMOS using Pull Up & Pull Down

DESIGN OVERVIEW

The below figure shows a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.
If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.

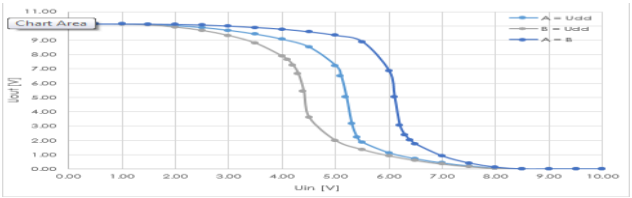


Saturation: $I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$

Linear (Triode, Ohmic):

$$I_D = \mu C_{ox}\frac{W}{L}\left((V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right)$$

Cutoff: $I_D \approx 0$



CONCLUSION

CMOS offers relatively high speed, low power dissipation, and high noise margins in both states and will operate over a wide range of source and input voltages (provided the source voltage is fixed).

REFERENCES

1) ELPROCUS:https://www.elprocus.com/cmos-working-principle-and-applications/
2) IJRASET(International Journal for Research in Applied Science & Engineering Technology)
3) UDEMY COURSE