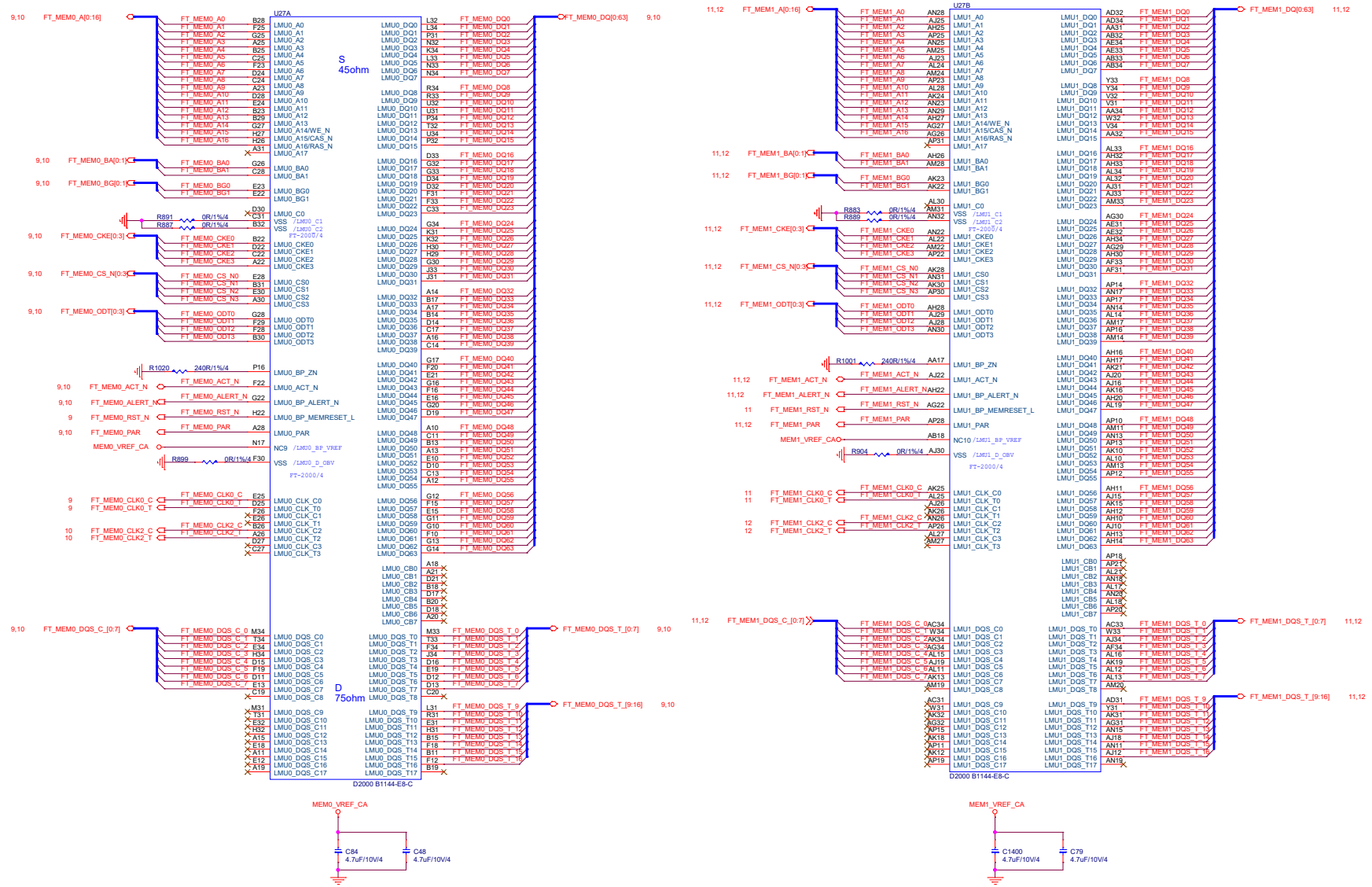
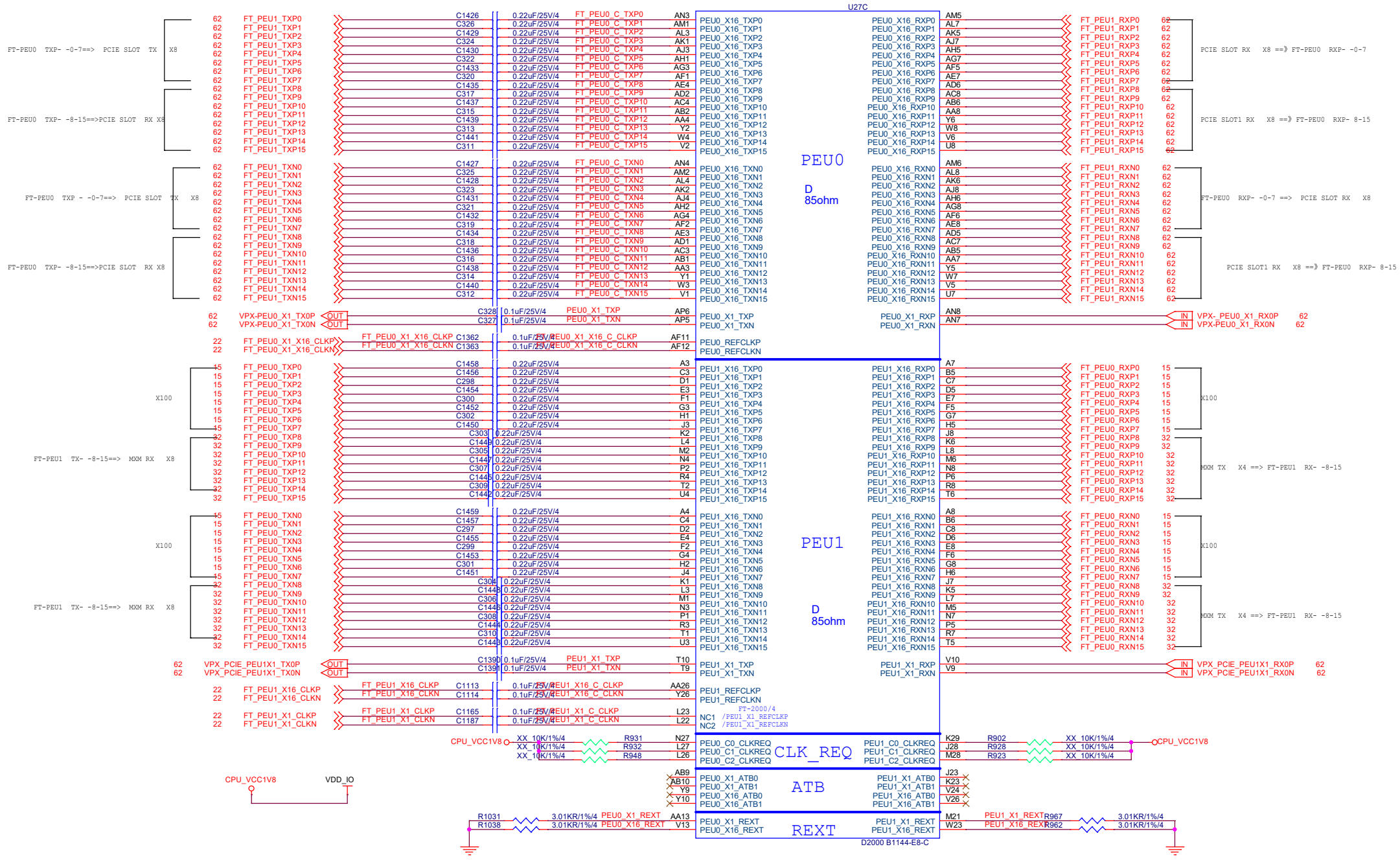
| | | | |
|---|---|---|---|
| Title <Title> | | | |
| Size A | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | | Sheet 1 of 64 | |

| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 2 of 64 | |

| | |
|---|---|
| Title | <Title> |
| Size A | Document Number <Doc> |
| Rev | <RevCode> |
| Date: | Saturday, April 19, 2025 |
| Sheet | 3 of 64 |




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 4 of 64 | | |


U27C
PEU0
D
85ohm
PEU1
D
85ohm
CLK_REQ
ATB
REXT
FT-2000/4
D2000 B1144-E8-C
FT-PEU0 TXP- -0-7==> PCIE SLOT TX X8
FT-PEU0 TXP- -8-15==>PCIE SLOT RX X8
FT-PEU0 TXP - -0-7==> PCIE SLOT TX X8
FT-PEU0 TXP- -8-15==>PCIE SLOT RX X8
FT-PEU1 TX- -8-15==> MXM RX X8
PCIE SLOT RX X8 ==》FT-PEU0 RXP- -0-7
PCIE SLOT1 RX X8 ==》FT-PEU0 RXP- 8-15
FT-PEU0 RXP- -0-7 ==> PCIE SLOT RX X8
MXM TX X4 ==> FT-PEU1 RX- -8-15
CPU_VCC1V8
VDD_IO
Title
<Title>
Size A3
Document Number
<Doc>
<RevCode>
Rev
Date: Saturday, April 19, 2025
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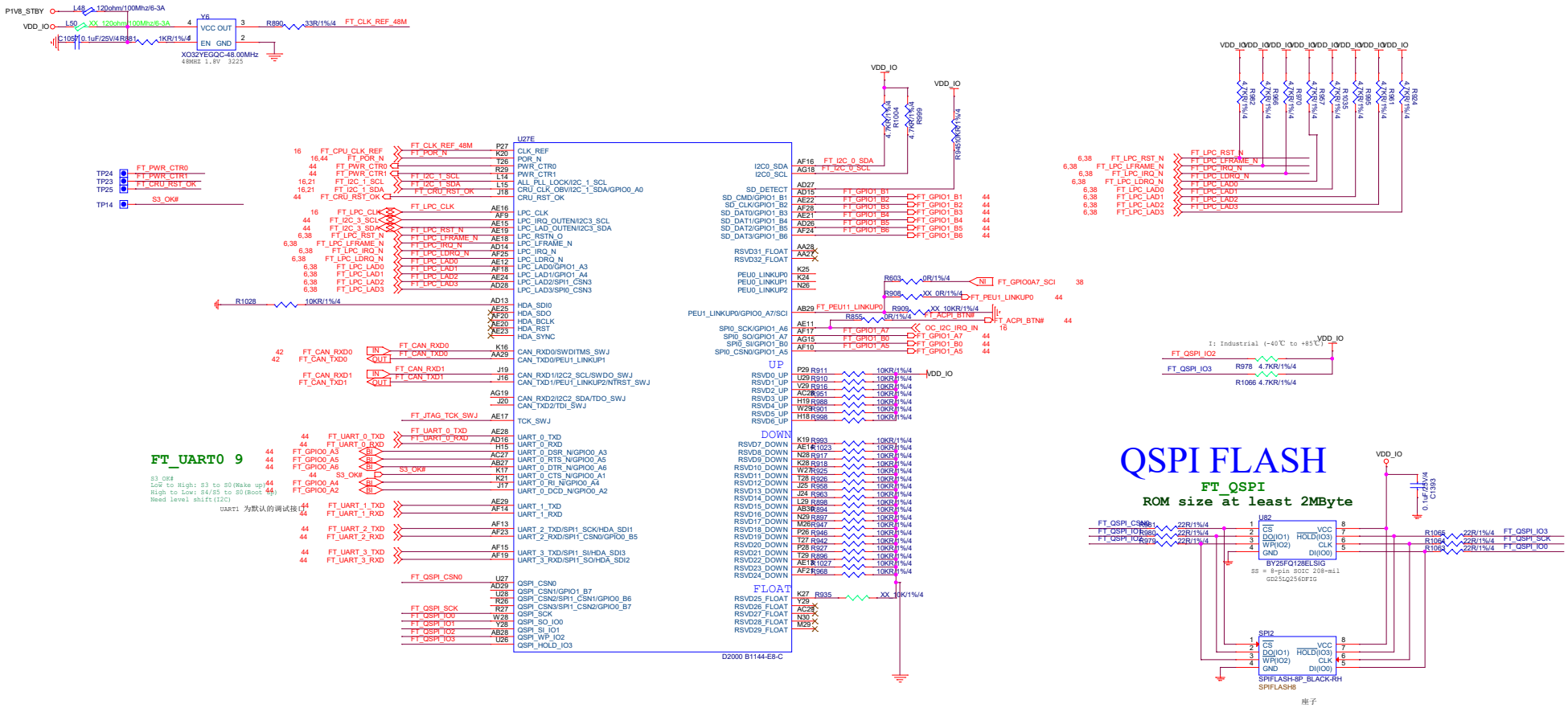
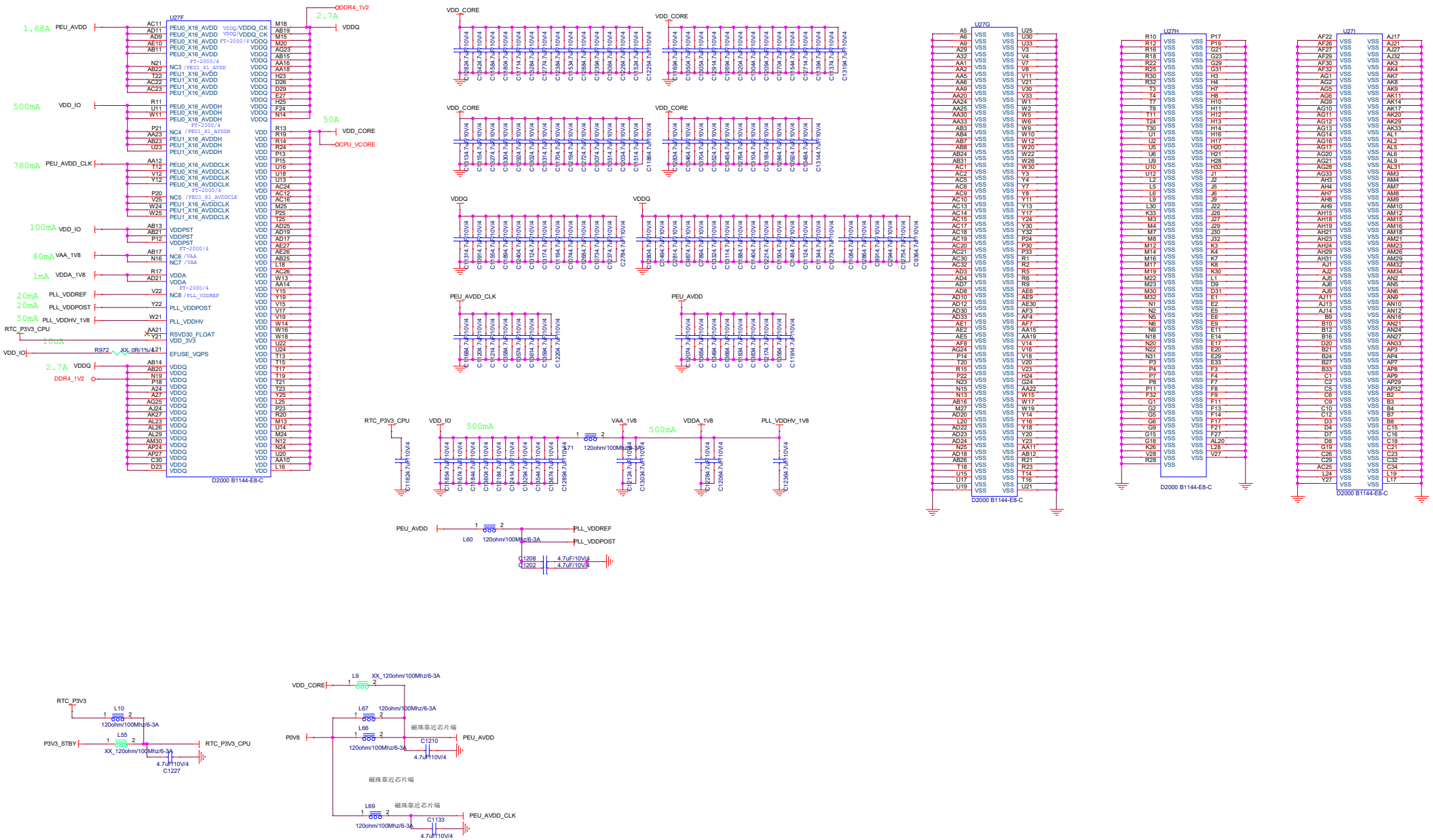
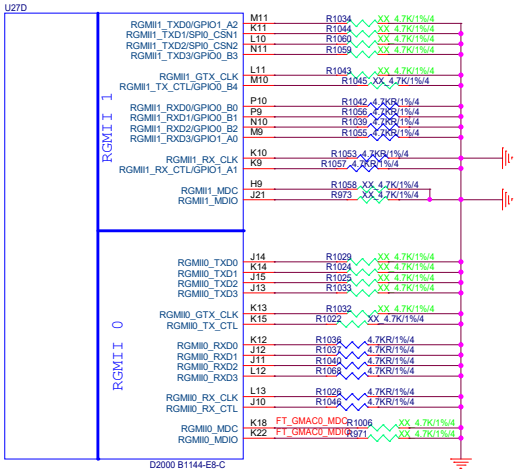


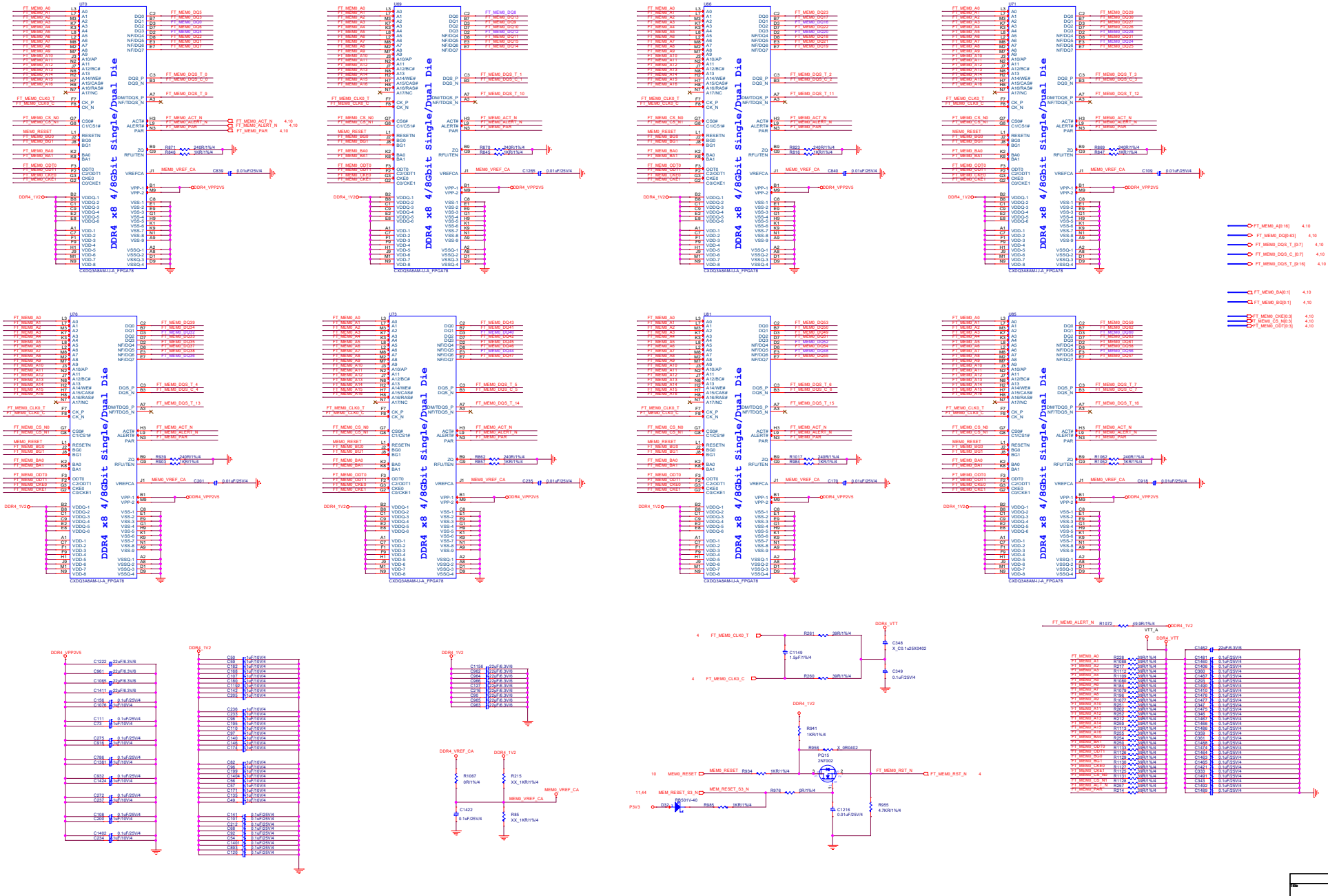

| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 6 of 64 |



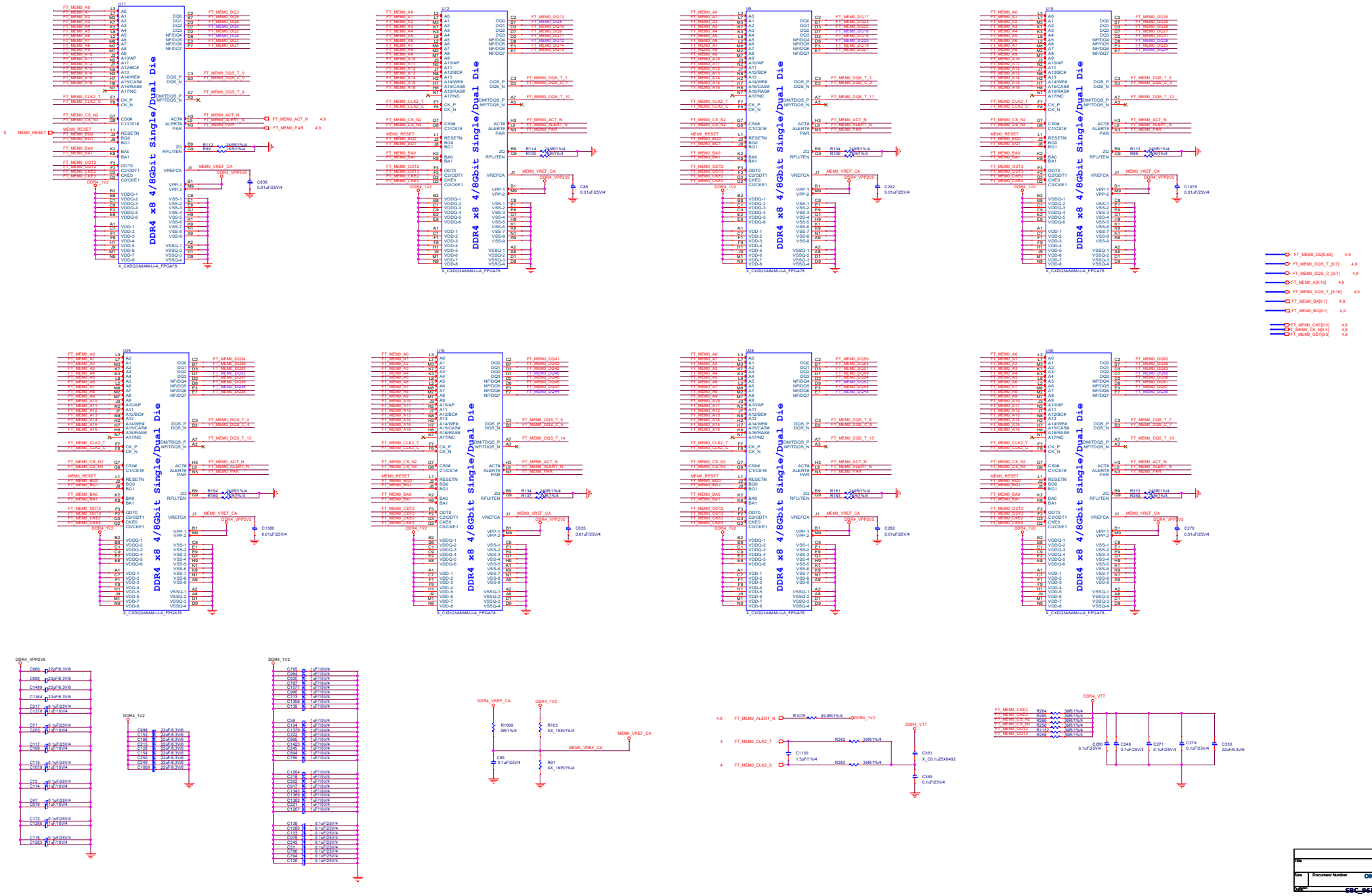

| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | <RevCode> Rev |
| Date: Saturday, April 19, 2025 | Sheet 7 of 64 | | |



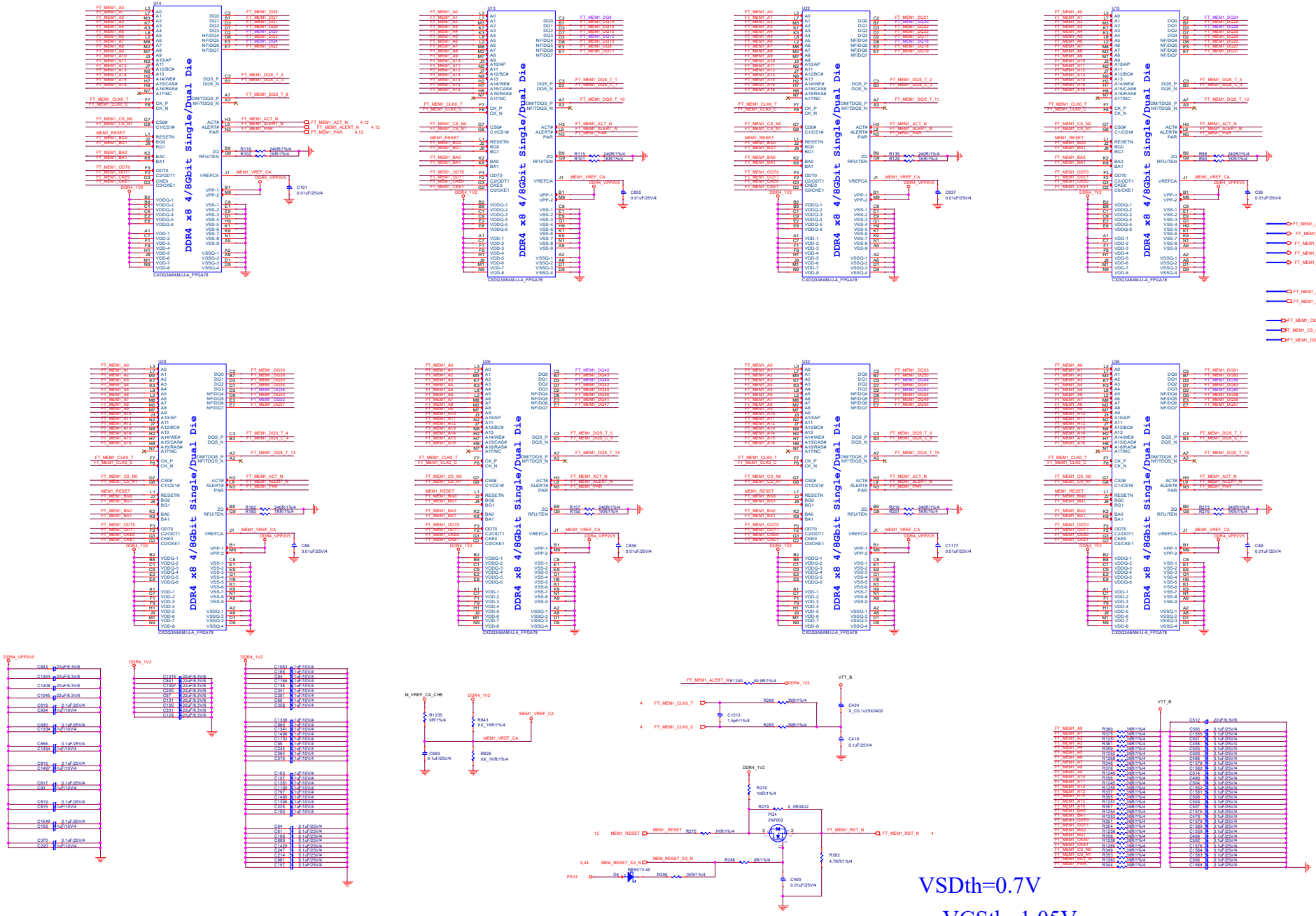

| | | |
|---|---|---|
| Title | <Title> | |
| Size C | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 8 of 64 | |




| | | | |
|---|---|---|---|
| Title | Henkun Electronics | | |
| Size | Document Number | ON-Board_DDR4 CHA_RANK0 | Rev 1.0 |
| Date: Saturday, April 19, 2025 | Sheet 9 of 64 | | |




| | |
|---|---|
| Title | Henkun Electronics |
| Size | Document Number: ON-Board_DDR4_CHA_RANK2 |
| Date: | SBC_9554 Sheet 10 of 64 |
| Saturday, April 19, 2025 | 1.0 |




| | |
|---|---|
| Title | Henkun Electronics |
| Size / Document Number | ON-Board_DDR4 CHB_RAM |
| Rev | 1.0 |
| Date: | Saturday, April 19, 2025 |
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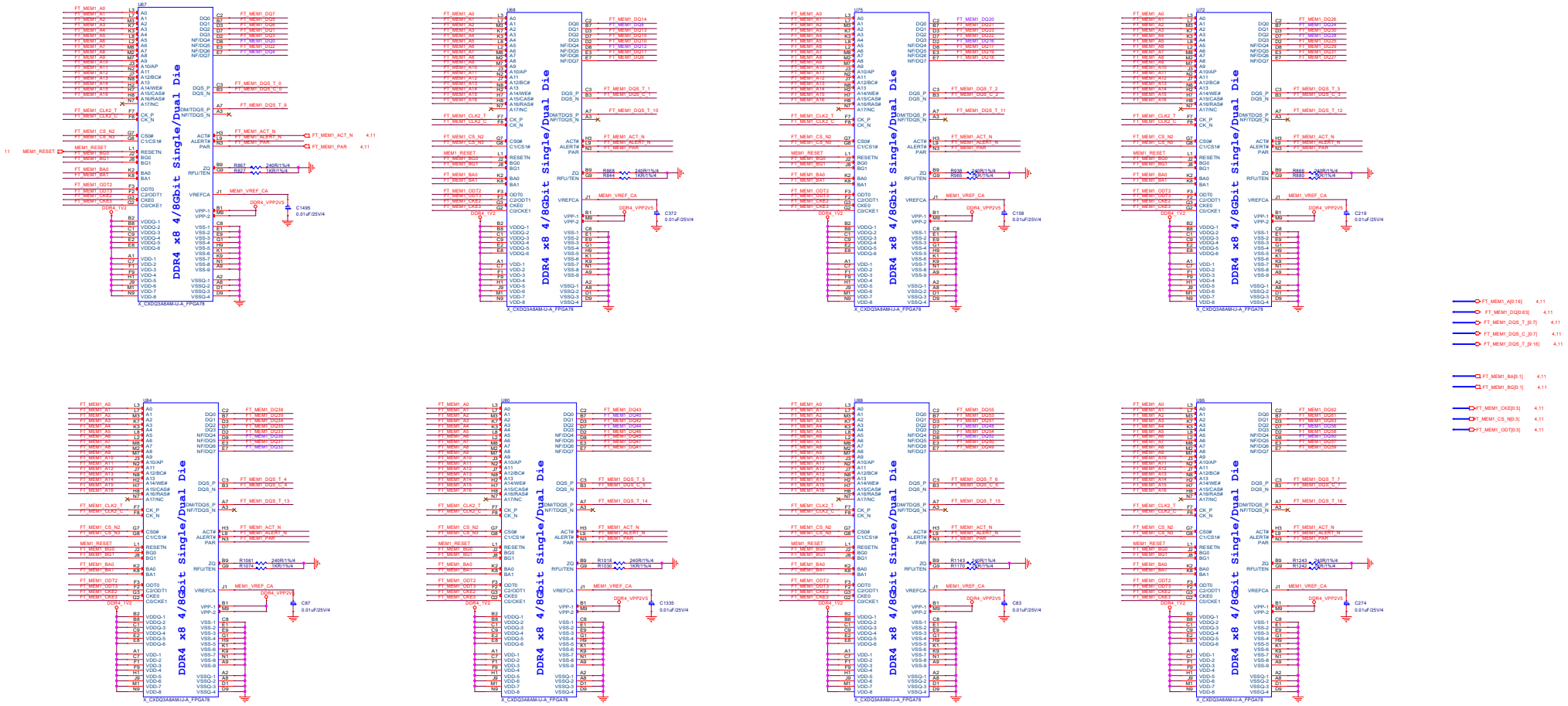
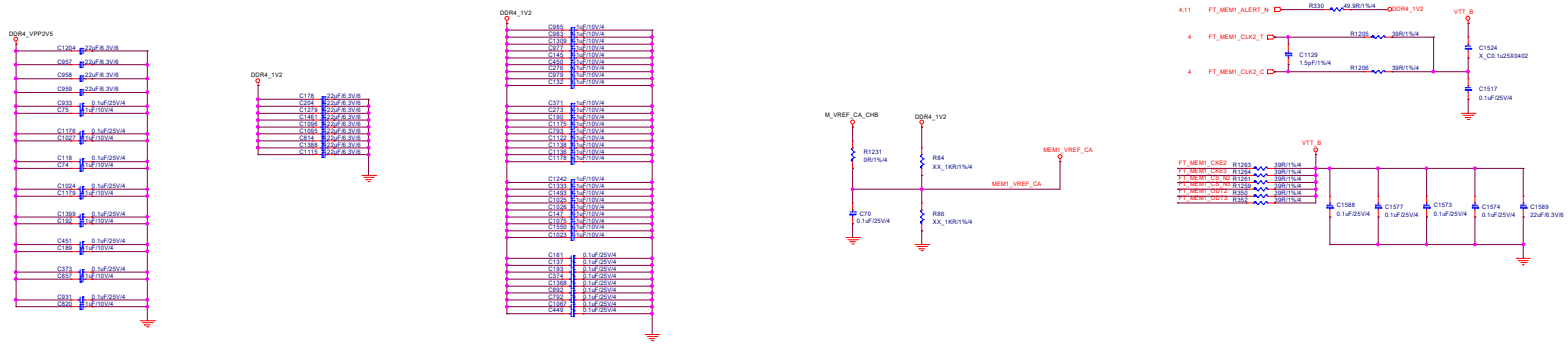
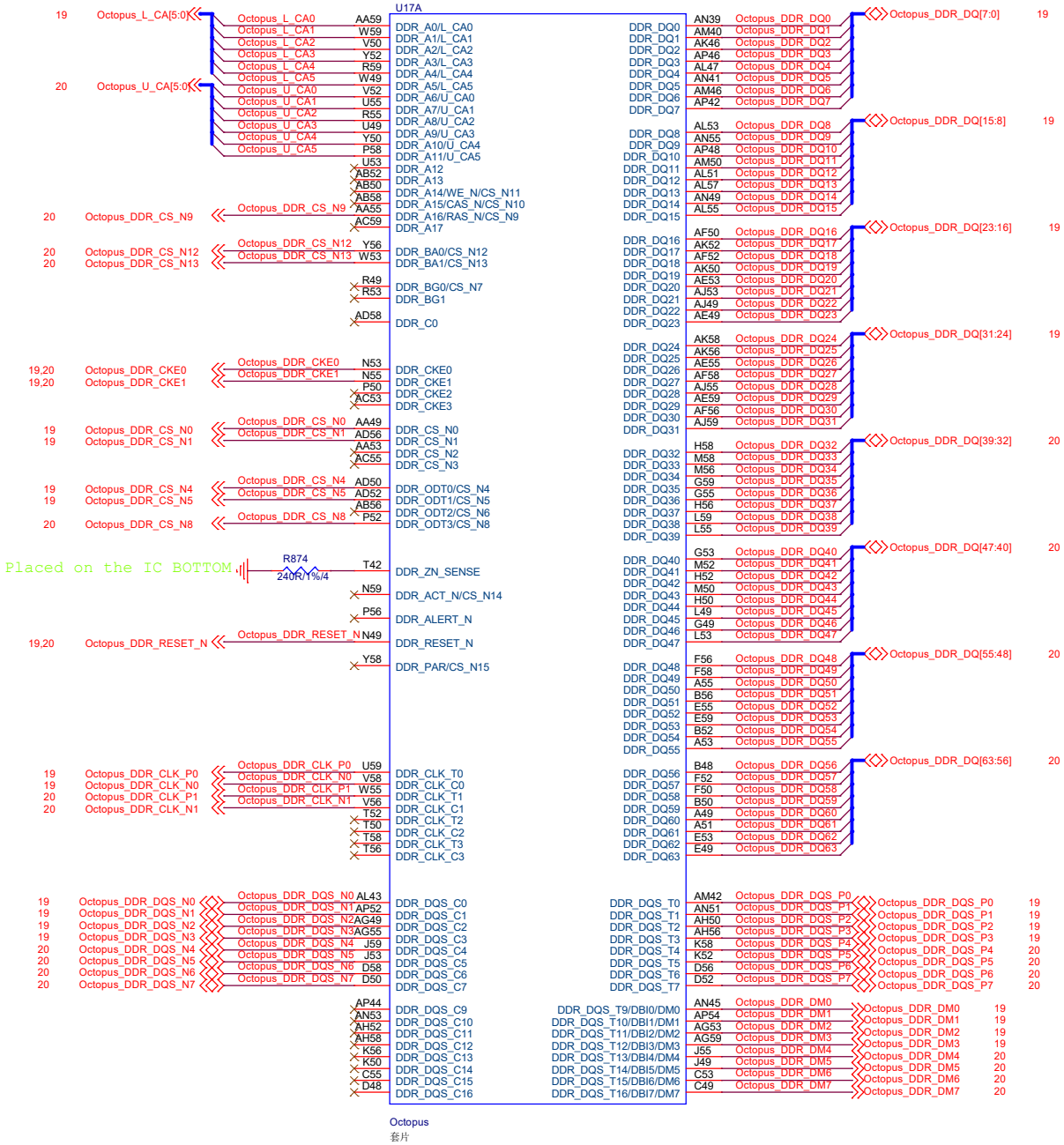



| | |
|---|---|
| Title | Henkun Electronics |
| Size | Document Number ON-Board_DDR4 CHB_RA[illegible]02 |
| Date: | SBC_0554 Sheet of 1.0 |
| Saturday, April 19, 2025 | 12 64 |




| | | | |
|---|---|---|---|
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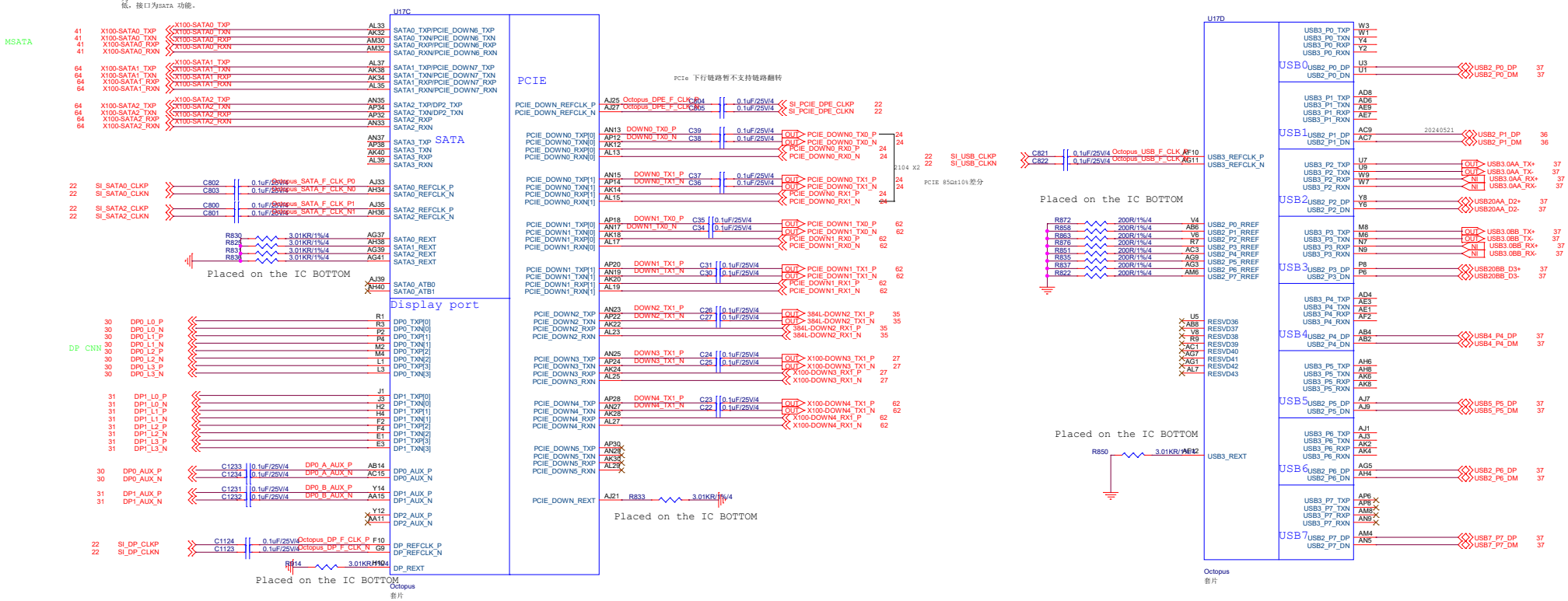
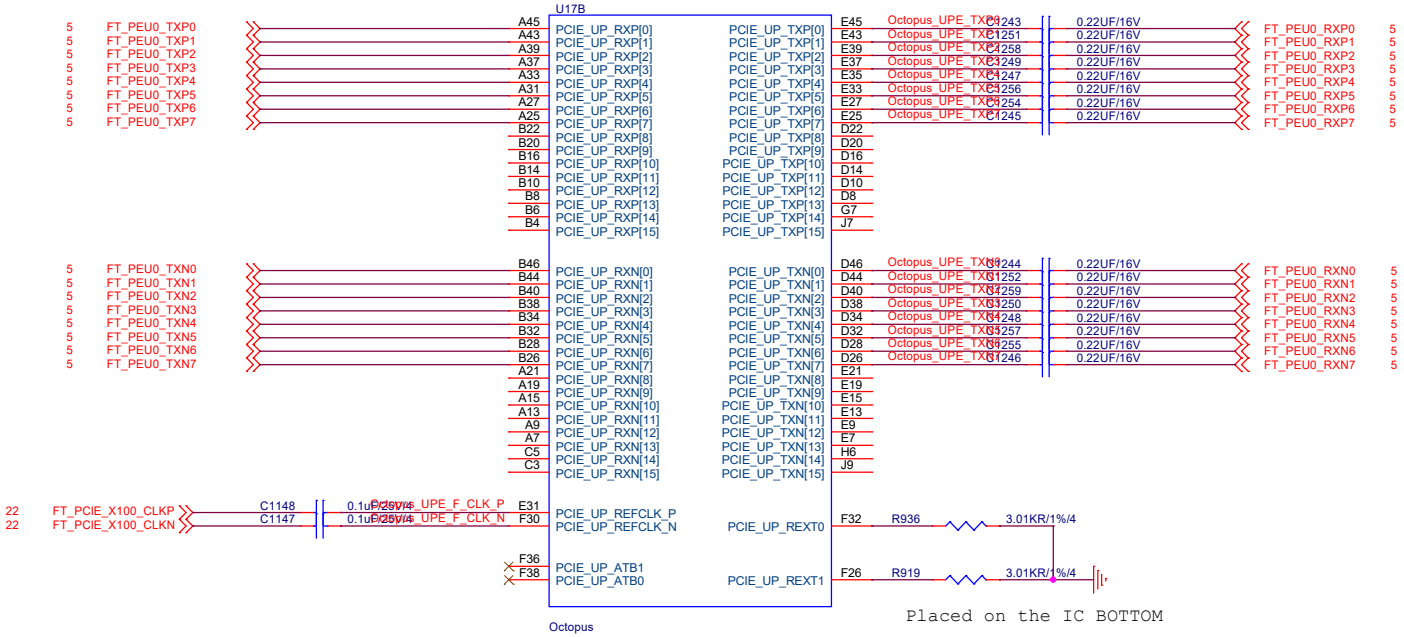
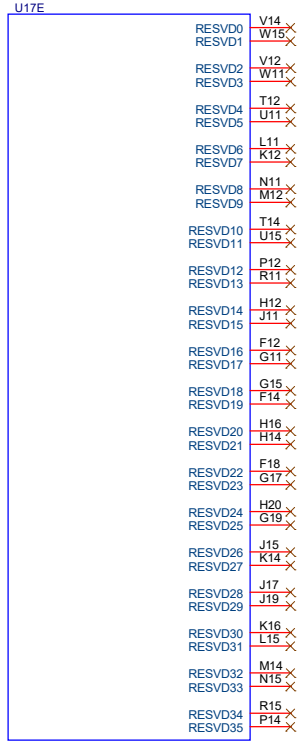
X100 PCIe 下行链路中PCIE_DOWN6 与PCIE_DOWN7 接口与SATA 复用
SATA0/PCIE_DOWN6 接口通过SP_DET0 检测插入设备类型。
SATA1/PCIE_DOWN7 接口通过SP_DET1 检测插入设备类型。
设备必须在系统上电前接入X100 的指定接口。
该类型接口不支持热插拔，系统启动后无法再自适应插入设备。
检测逻辑为：当检测到PEDET 为高，接口为PCIe 功能；当检测到PEDET 为
低，接口为SATA 功能。

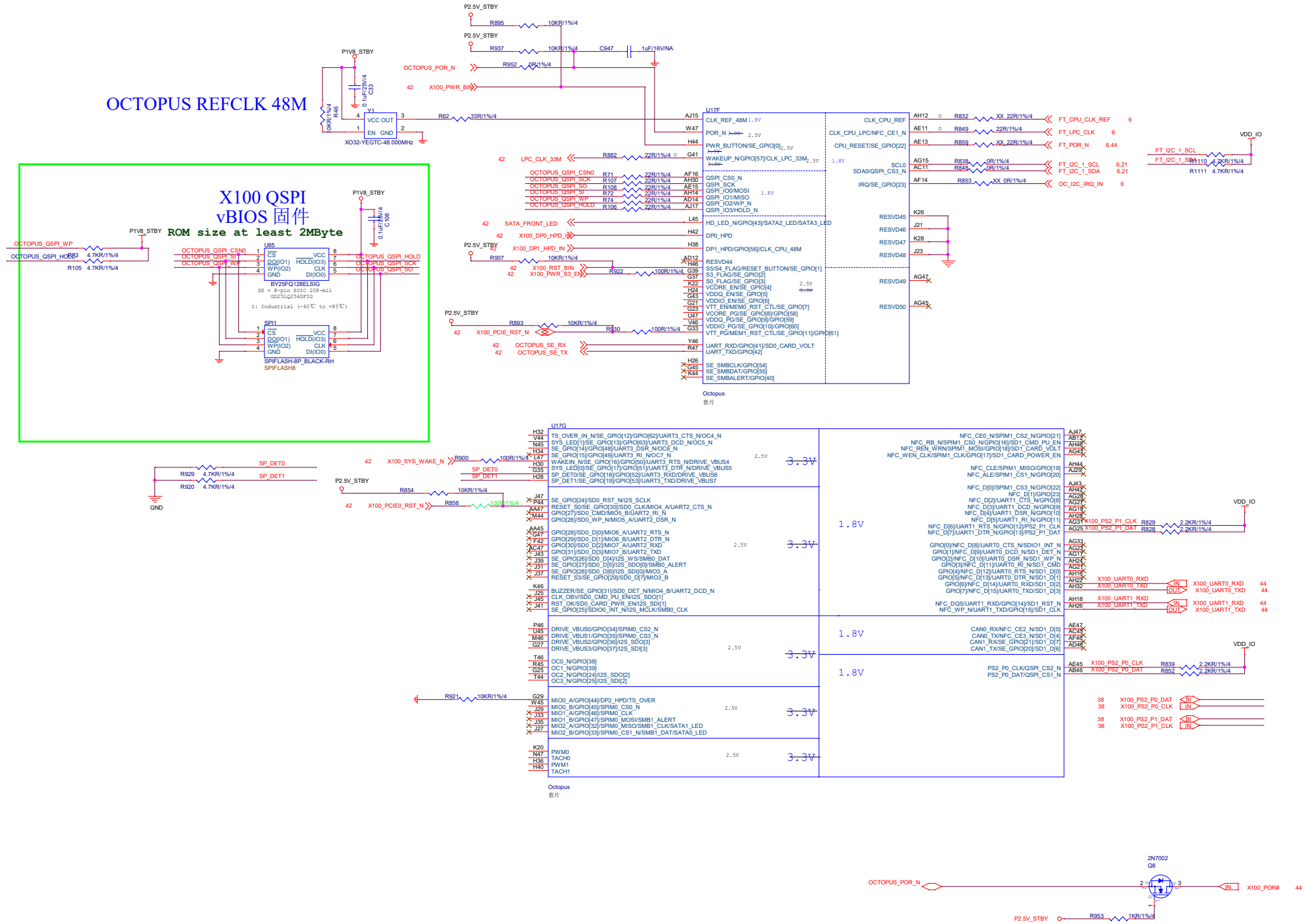



| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> |
| Rev | <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 14 of 64 |




| | | |
|---|---|---|
| Title <Title> | | |
| Size A3 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 15 of 64 | |


OCTOPUS REFCLK 48M
X100 QSPI
vBIOS 固件
ROM size at least 2MByte
U17F
Octopus
套片
U17G
Octopus
套片
2N7002
Q8
Title
<Title>
Size
A2
Document Number
<Doc>
Rev
<RevCode>
Date: Saturday, April 19, 2025
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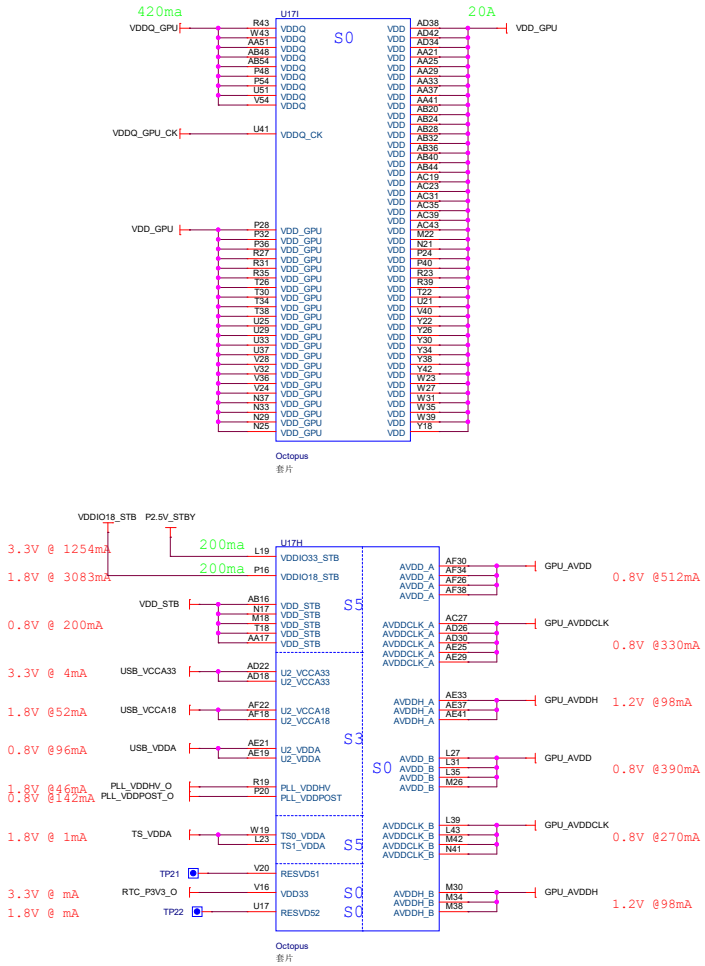
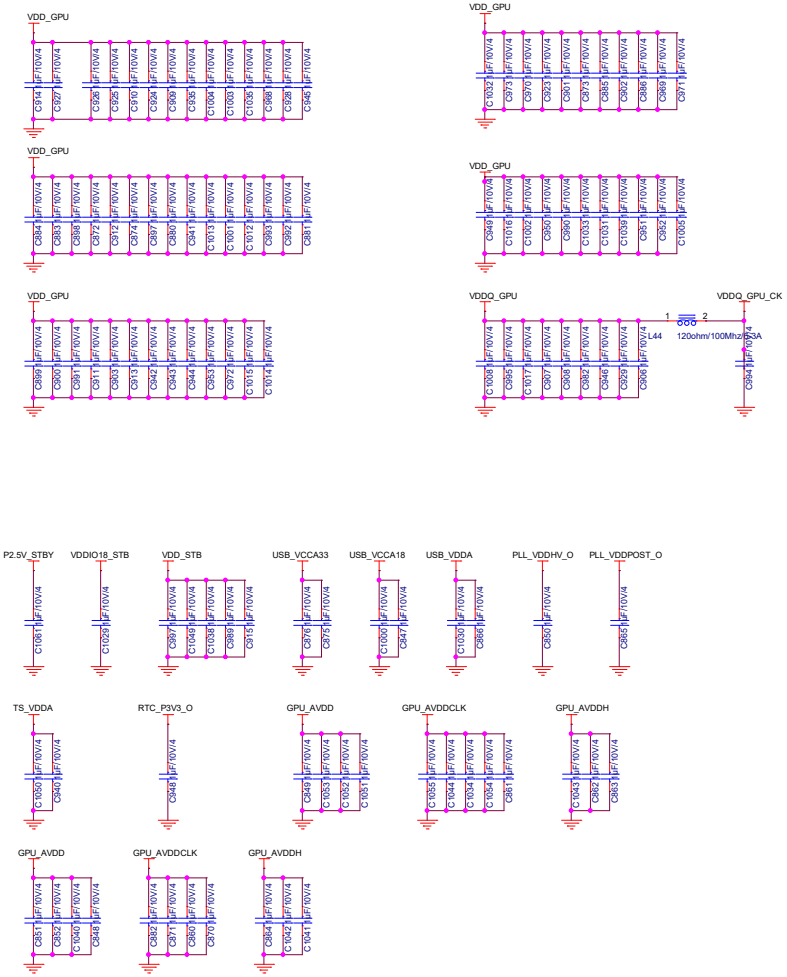
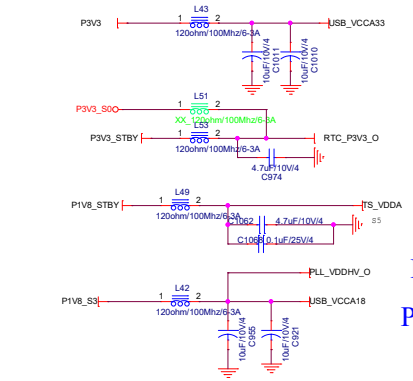


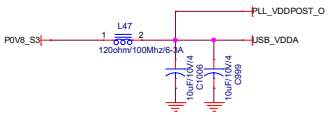

All the capacitors placed on the OCTPUS BOTTOM




P3V3_USB

P1V8_PLL

P1V8_USB




P0V8_PLL

P0V8_USB

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|---|---|---|---|
| Title <Title> | | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
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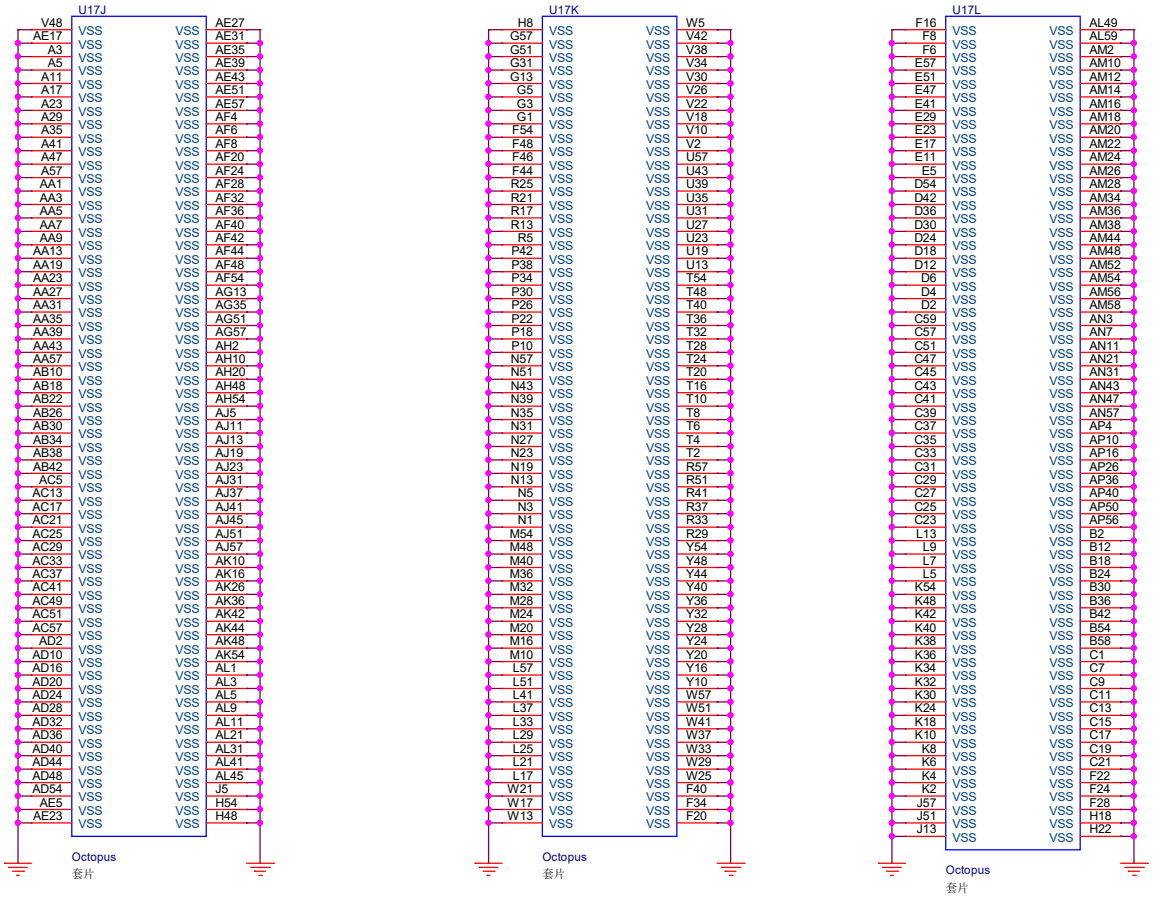
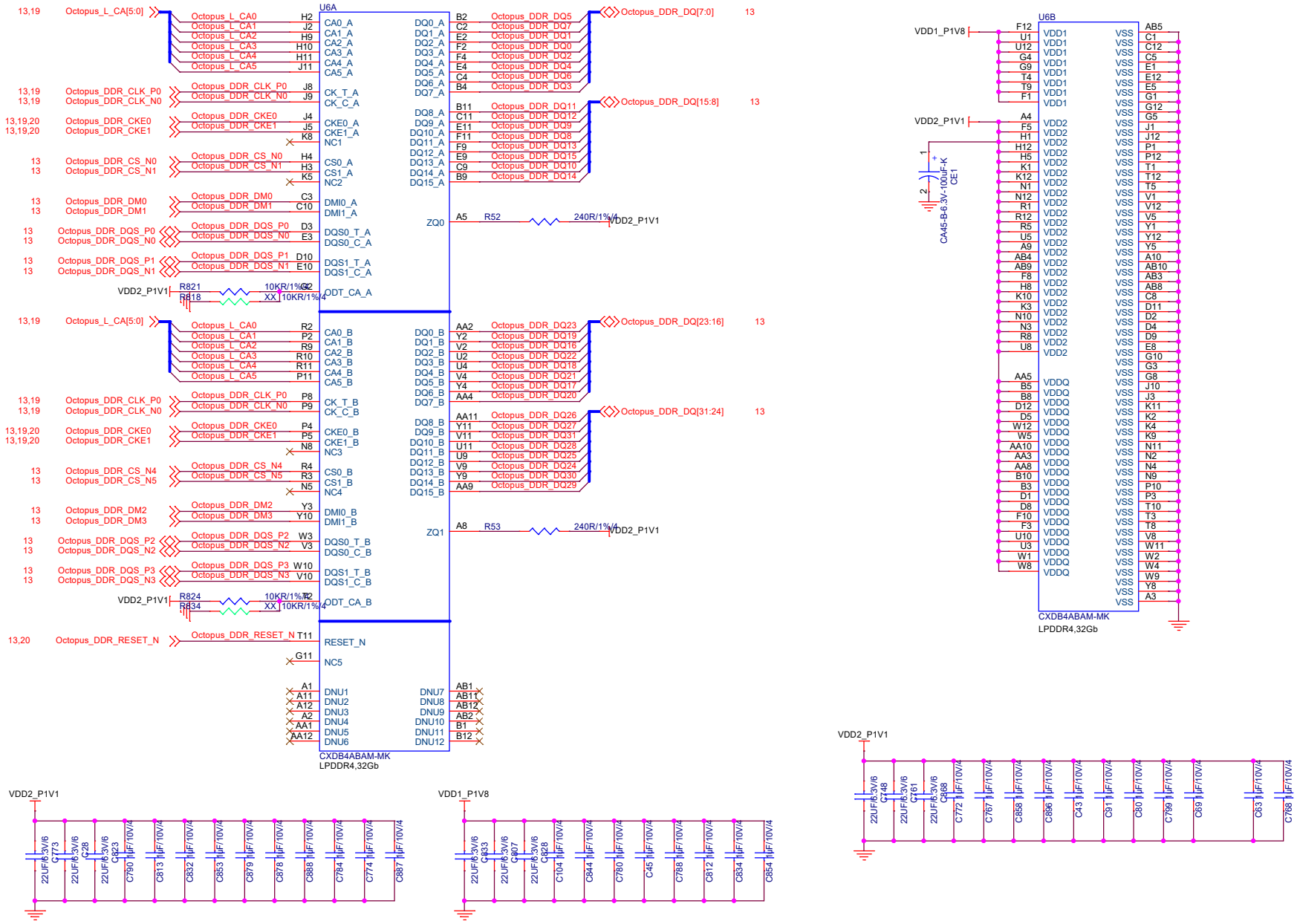
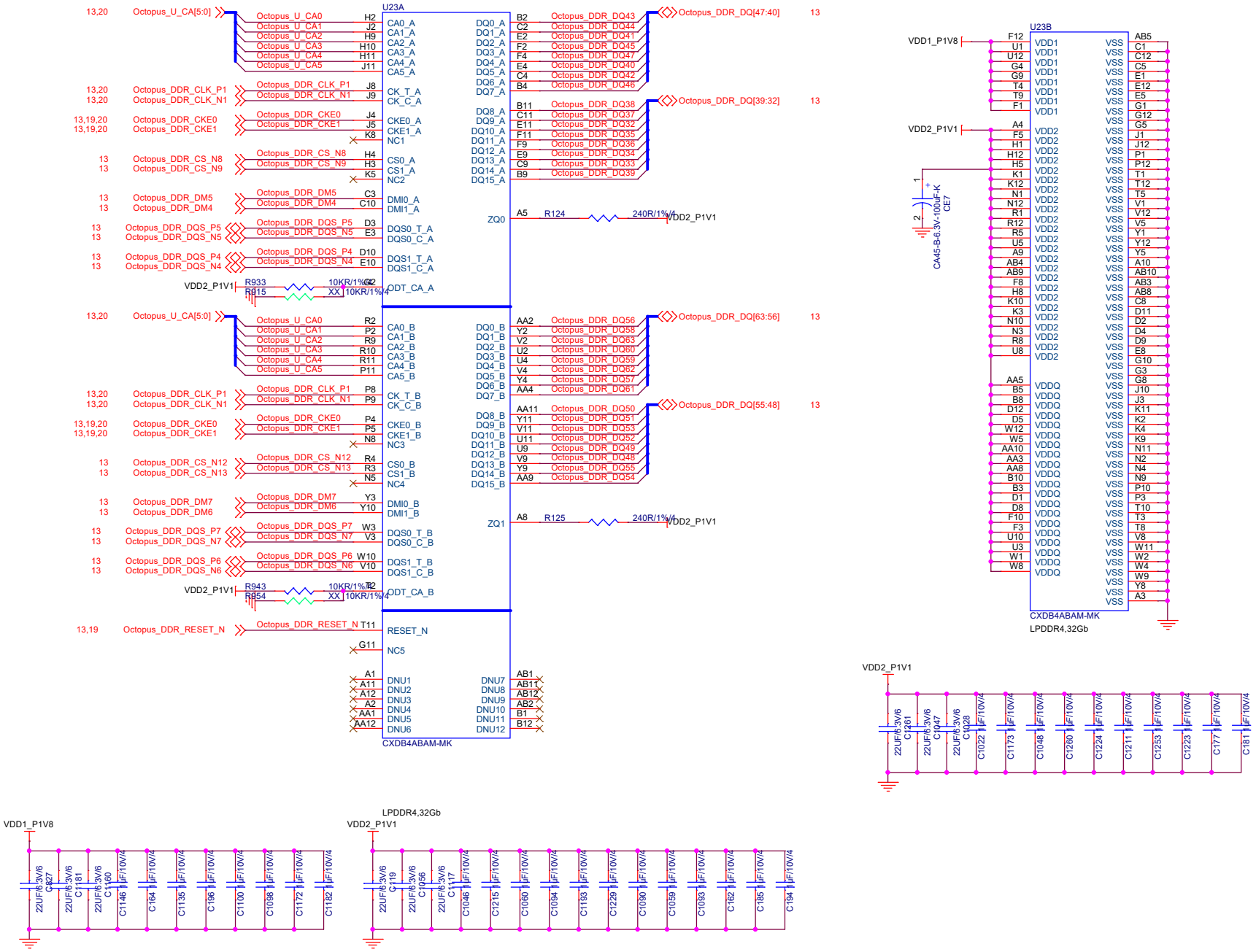



| | | |
|---|---|---|
| Title <Title> | | |
| Size A3 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 18 of 64 | |




| Title | <Title> | |
|---|---|---|
| Size A3 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 19 of 64 | |




Cap Place next U5

| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A3 | Document Number <Doc> | | Rev <RevCode> |
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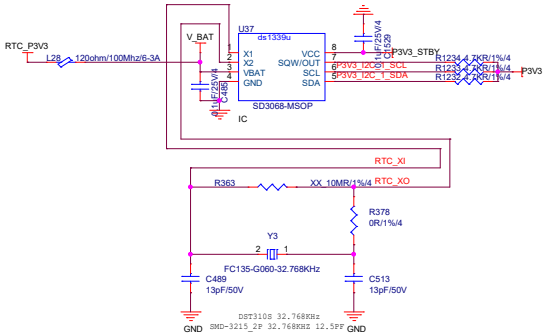
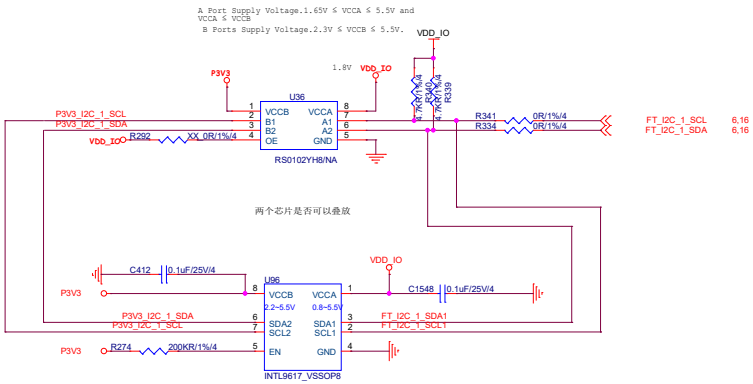
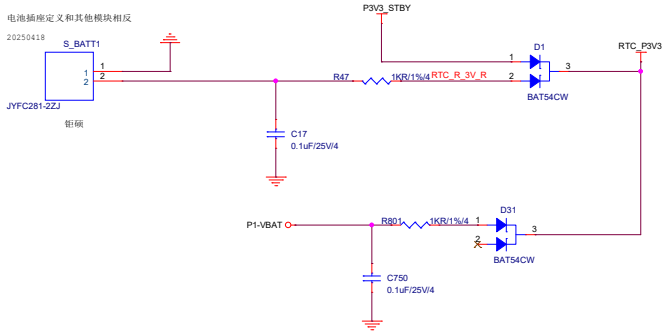


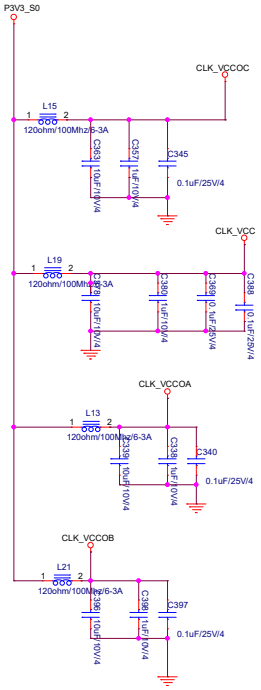

# RTC

# FT I2C1

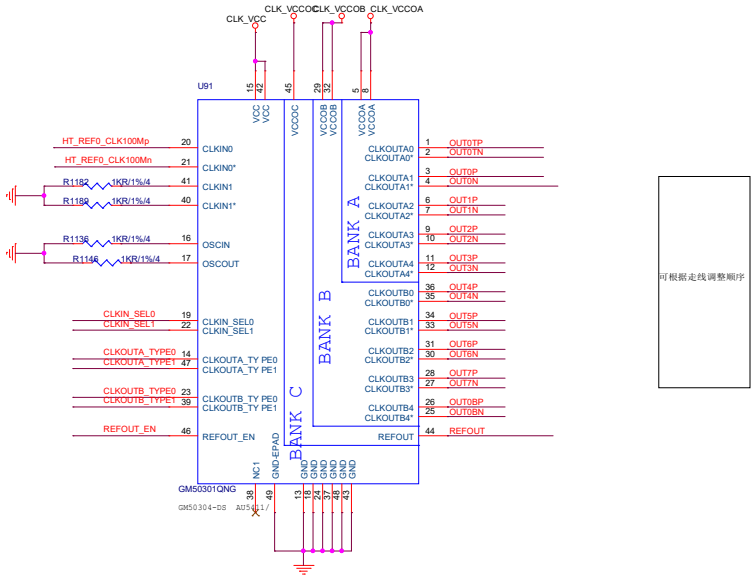


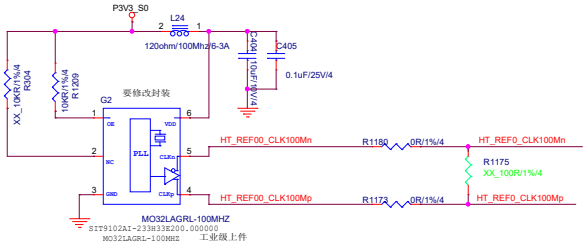

| | | |
|---|---|---|
| Title | <Title> | |
| Size A2 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 21 of 64 | |

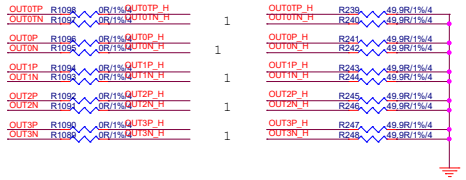


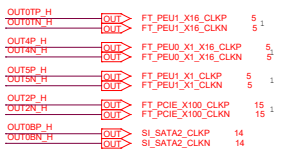

Close to chip

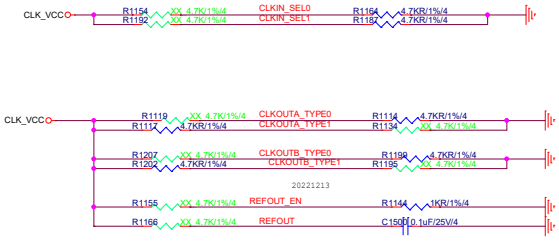


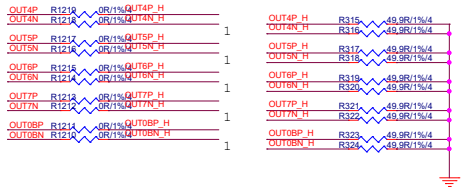

可根据走线调整顺序

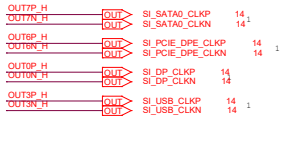



HCSL_DC_Couple(Refer to datasheet)

| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
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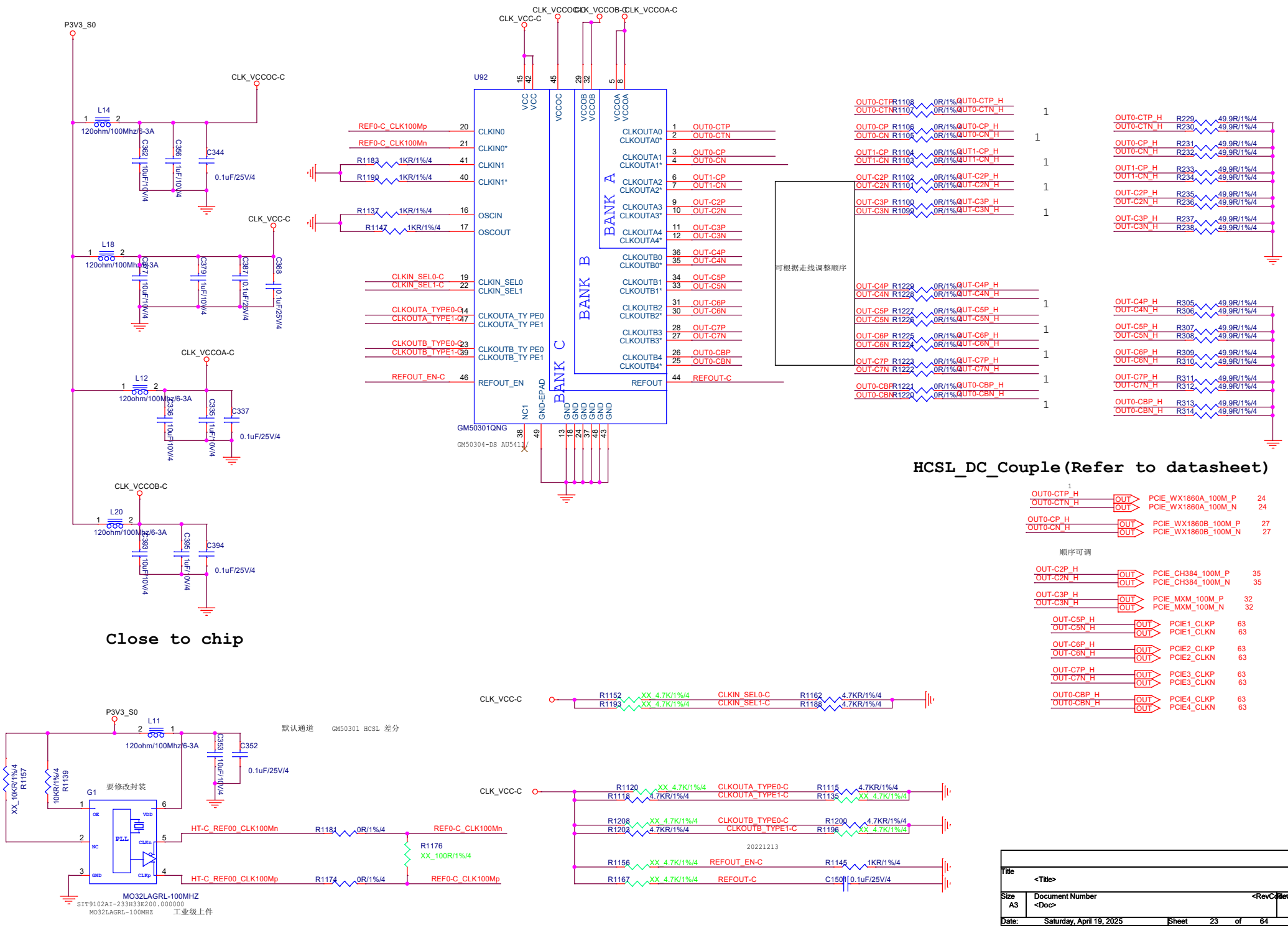
P3V3_S0
CLK_VCCOC-C
CLK_VCC-C
CLK_VCCOA-C
CLK_VCCOB-C
L14
120ohm/100Mhz/6-3A
L18
L12
L20
C344
C337
C394
0.1uF/25V/4
U92
GM50301QNG
GM50304-DS AU5413
CLKIN0
CLKIN0*
CLKIN1
CLKIN1*
OSCIN
OSCOUT
CLKIN_SEL0
CLKIN_SEL1
CLKOUTA_TY PE0
CLKOUTA_TY PE1
CLKOUTB_TY PE0
CLKOUTB_TY PE1
REFOUT_EN
REFOUT
BANK A
BANK B
BANK C
REF0-C_CLK100Mp
REF0-C_CLK100Mn
CLKIN_SEL0-C
CLKIN_SEL1-C
CLKOUTA_TYPE0-C
CLKOUTA_TYPE1-C
CLKOUTB_TYPE0-C
CLKOUTB_TYPE1-C
REFOUT_EN-C
REFOUT-C
可根据走线调整顺序
HCSL_DC_Couple(Refer to datasheet)
Close to chip
顺序可调
PCIE_WX1860A_100M_P
PCIE_WX1860A_100M_N
PCIE_WX1860B_100M_P
PCIE_WX1860B_100M_N
PCIE_CH384_100M_P
PCIE_CH384_100M_N
PCIE_MXM_100M_P
PCIE_MXM_100M_N
PCIE1_CLKP
PCIE1_CLKN
PCIE2_CLKP
PCIE2_CLKN
PCIE3_CLKP
PCIE3_CLKN
PCIE4_CLKP
PCIE4_CLKN
默认通道
GM50301 HCSL 差分
要修改封装
G1
MO32LAGRL-100MHZ
SIT9102AI-233H33E200.000000
MO32LAGRL-100MHZ
工业级上件
HT-C_REF00_CLK100Mn
HT-C_REF00_CLK100Mp
REF0-C_CLK100Mn
REF0-C_CLK100Mp
20221213
Title
<Title>
Size
A3
Document Number
<Doc>
<RevCode>
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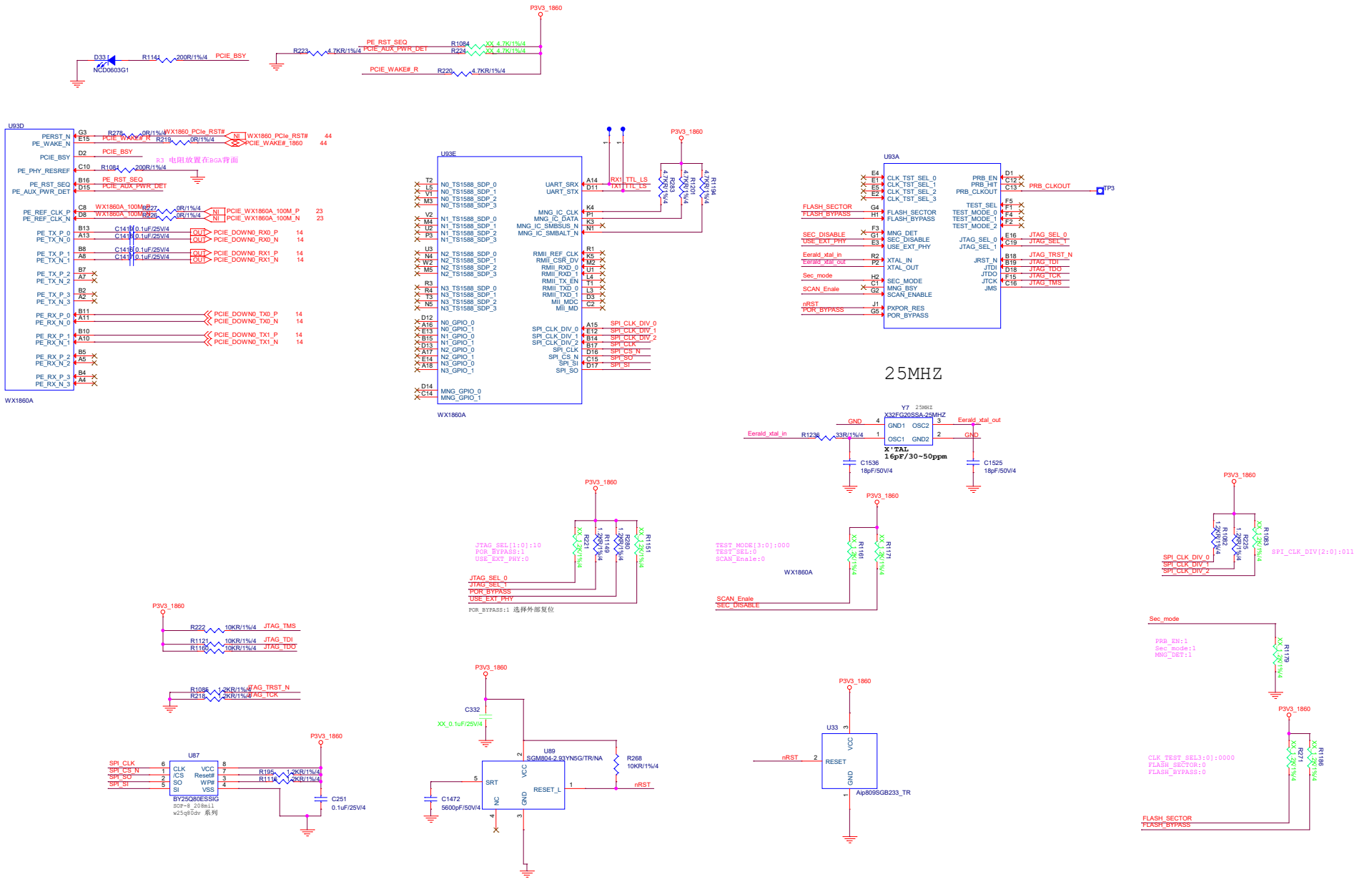
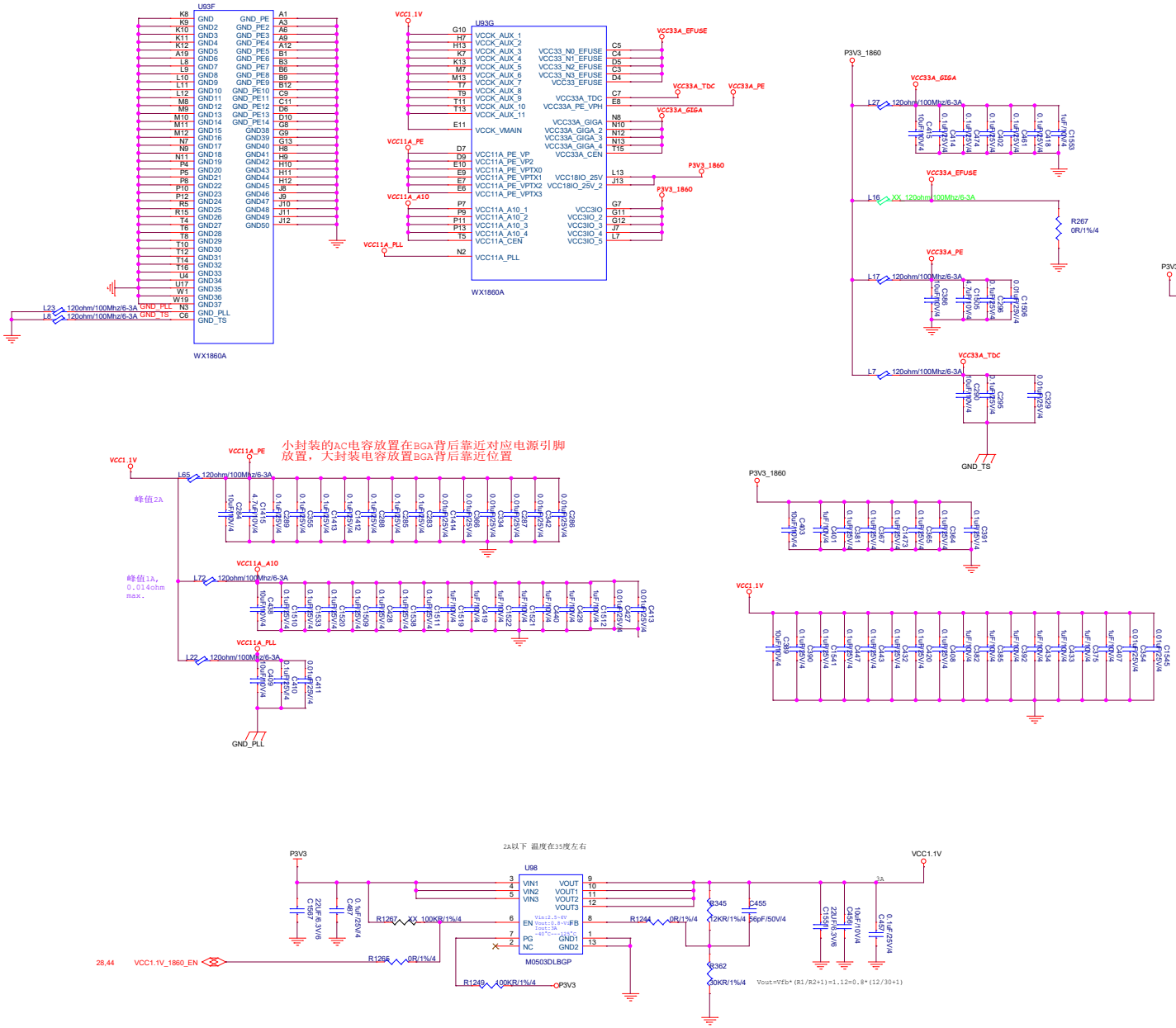



| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 24 of 64 | | |




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
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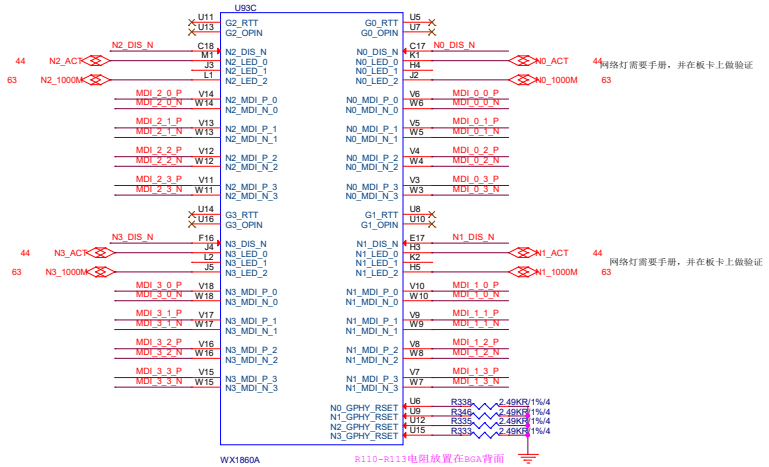


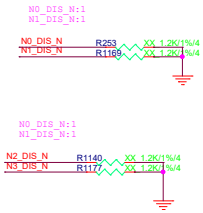


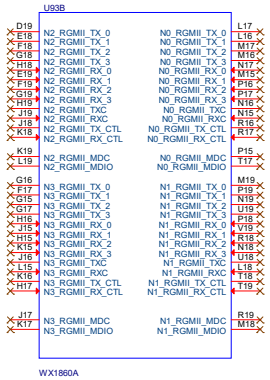


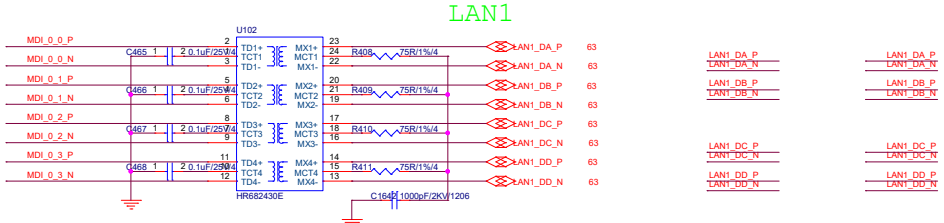


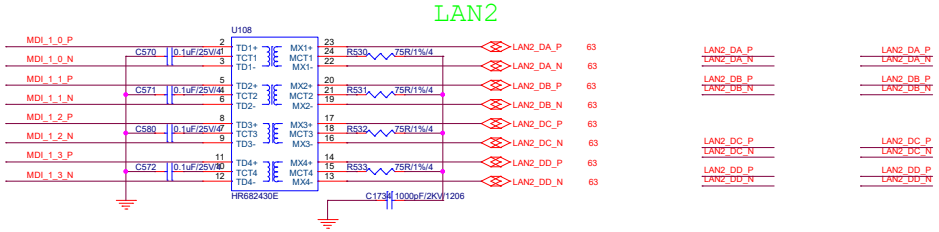


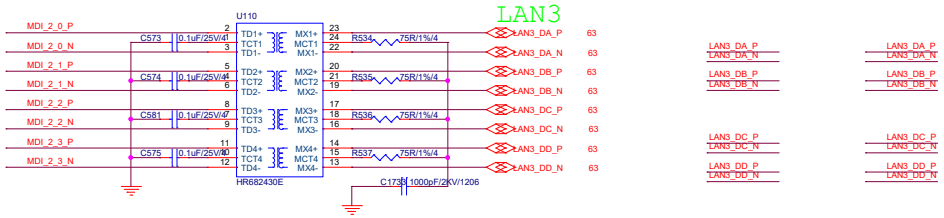


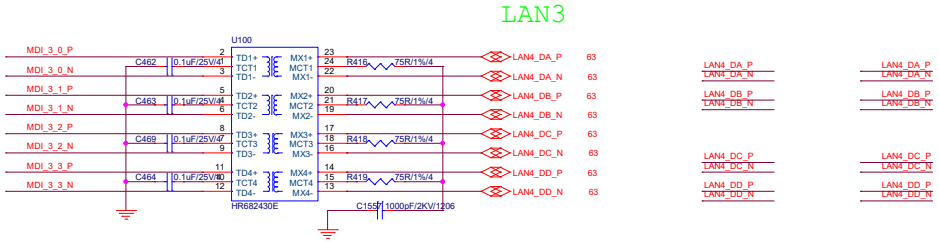


| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
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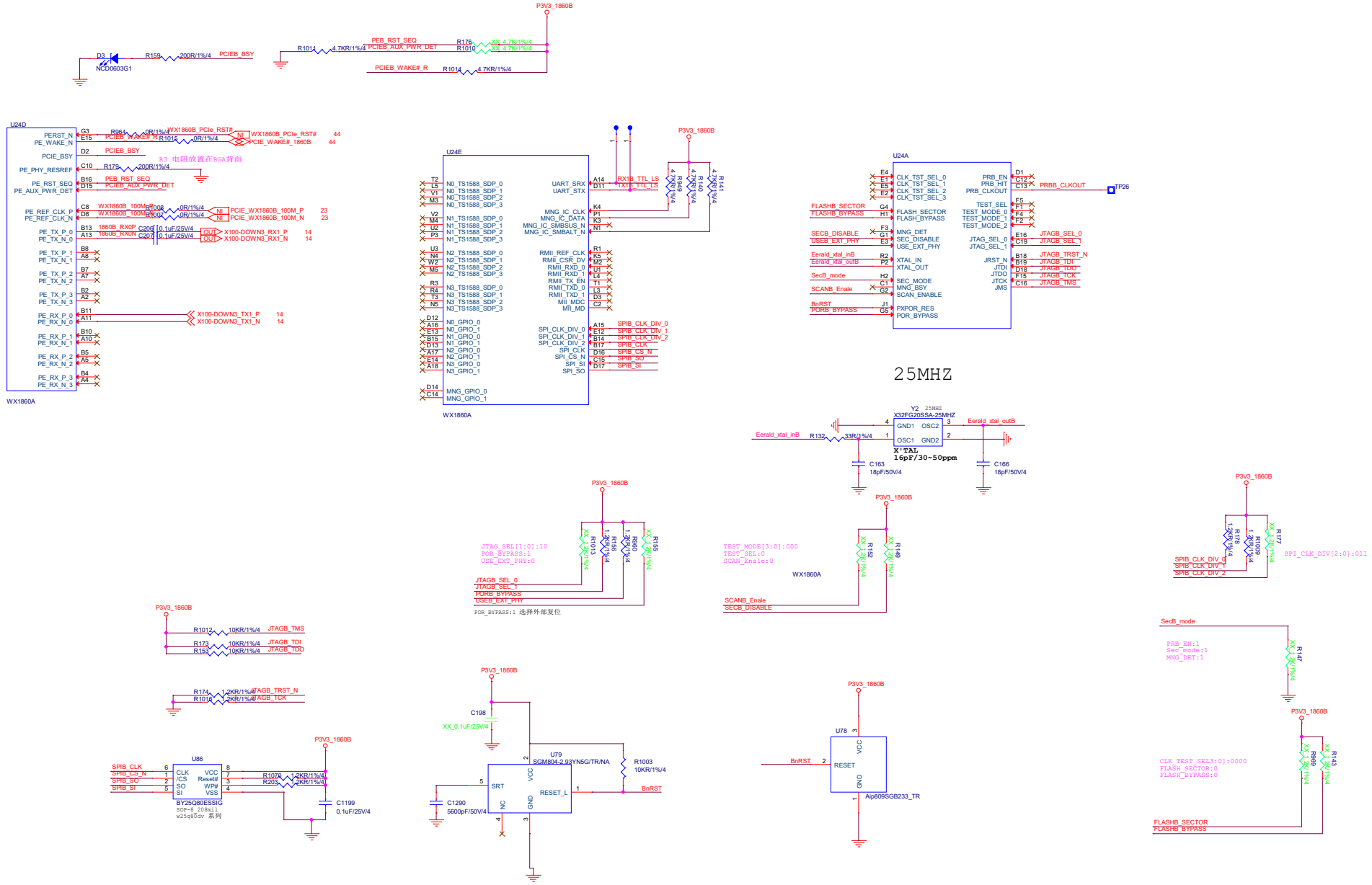
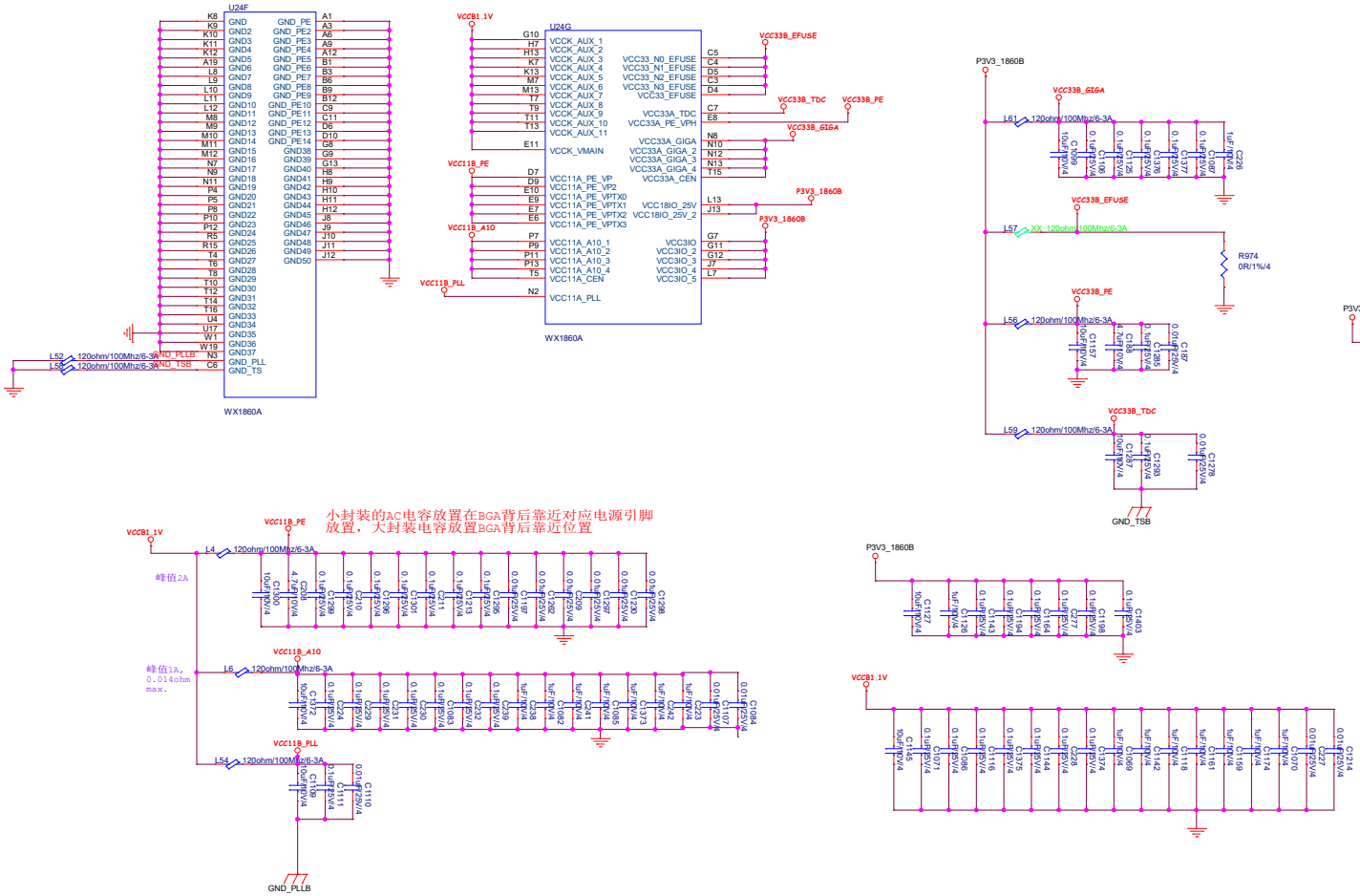
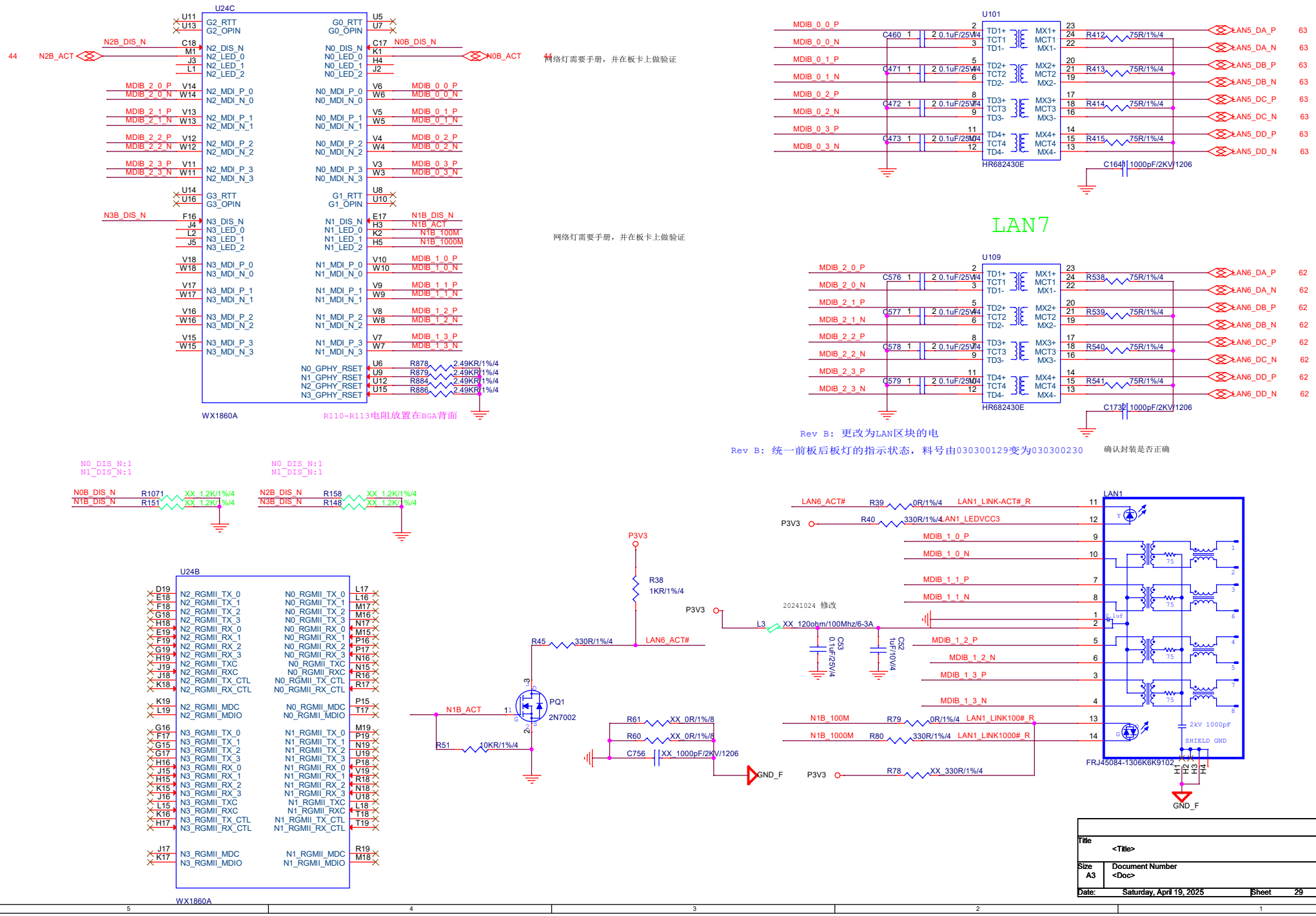



| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 27 of 64 | | |



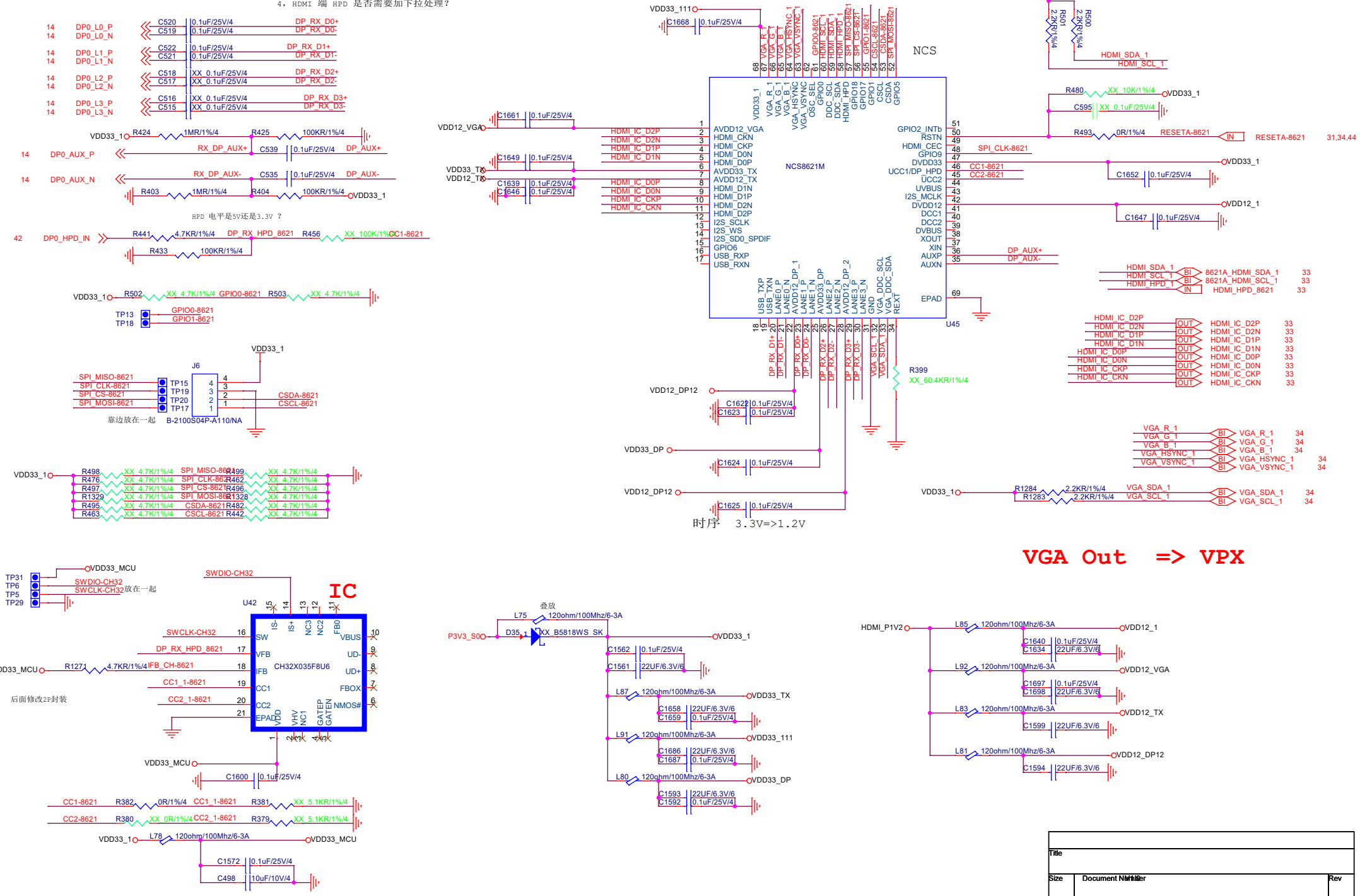

| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 28 of 64 | | |




| | | |
|---|---|---|
| Title | <Title> | |
| Size A3 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 29 of 64 | |

# DP Input

应用场景：配合飞腾X100 DP转HDMI ,VGA使用
问题点：
1, DP端的HDP 电平为3.3V吗？
2, 无时序关系吗？目前打算设计3.3V>1.2V, 无reset?
3, VGA输出，不需要75欧姆阻抗匹配吗？参考设计是不上件，VGA 直出，是否加电感等进行去除干扰滤波等？
4, 芯片是否有ESD功能？参考设计VGA未加ESD处理？
4, HDMI 端 HPD 是否需要加下拉处理？




| | |
|---|---|
| Title | |
| Size | Document Number Rev |
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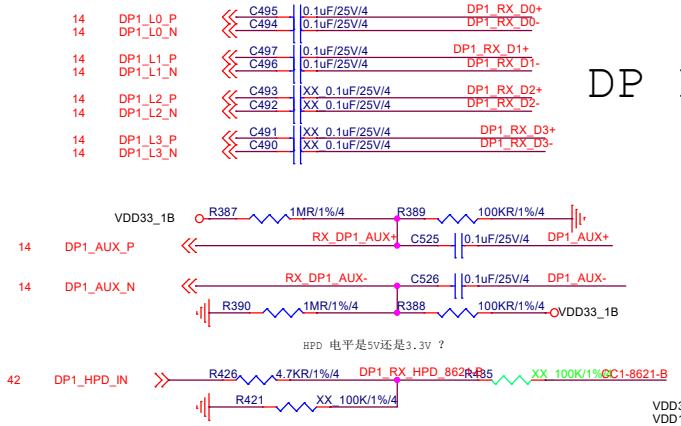
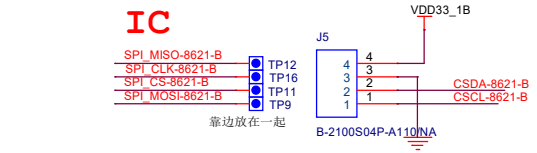
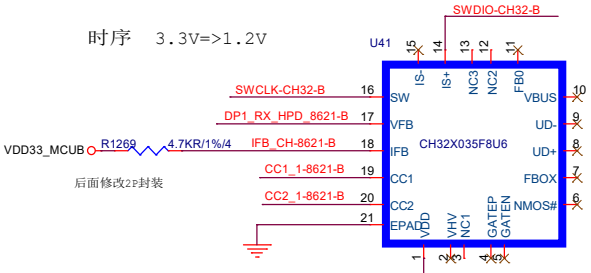
应用场景：配合飞腾X100 DP转HDMI ,VGA使用
问题点：
1, DP端的HDP 电平为3.3V吗？
2, 无时序关系吗？目前打算设计3.3V>1.2V, 无reset?
3, VGA输出，不需要75欧姆阻抗匹配吗？参考设计是不上件，VGA 直出，是否加电感等进行去除干扰滤波等？
4, 芯片是否有ESD功能？参考设计VGA未加ESD处理？
4, HDMI 端 HPD 是否需要加下拉处理？

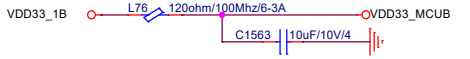
# DP Input

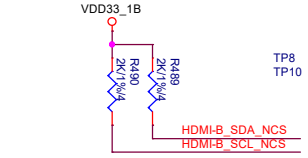


时序 3.3V=>1.2V



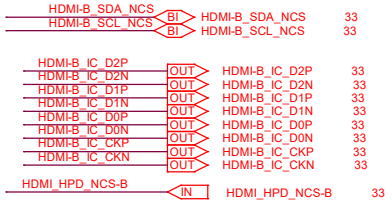


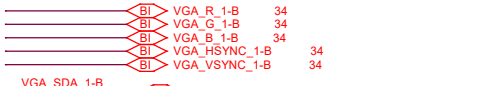



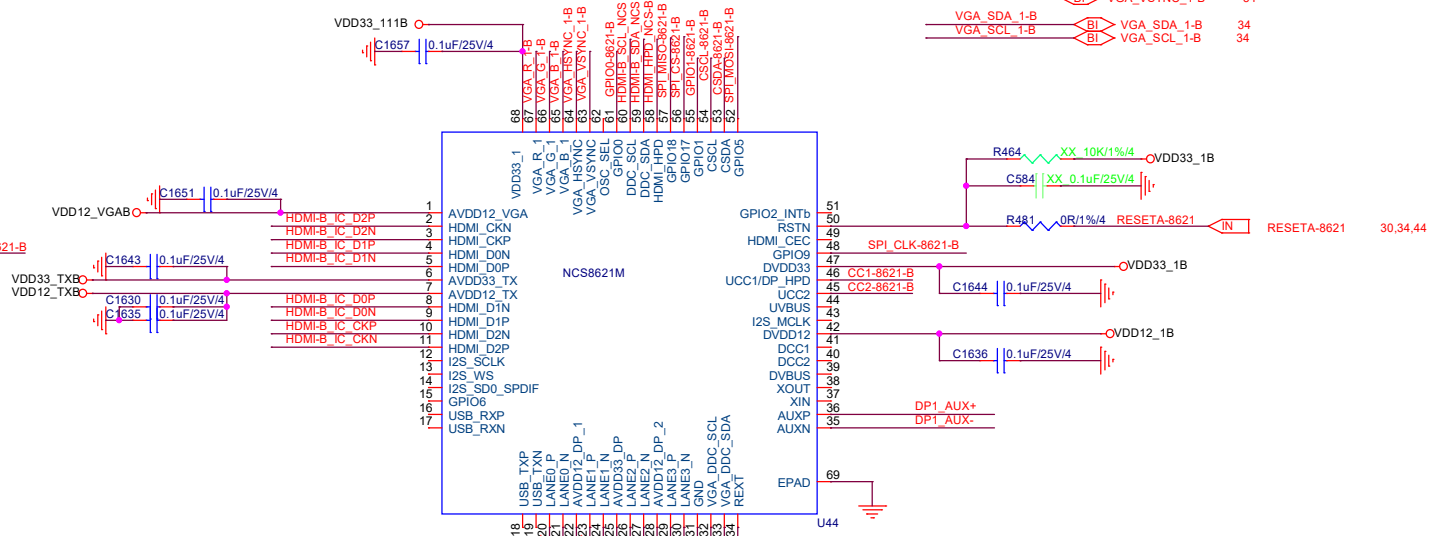


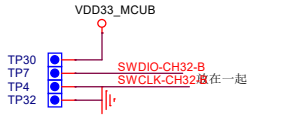


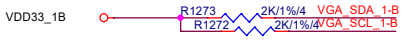


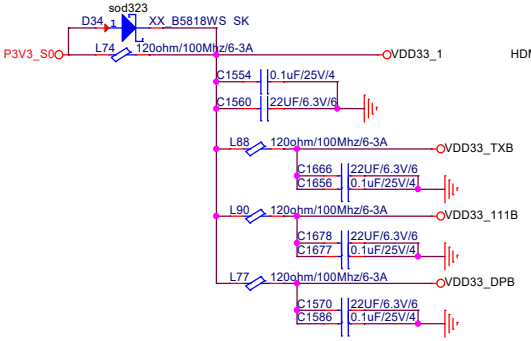



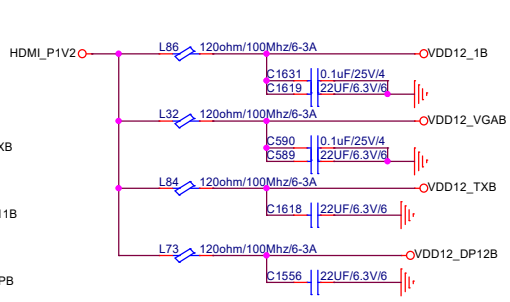




| | | | |
|---|---|---|---|
| Title | | | |
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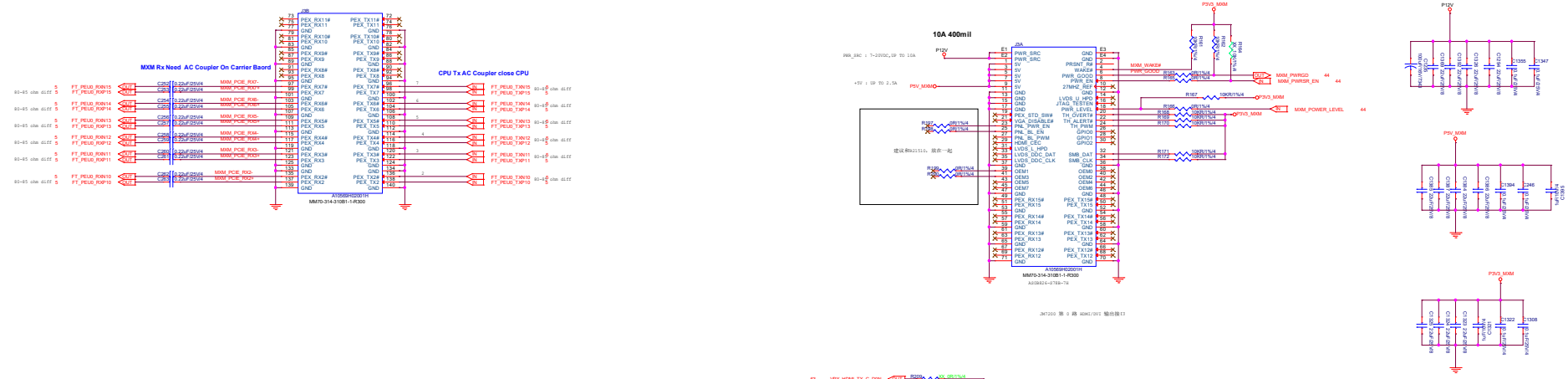
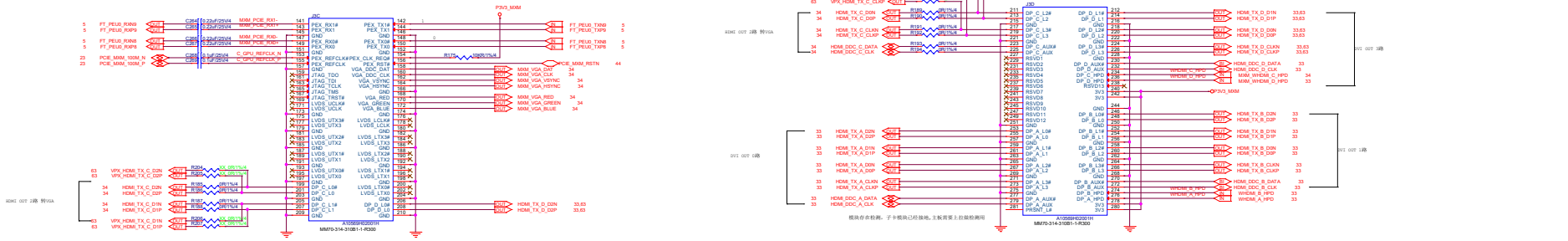
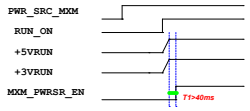



From CPLD
Chipset S3 Delay 20mS

## Power-Up Sequence For MXM




| | | | |
|---|---|---|---|
| Title: <Title> | | | |
| Size: A1 | Document Number: <Doc> | | Rev: <RevCode> |
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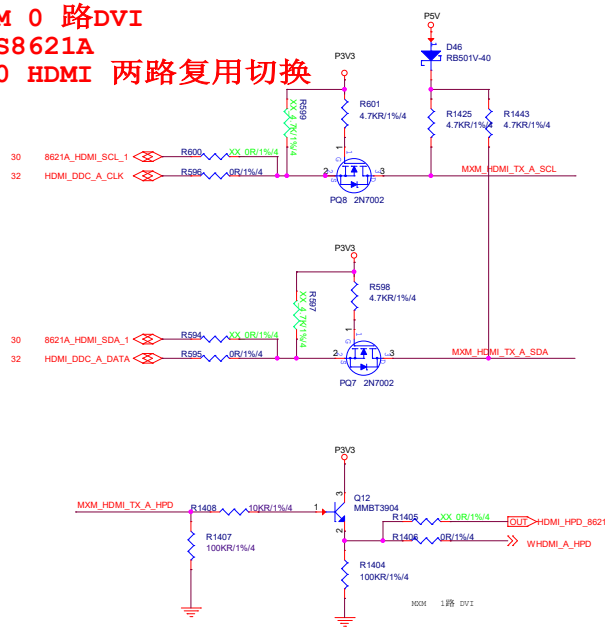
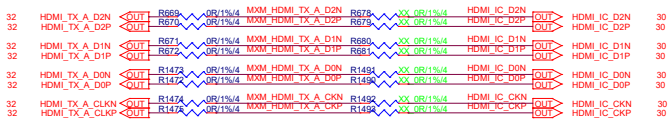
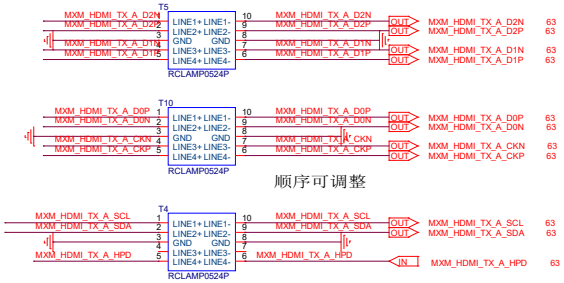
# MXM 0 路DVI
# NCS8621A
# DP0 HDMI 两路复用切换




电阻叠放

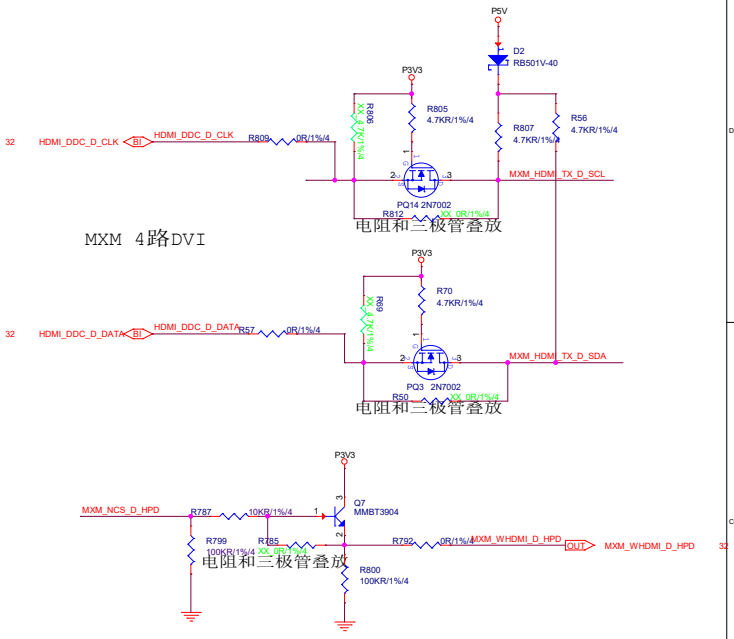



## HDMI Out--VPX接口

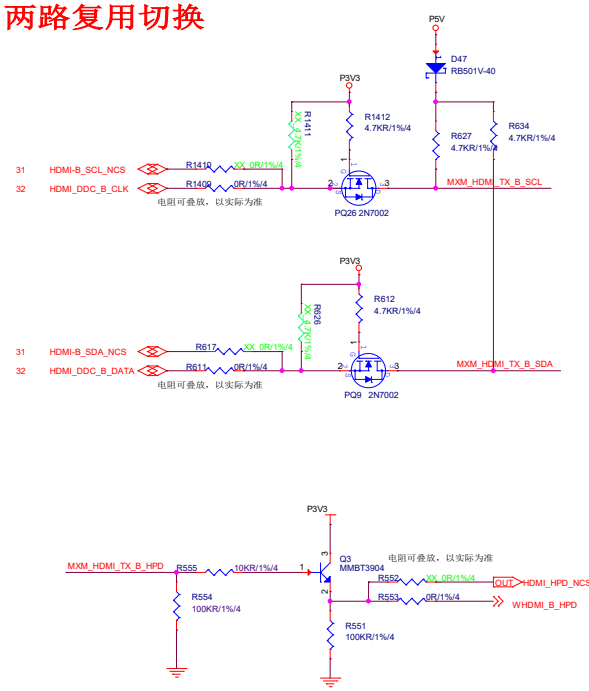



顺序可调整

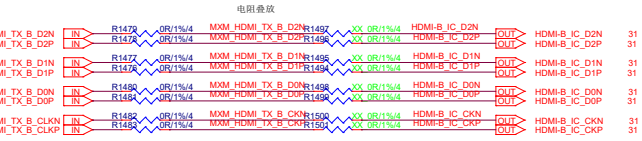
# MXM 4路DVI



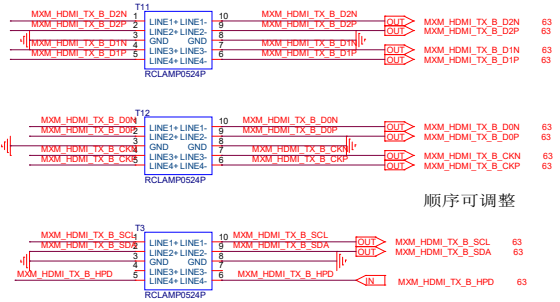

# MXM 1路DVIMXM
# NCS8621B DP1 HDMI
# 两路复用切换




电阻叠放



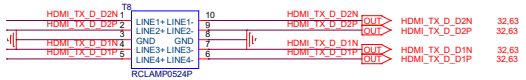

## HDMI Out--VPX接口

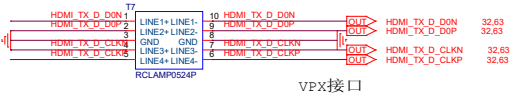



顺序可调整

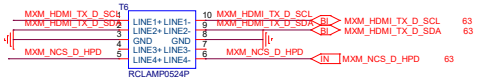



顺序可调整




VPX接口

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| Title | <Title> | |
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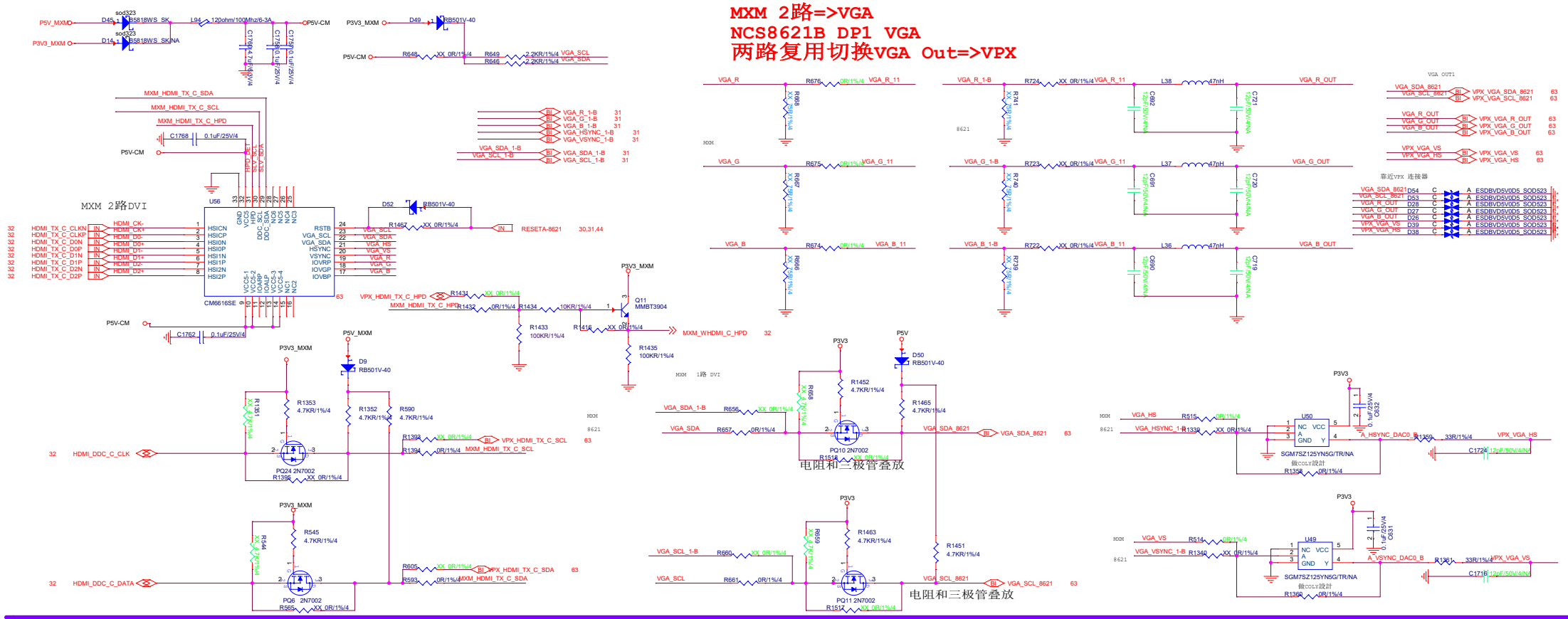
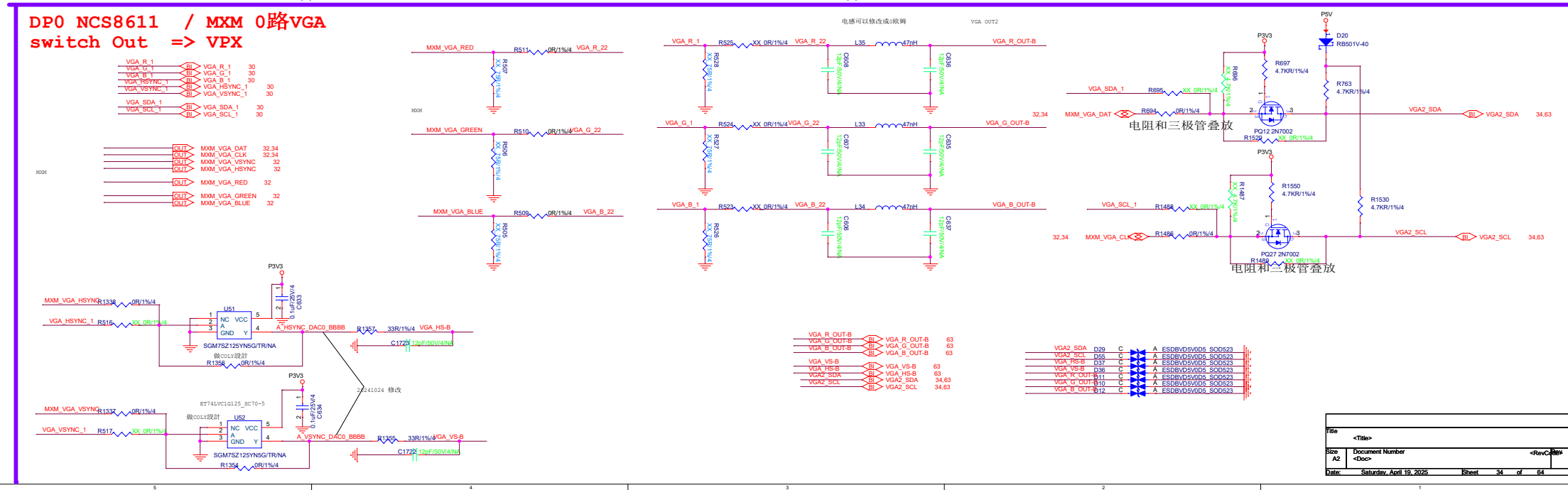
# MXM 2路=>VGA
# NCS8621B DP1 VGA
# 两路复用切换VGA Out=>VPX




# DP0 NCS8611 / MXM 0路VGA
# switch Out => VPX




| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> <RevCode> |
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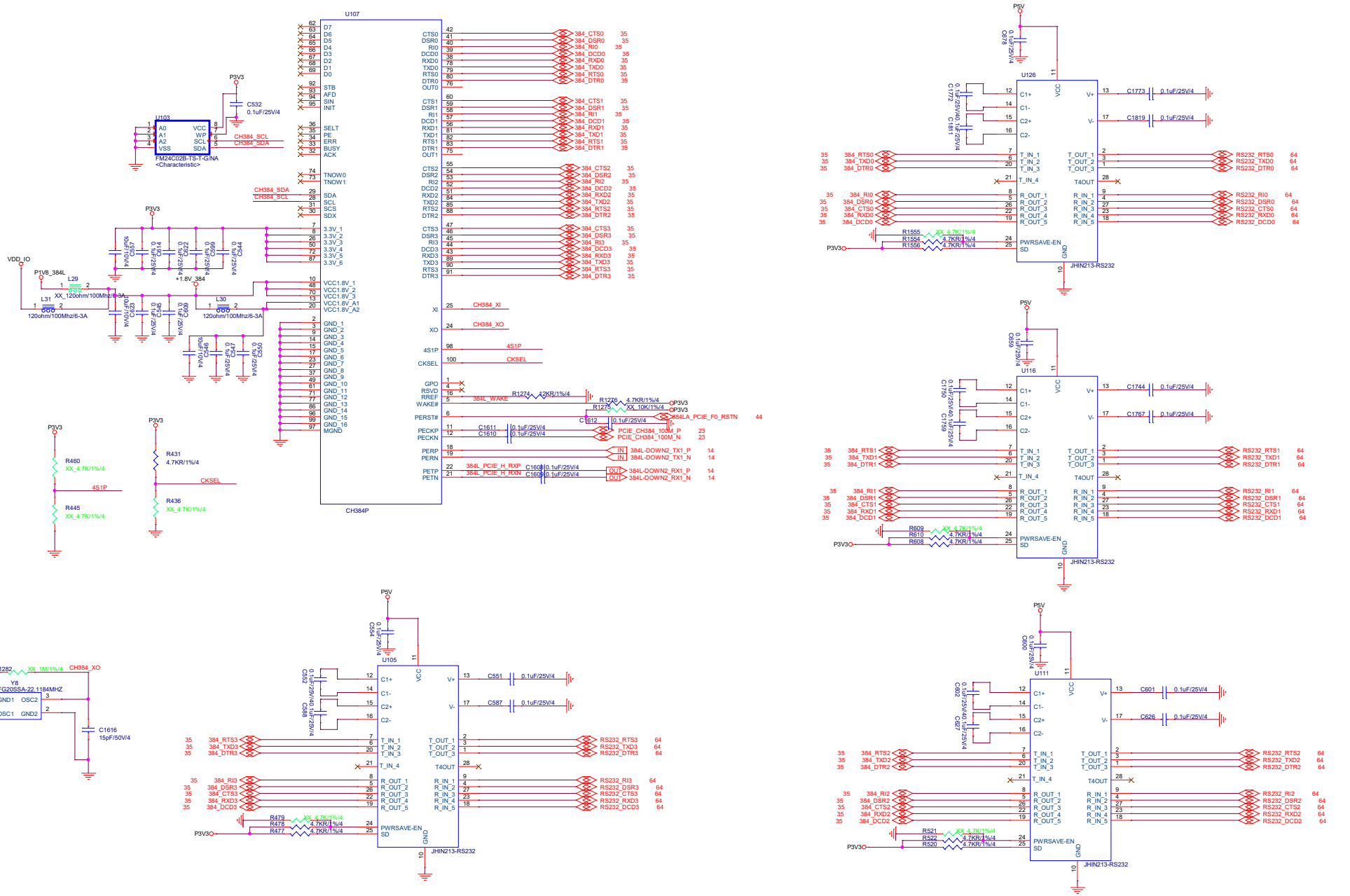
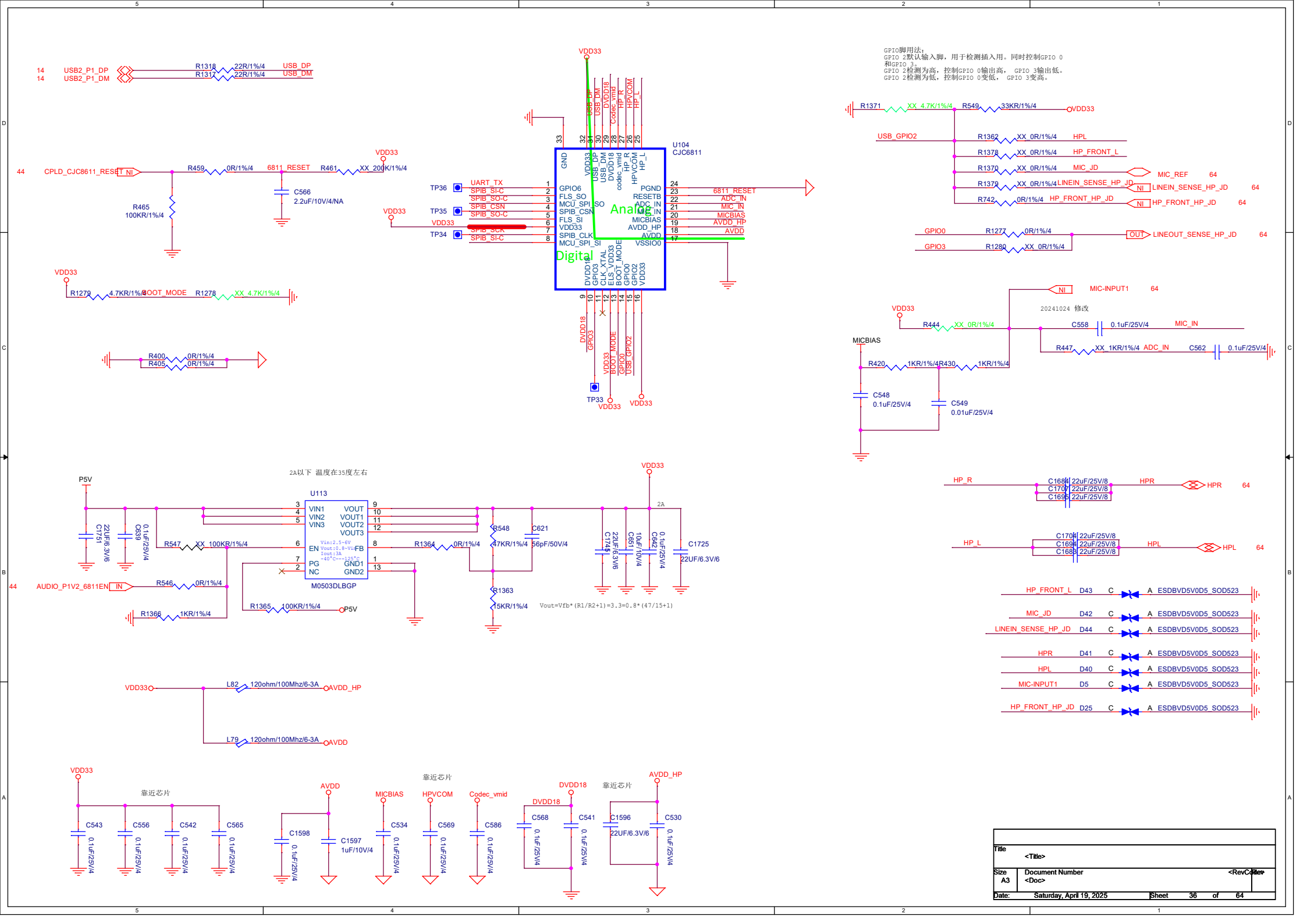



| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 35 of 64 |


GPIO脚用法:
GPIO 2默认输入脚，用于检测插入用。同时控制GPIO 0
和GPIO 3。
GPIO 2检测为高，控制GPIO 0输出高， GPIO 3输出低。
GPIO 2检测为低，控制GPIO 0变低， GPIO 3变高。
U104
CJC6811
Analog
Digital
U113
M0503DLBGP
2a以下 温度在35度左右
Vout=Vfb*(R1/R2+1)=3.3=0.8*(47/15+1)
20241024 修改
靠近芯片
Title
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Size
A3
Document Number
<Doc>
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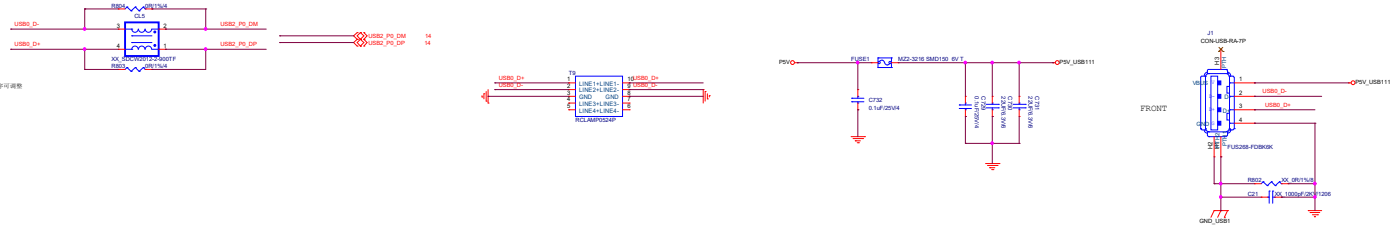
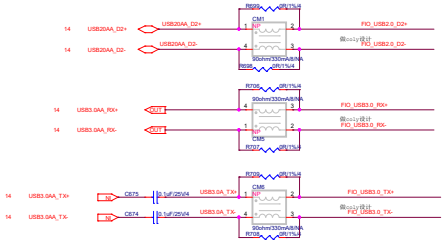
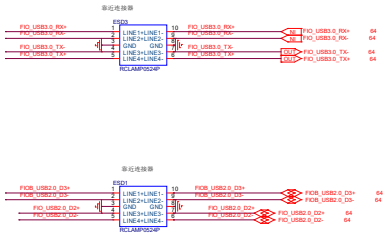
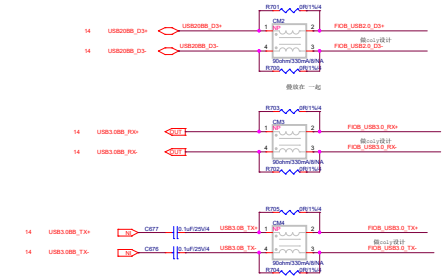
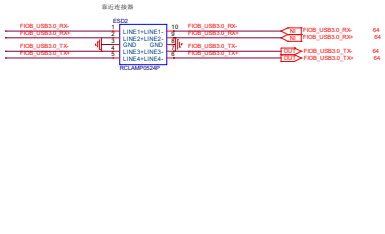


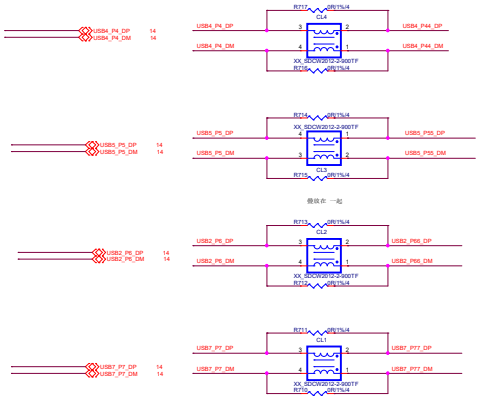

# PS2

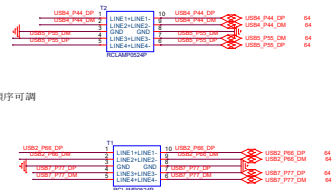
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| Title | <Title> | | |
| Size A1 | Document Number <Doc> | | Rev <RevCode> |
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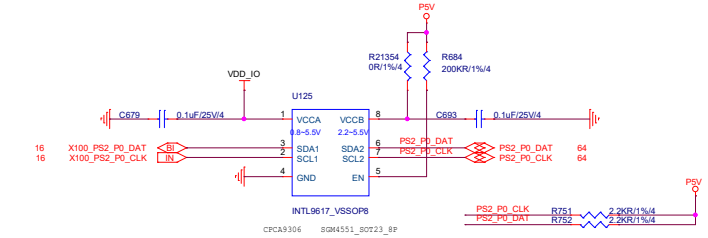


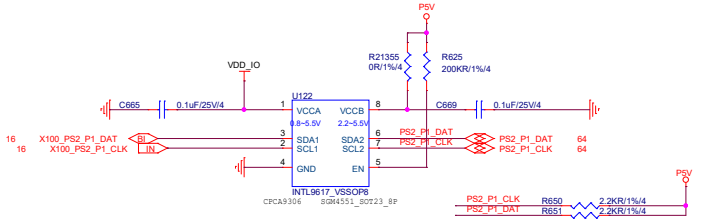


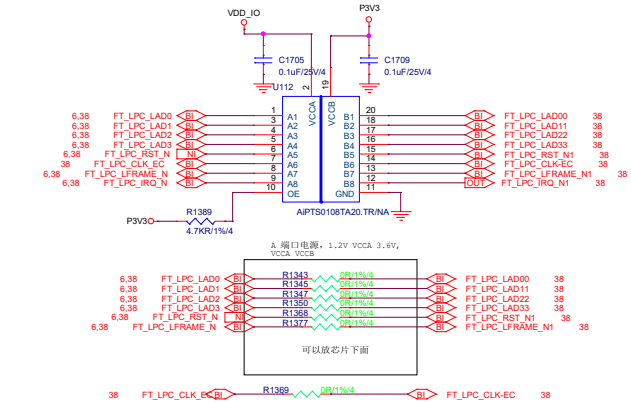


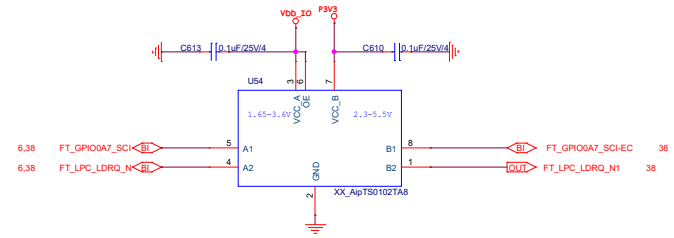


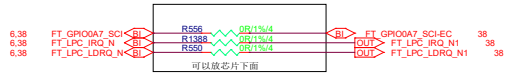


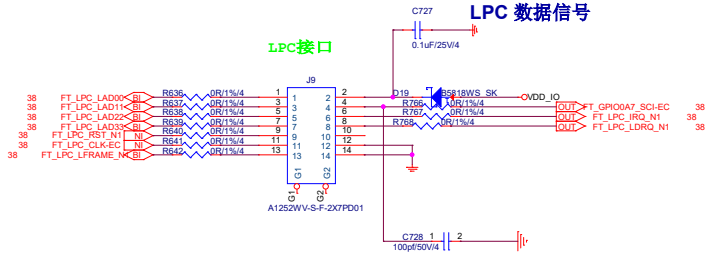


| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
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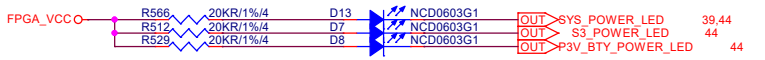
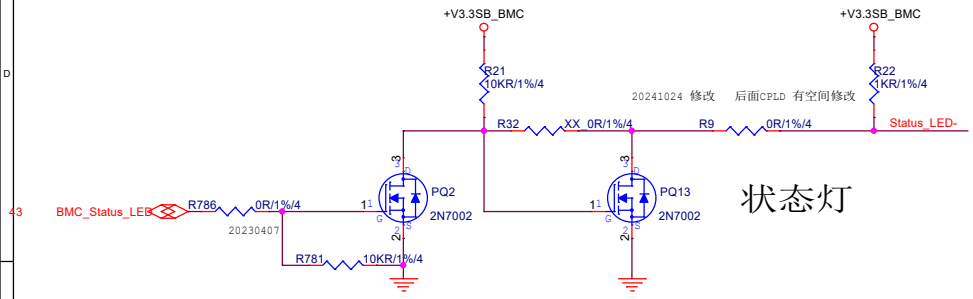
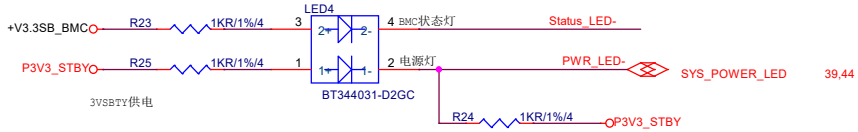
系统_LED　　S3_LED



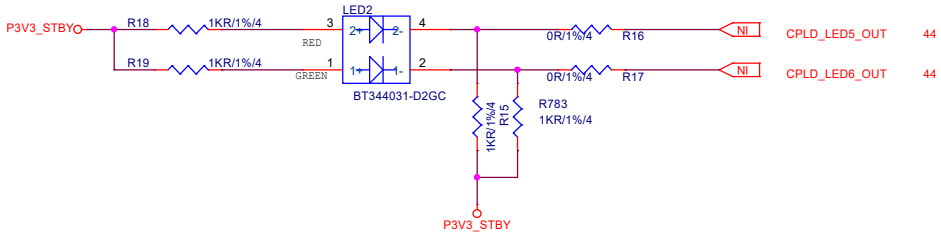

状态灯

放在指定位置

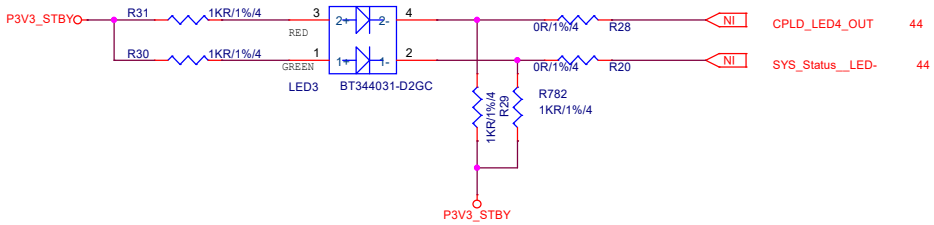


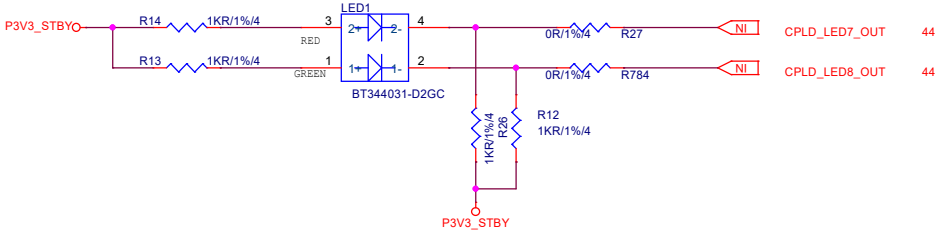

后面修改成高电平

绿灯，闪亮，指示模块工作正常，频率为2hz，占空比50%，通过CPU和CPLD都可控制灯状态。




20240102 修改　R496 下件，R501上件，R483下件，R1874新增




| | | |
|---|---|---|
| Title | <Title> | |
| Size A3 | Document Number <Doc> | <RevCode> |
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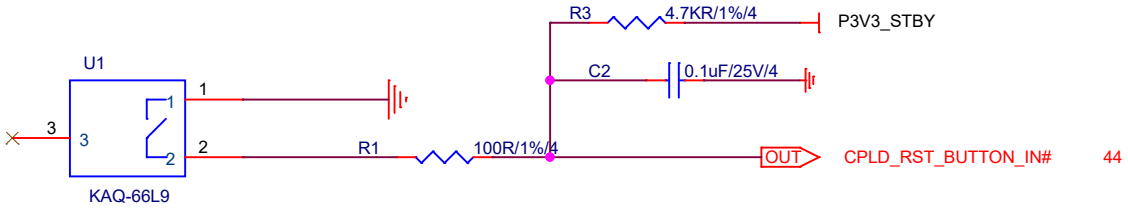
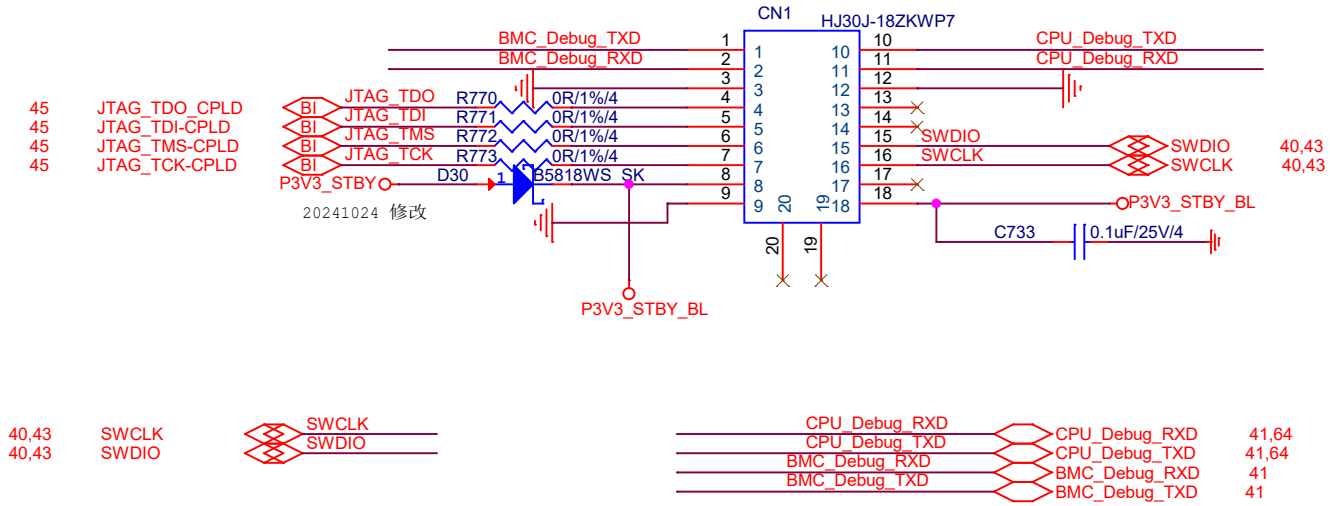



Reset butten 默认为高，低有效




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A4 | Document Number <Doc> | | <Rev Code> |
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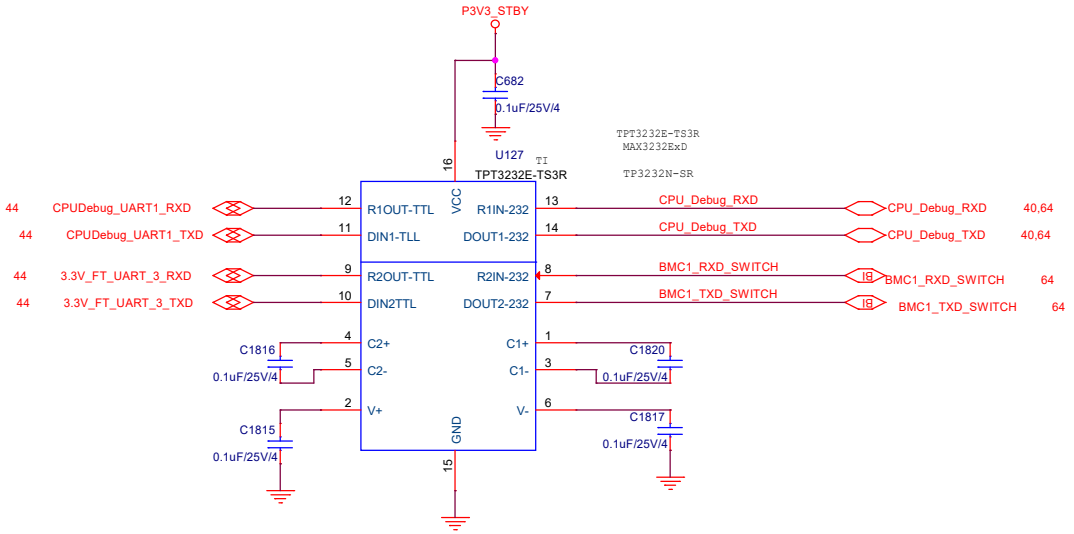
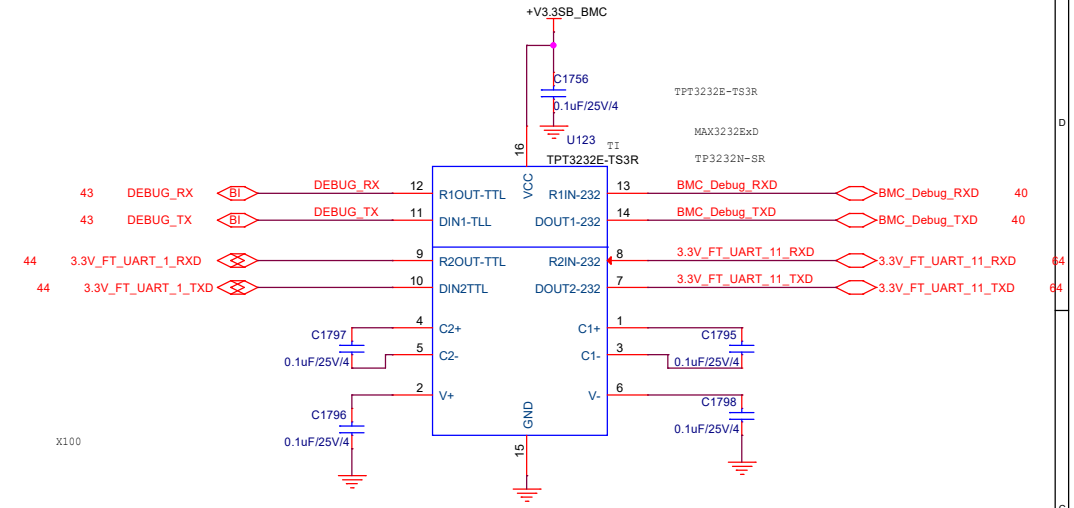
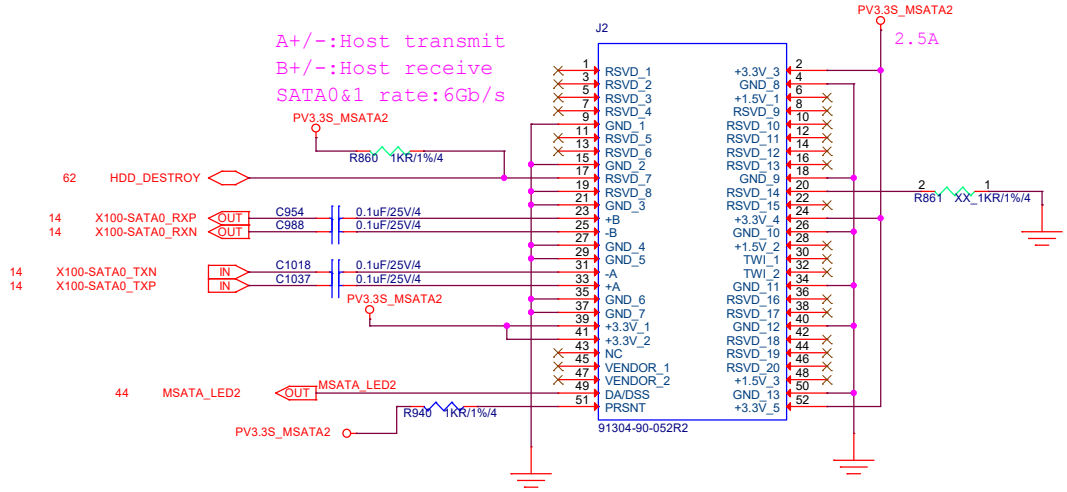
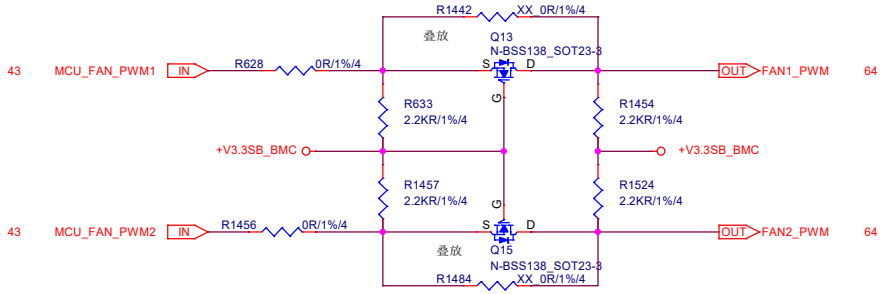
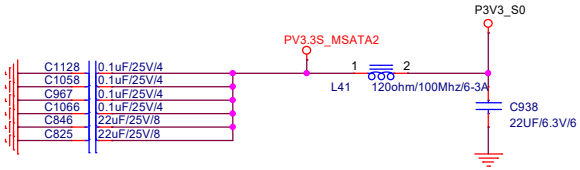


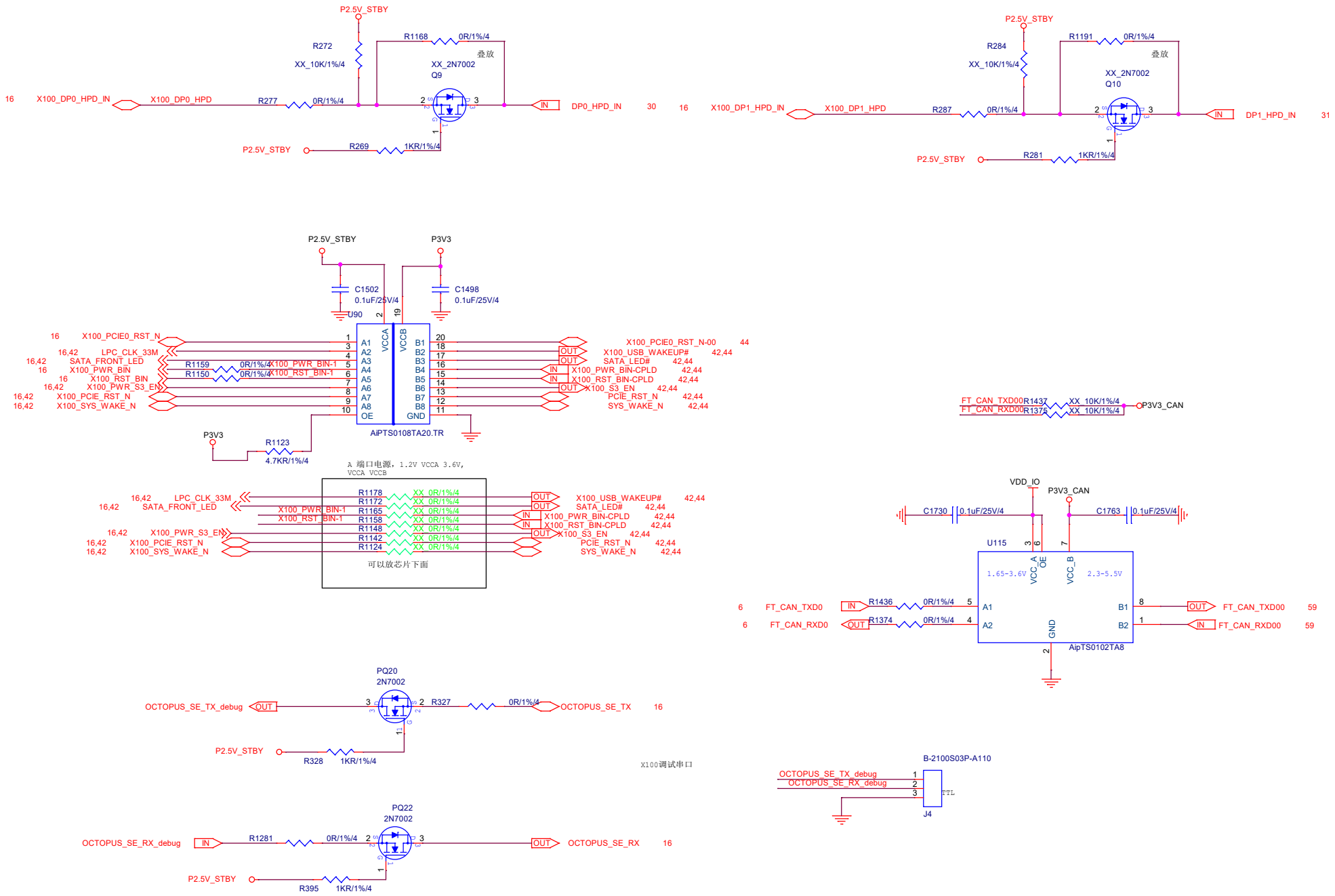




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A3 | Document Number <Doc> | | <RevCode> Rev |
| Date: Saturday, April 19, 2025 | Sheet 41 of 64 | | |




| | | |
|---|---|---|
| Title | <Title> | |
| Size A3 | Document Number <Doc> | <RevCode> |
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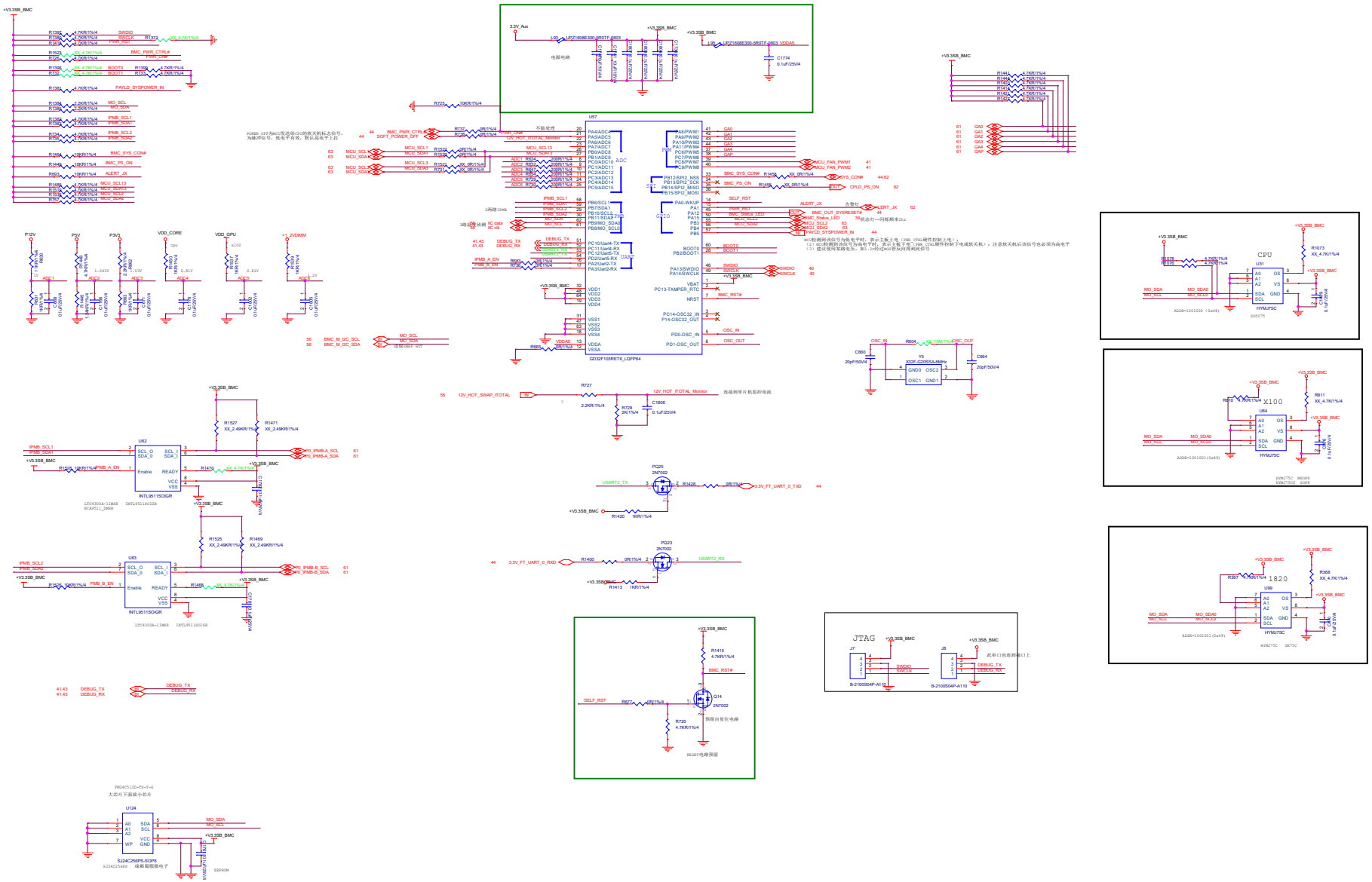
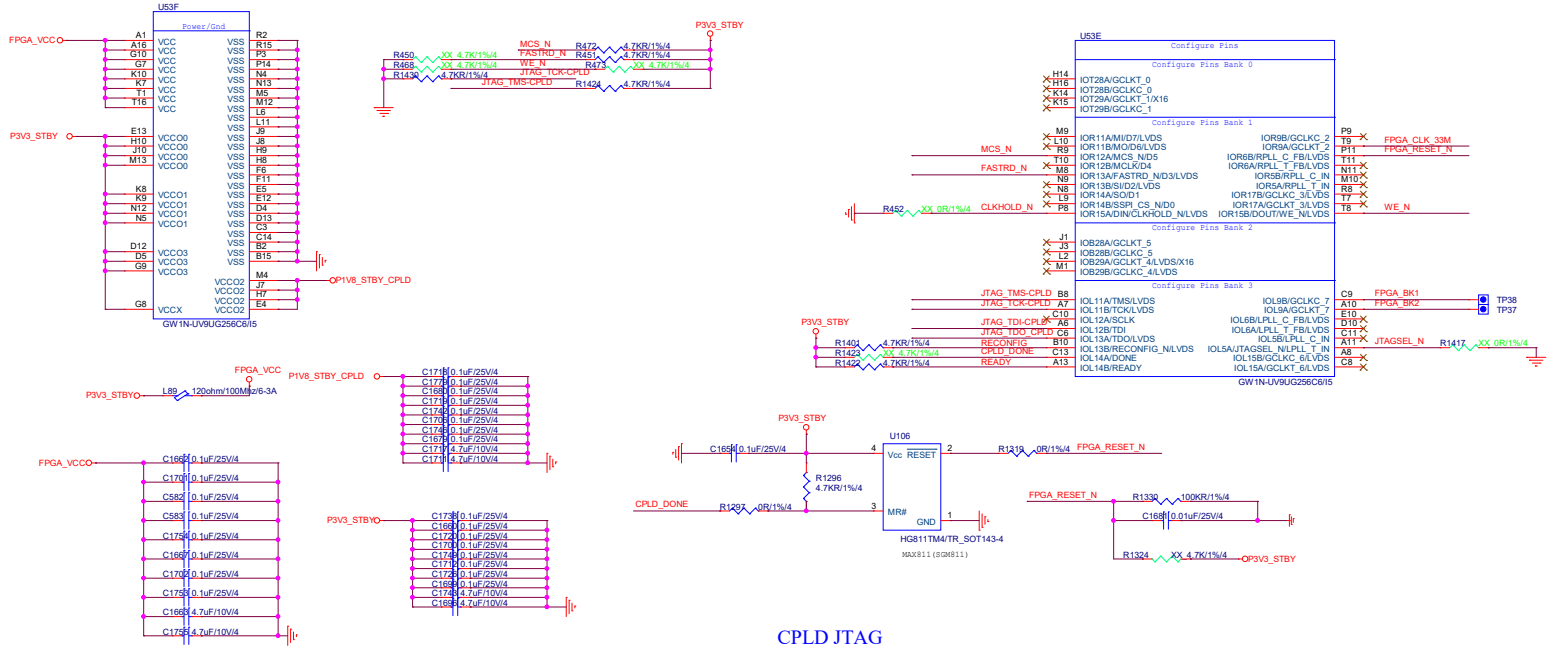



| | | | |
|---|---|---|---|
| File | <Title> | | |
| Size A1 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | | Sheet 43 of 64 | |

| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> |
| Rev | A |
| Date: Saturday, April 19, 2025 | Sheet 44 of 64 |

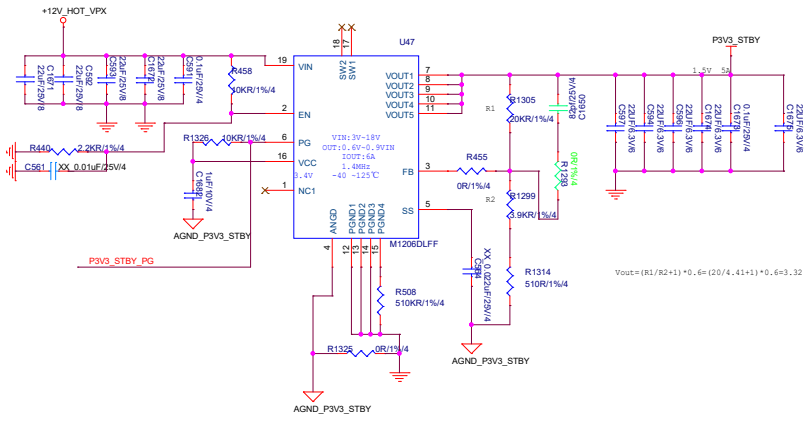


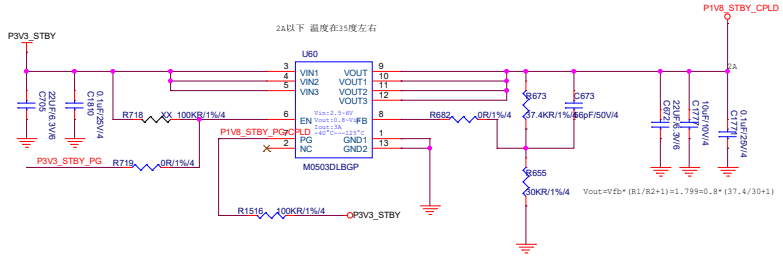

CPLD JTAG

33M CLK

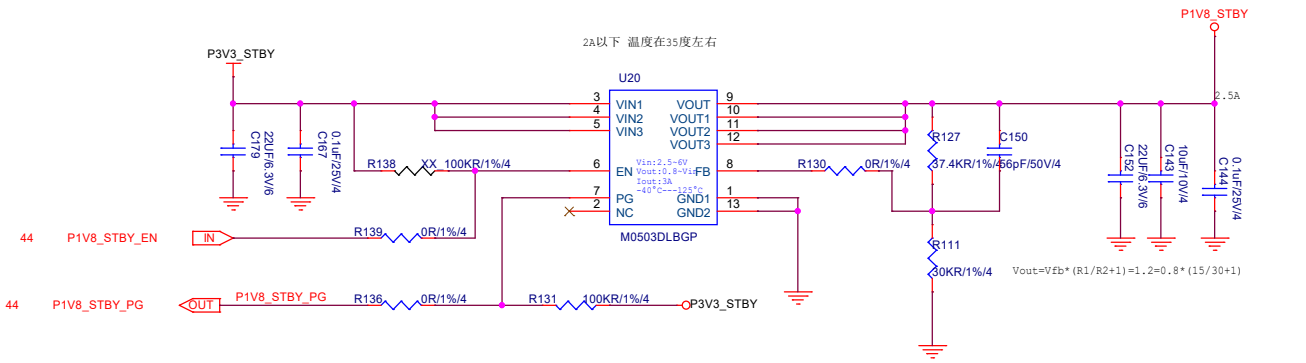
CPLD JTAG到前面板接口上

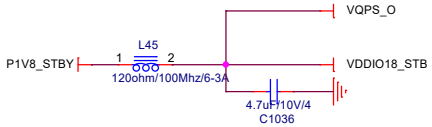
| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> |
| Rev | <RevCod |
| Date: Saturday, April 19, 2025 | Sheet 45 of 64 |

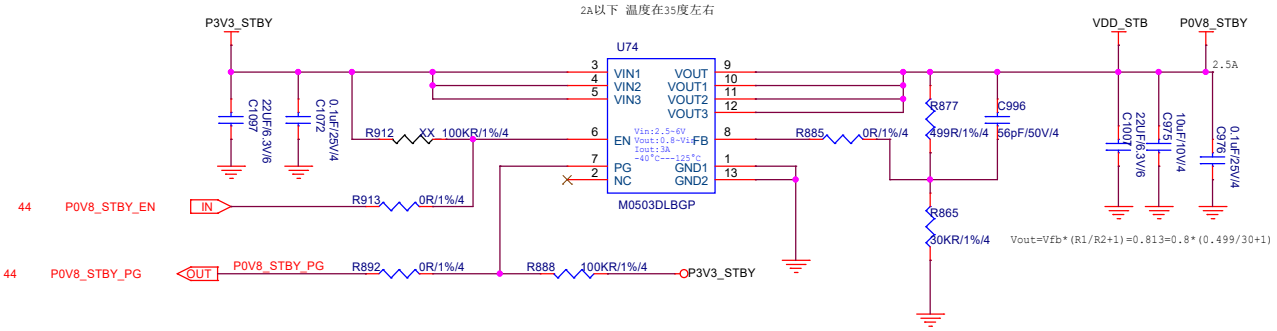


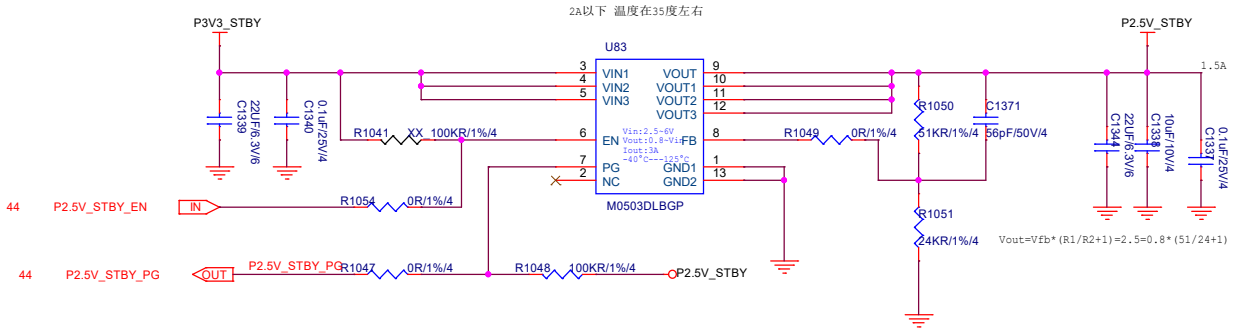




| | | |
|---|---|---|
| Title | <Title> | |
| Size A2 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 46 of 64 | |

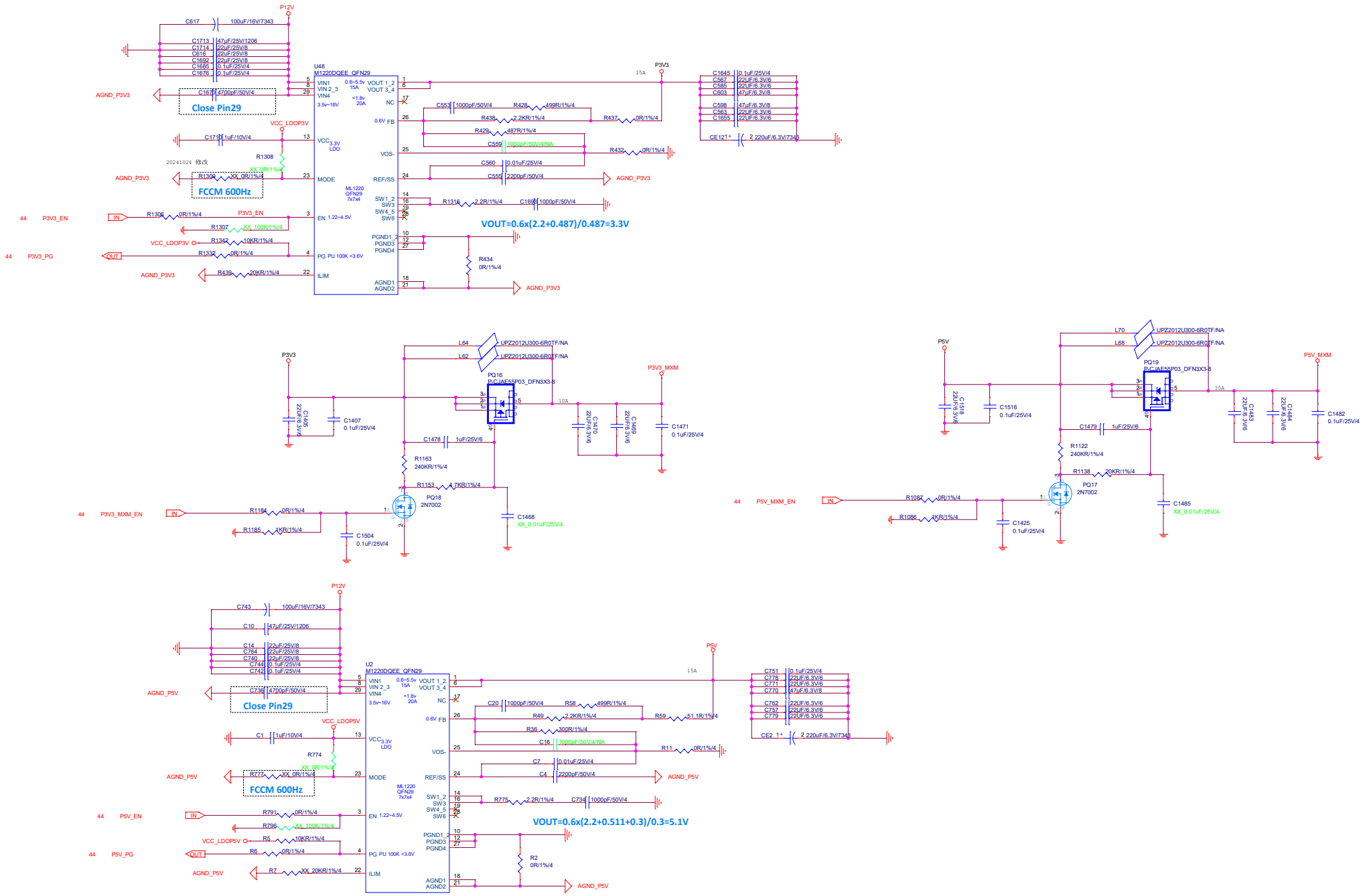



| | | |
|---|---|---|
| Title <Title> | | |
| Size A3 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 47 of 64 | |




| | | |
|---|---|---|
| Title <Title> | | |
| Size A2 | Document Number <Doc> | Rev <RevCode> |
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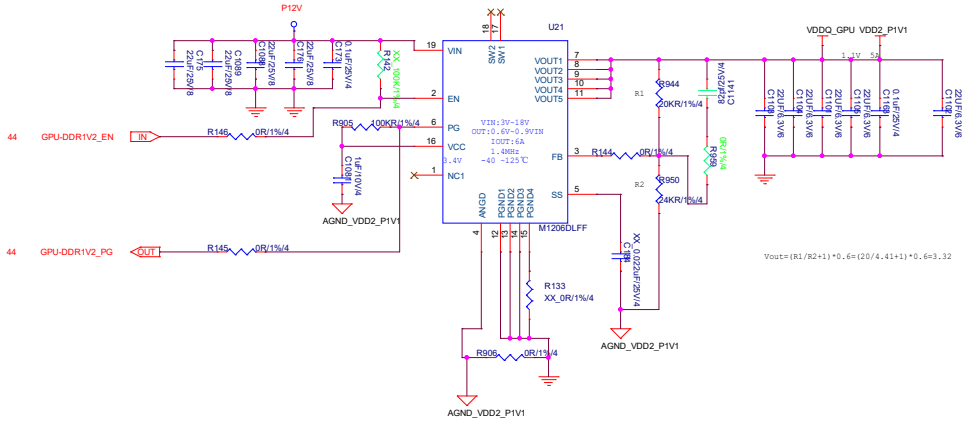


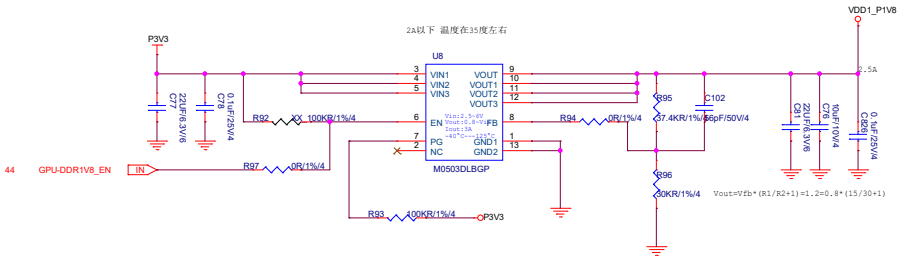


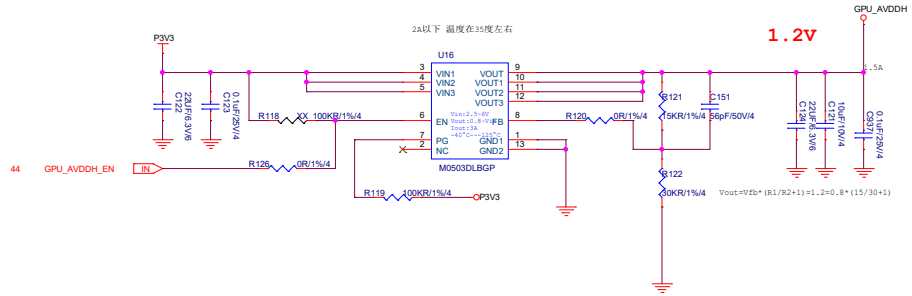


| | | |
|---|---|---|
| Title <Title> | | |
| Size A2 | Document Number <Doc> | Rev <RevCode> |
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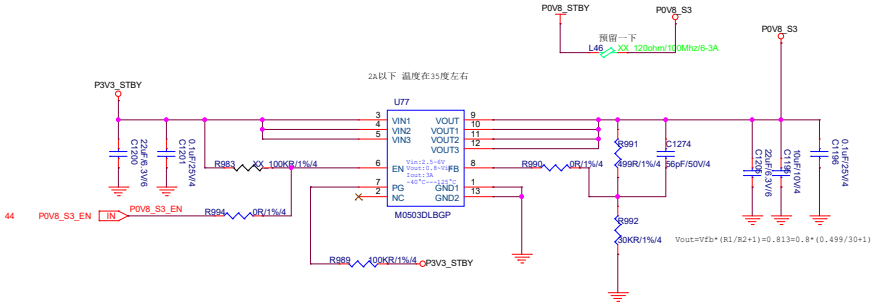
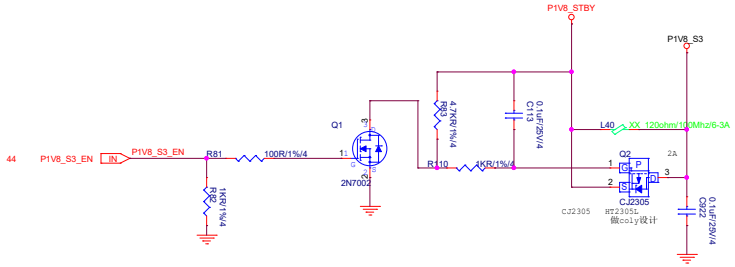
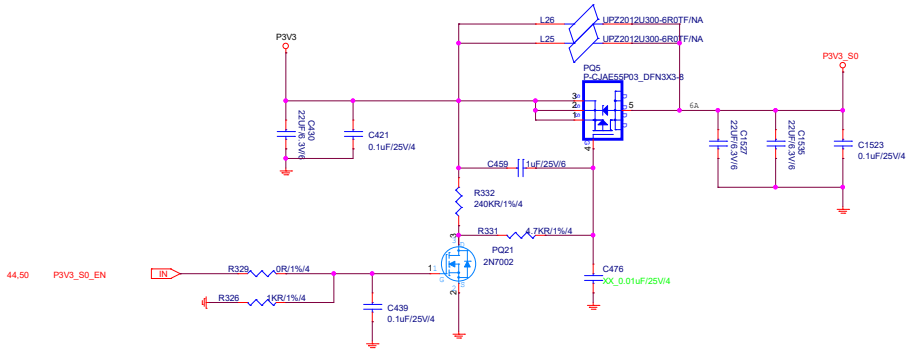
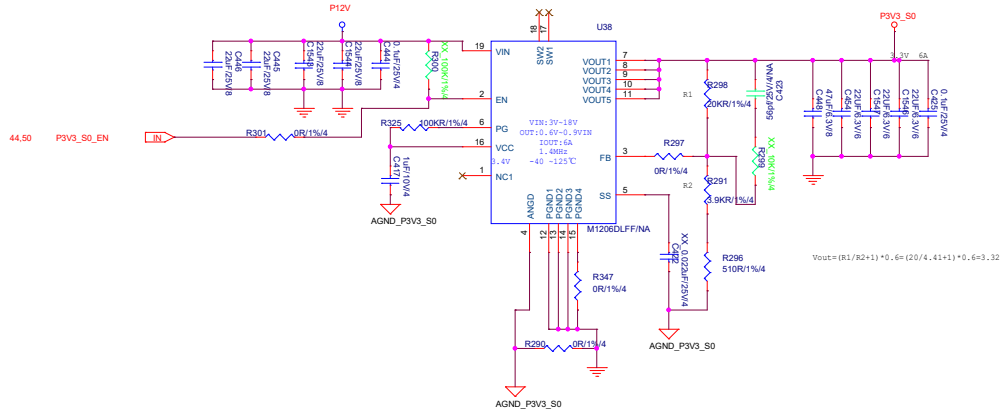
# P0V8_S3

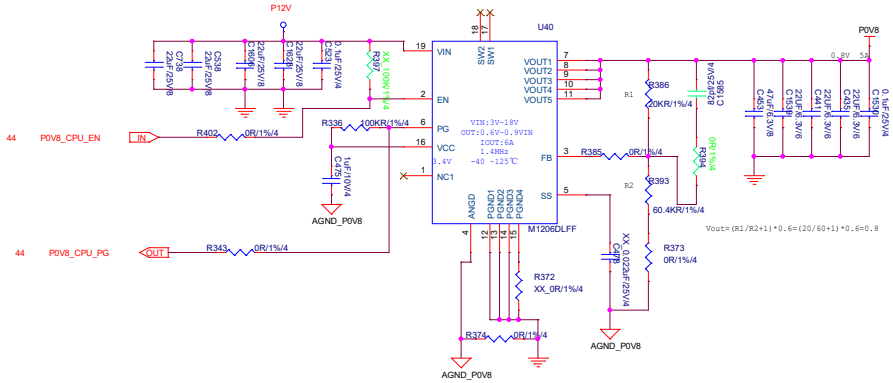


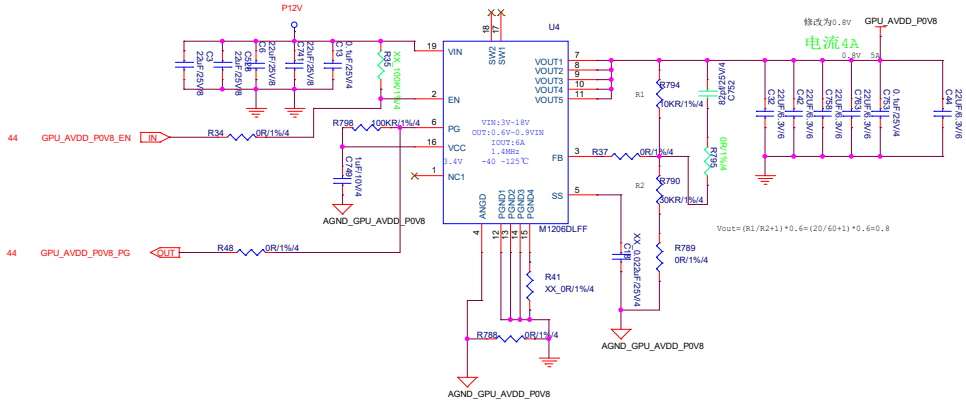



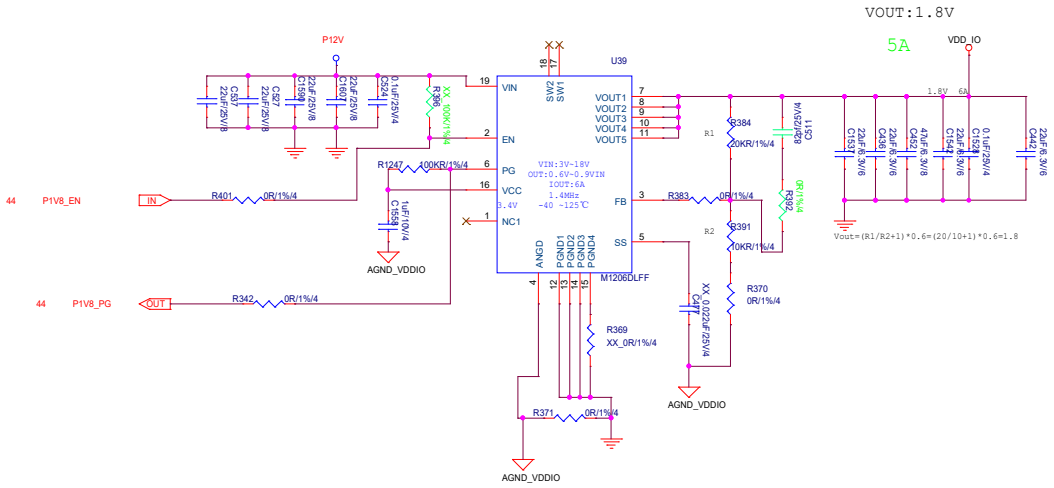




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 50 of 64 | | |

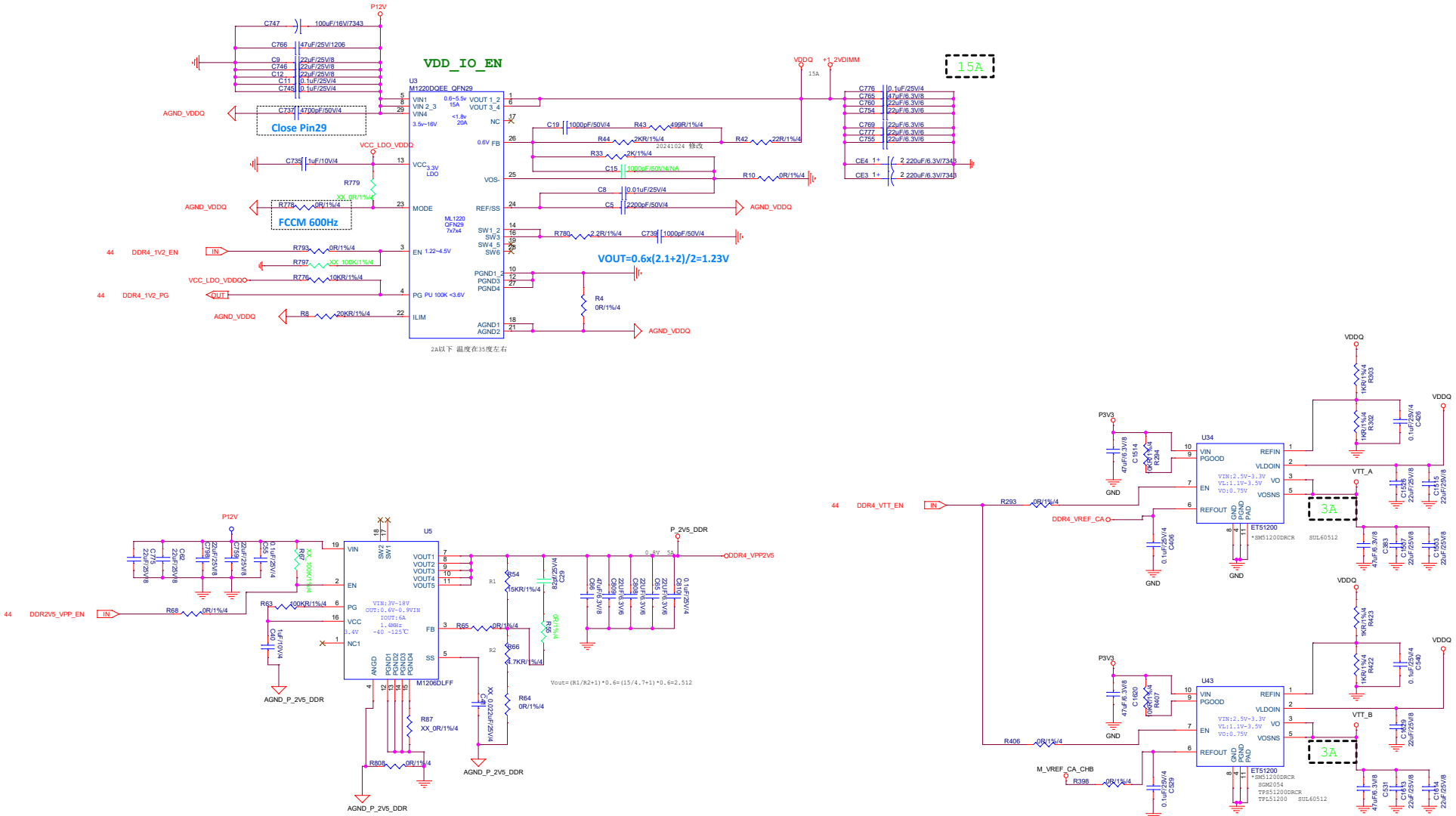


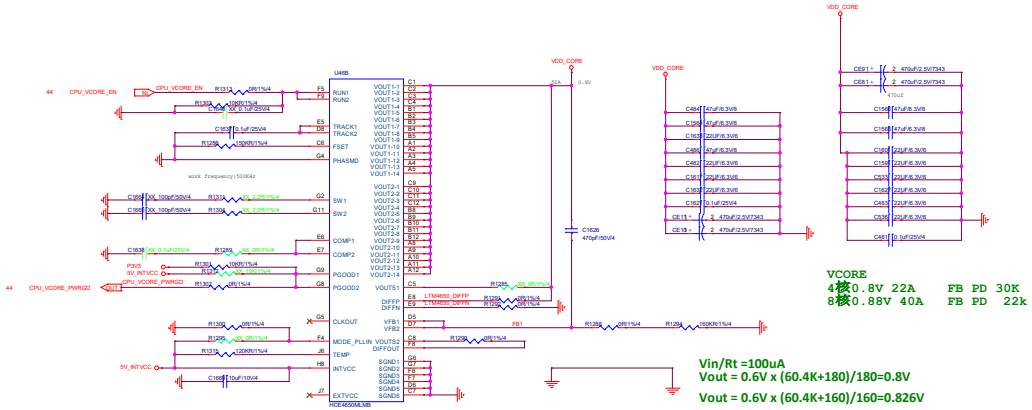

| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A2 | Document Number <Doc> | | Rev <RevCode> |
| Date: Wednesday, April 23, 2025 | Sheet 51 of 64 | | |




| | | | |
|---|---|---|---|
| Title <Title> | | | |
| Size C | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 52 of 64 | | |




| | |
|---|---|
| Title | <Title> |
| Size A2 | Document Number <Doc> |
| Rev | <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 53 of 64 |









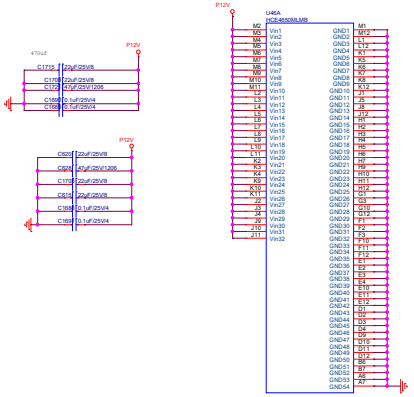




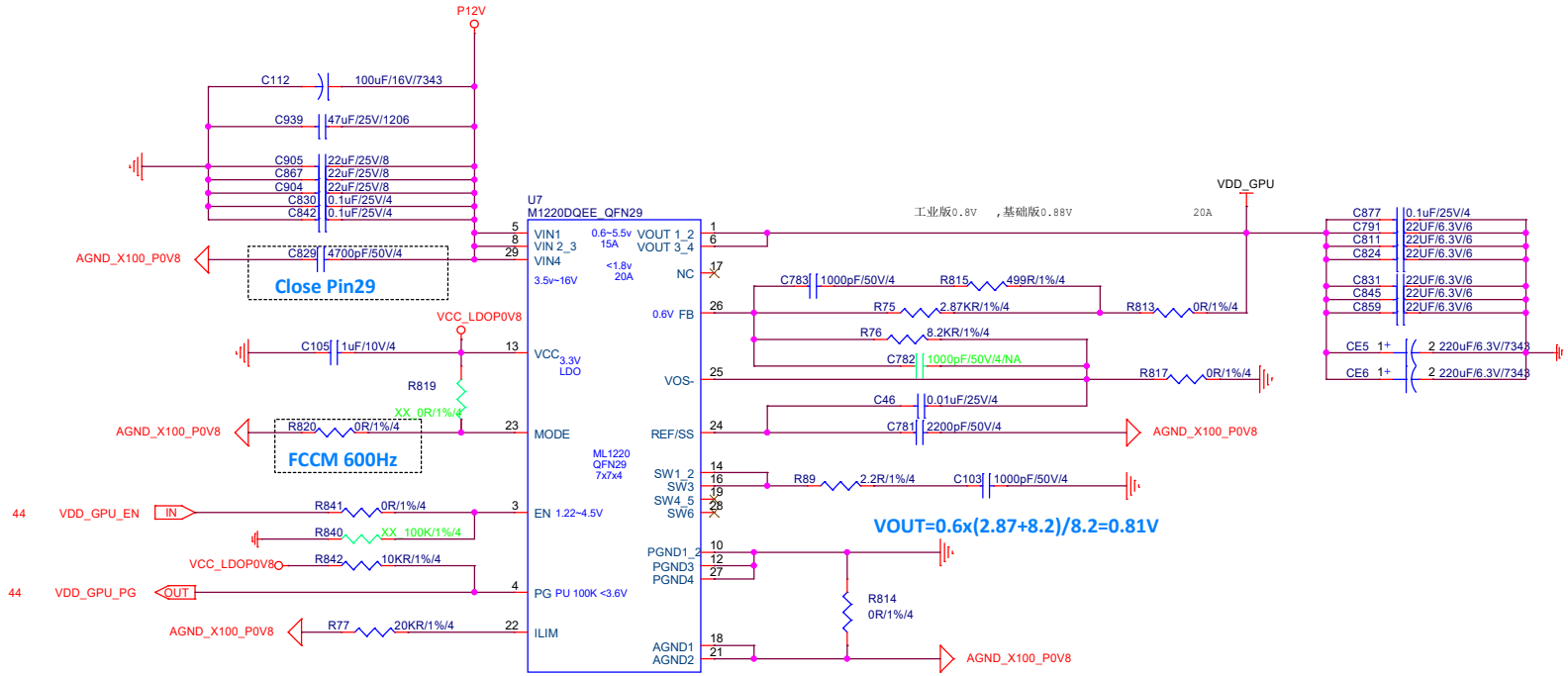
VCORE
4核0.8V 22A FB PD 30K
8核0.88V 40A FB PD 22k

Vin/Rt =100uA
Vout = 0.6V x (60.4K+180)/180=0.8V

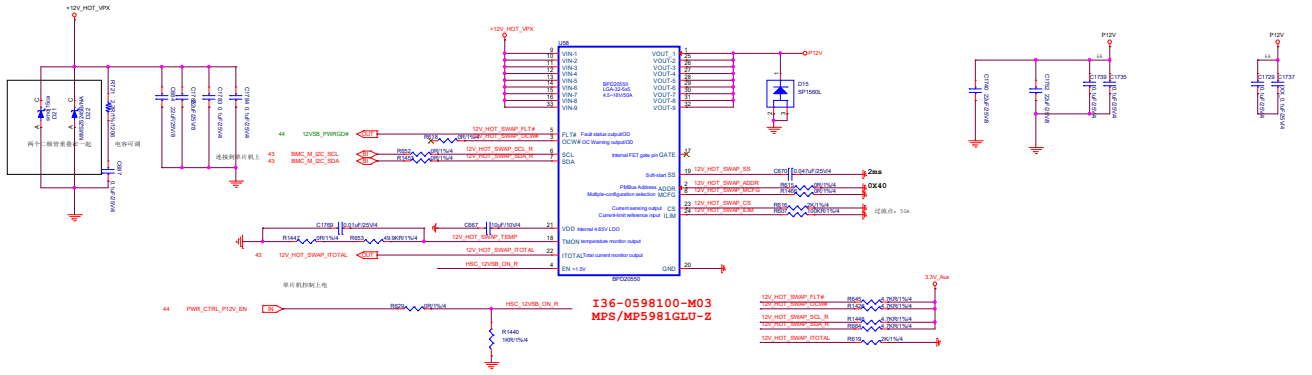
Vout = 0.6V x (60.4K+160)/160=0.826V

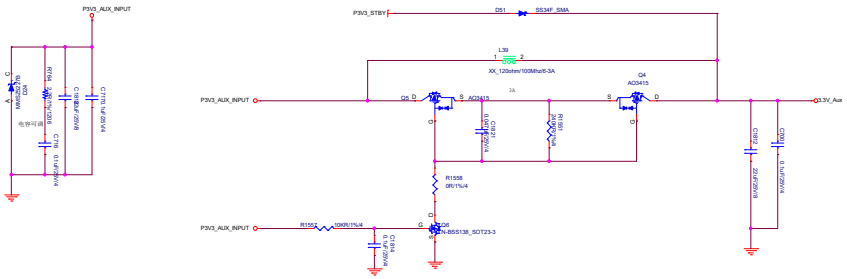



| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A1 | Document Number <Doc> | | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 54 of 54 | | |

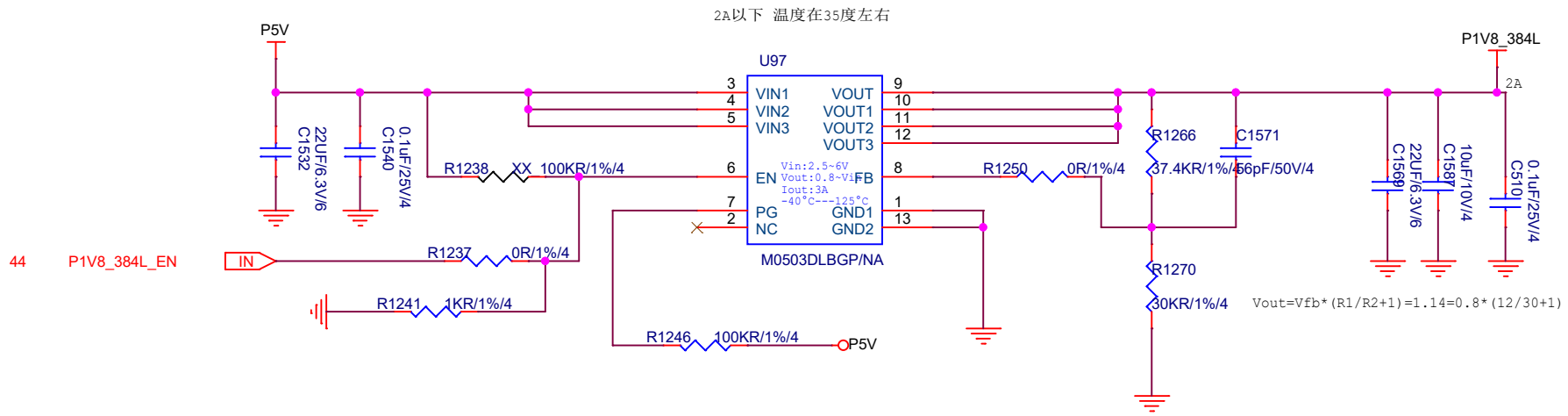



| | | |
|---|---|---|
| Title <Title> | | |
| Size A3 | Document Number <Doc> | Rev <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 55 of 64 | |




| | | | |
|---|---|---|---|
| Title: <Title> | | | |
| Size: A1 | Document Number: <Doc> | | Rev: <RevCode> |
| Date: Saturday, April 19, 2025 | Sheet 56 of 54 | | |




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A4 | Document Number <Doc> | | Rev <RevCode> |
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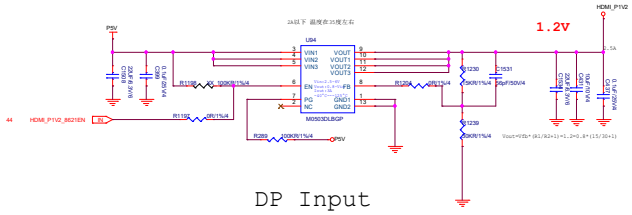
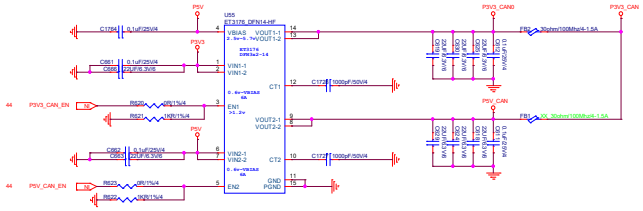



DP Input




| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A1 | Document Number <Doc> | | Rev <RevCode> |
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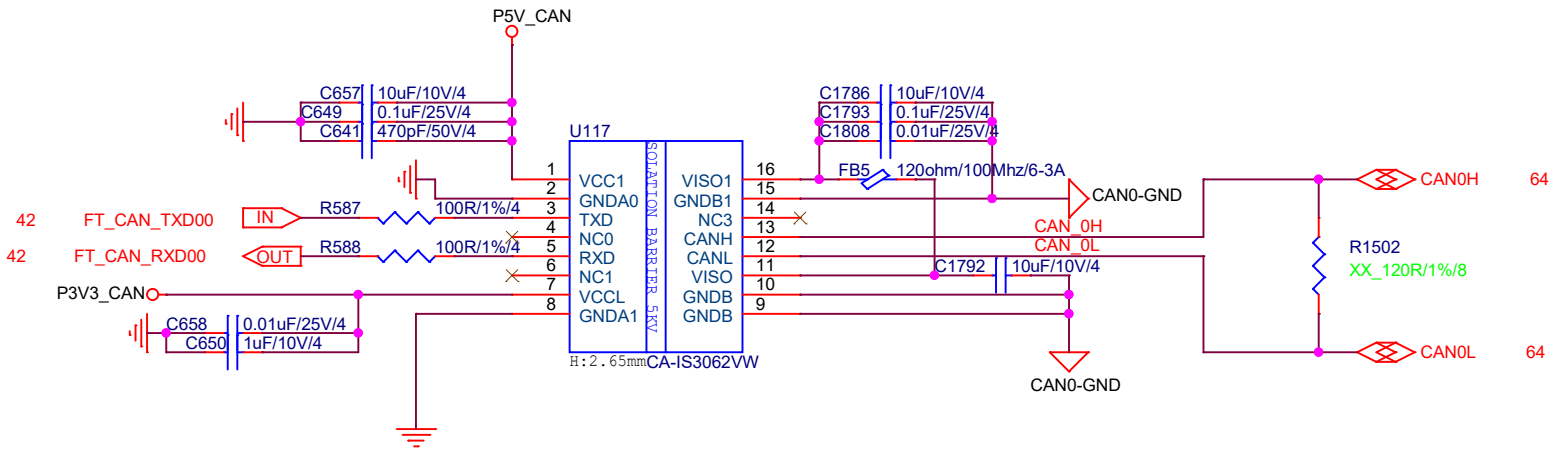


| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A4 | Document Number <Doc> | | Rev <RevCode> |
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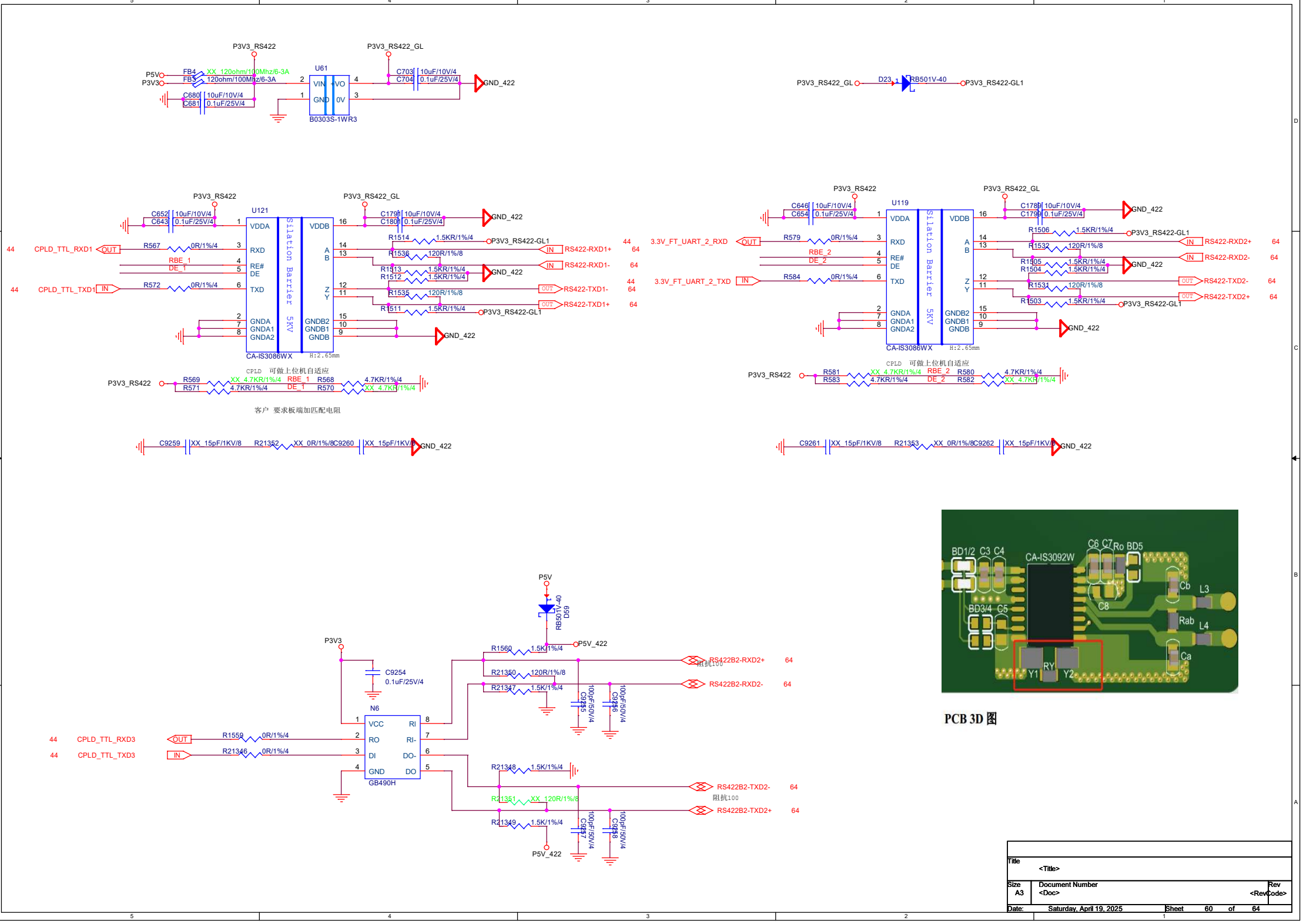
P3V3_RS422
P3V3_RS422_GL
P5V
P3V3
FB4 XX_120ohm/100Mhz/6-3A
FB5 120ohm/100Mhz/6-3A
C680 10uF/10V/4
C681 0.1uF/25V/4
U61
VIN VO
GND 0V
B0303S-1WR3
C703 10uF/10V/4
C704 0.1uF/25V/4
GND_422
P3V3_RS422_GL
D23
RB501V-40
P3V3_RS422-GL1
U121
VDDA
RXD
RE#
DE
TXD
GNDA
GNDA1
GNDA2
VDDB
A
B
Z
Y
GNDB2
GNDB1
GNDB
Silation Barrier 5KV
CA-IS3086WX
H:2.65mm
C652 10uF/10V/4
C643 0.1uF/25V/4
C1791 10uF/10V/4
C1801 0.1uF/25V/4
44 CPLD_TTL_RXD1 OUT
R567 0R/1%/4
RBE_1
DE_1
44 CPLD_TTL_TXD1 IN
R572 0R/1%/4
R1514 1.5KR/1%/4
R1536 120R/1%/8
R1513 1.5KR/1%/4
R1512 1.5KR/1%/4
R1535 120R/1%/8
R1511 1.5KR/1%/4
RS422-RXD1+ 64
RS422-RXD1- 64
44 RS422-TXD1- 64
RS422-TXD1+ 64
CPLD 可做上位机自适应
P3V3_RS422
R569 XX_4.7KR/1%/4
R571 4.7KR/1%/4
RBE_1
DE_1
R568 4.7KR/1%/4
R570 XX_4.7KR/1%/4
客户 要求板端加匹配电阻
C9259 XX_15pF/1KV/8
R21352 XX_0R/1%/8
C9260 XX_15pF/1KV/8
U119
3.3V_FT_UART_2_RXD
R579 0R/1%/4
RBE_2
DE_2
3.3V_FT_UART_2_TXD
R584 0R/1%/4
C646 10uF/10V/4
C654 0.1uF/25V/4
C1789 10uF/10V/4
C1799 0.1uF/25V/4
R1506 1.5KR/1%/4
R1532 120R/1%/8
R1505 1.5KR/1%/4
R1504 1.5KR/1%/4
R1531 120R/1%/8
R1503 1.5KR/1%/4
44 RS422-RXD2+ 64
RS422-RXD2- 64
RS422-TXD2- 64
RS422-TXD2+ 64
R581 XX_4.7KR/1%/4
R583 4.7KR/1%/4
R580 4.7KR/1%/4
R582 XX_4.7KR/1%/4
C9261 XX_15pF/1KV/8
R21353 XX_0R/1%/8
C9262 XX_15pF/1KV/8
P5V
RB501V-40
D59
P5V_422
P3V3
C9254 0.1uF/25V/4
N6
VCC RI
RO RI-
DI DO-
GND DO
GB490H
44 CPLD_TTL_RXD3 OUT
44 CPLD_TTL_TXD3 IN
R1559 0R/1%/4
R21346 0R/1%/4
R1560 1.5K/1%/4
R21350 120R/1%/8
R21347 1.5K/1%/4
R21348 1.5K/1%/4
R21351 XX_120R/1%/8
R21349 1.5K/1%/4
C9255 100pF/50V/4
C9256 100pF/50V/4
C9257 100pF/50V/4
C9258 100pF/50V/4
RS422B2-RXD2+ 64
阻抗100
RS422B2-RXD2- 64
RS422B2-TXD2- 64
阻抗100
RS422B2-TXD2+ 64
BD1/2 C3 C4
CA-IS3092W
C6 C7 Ro BD5
BD3/4 C5
C8
Cb L3
Rab L4
Ca
RY
Y1 Y2
PCB 3D 图
Title
<Title>
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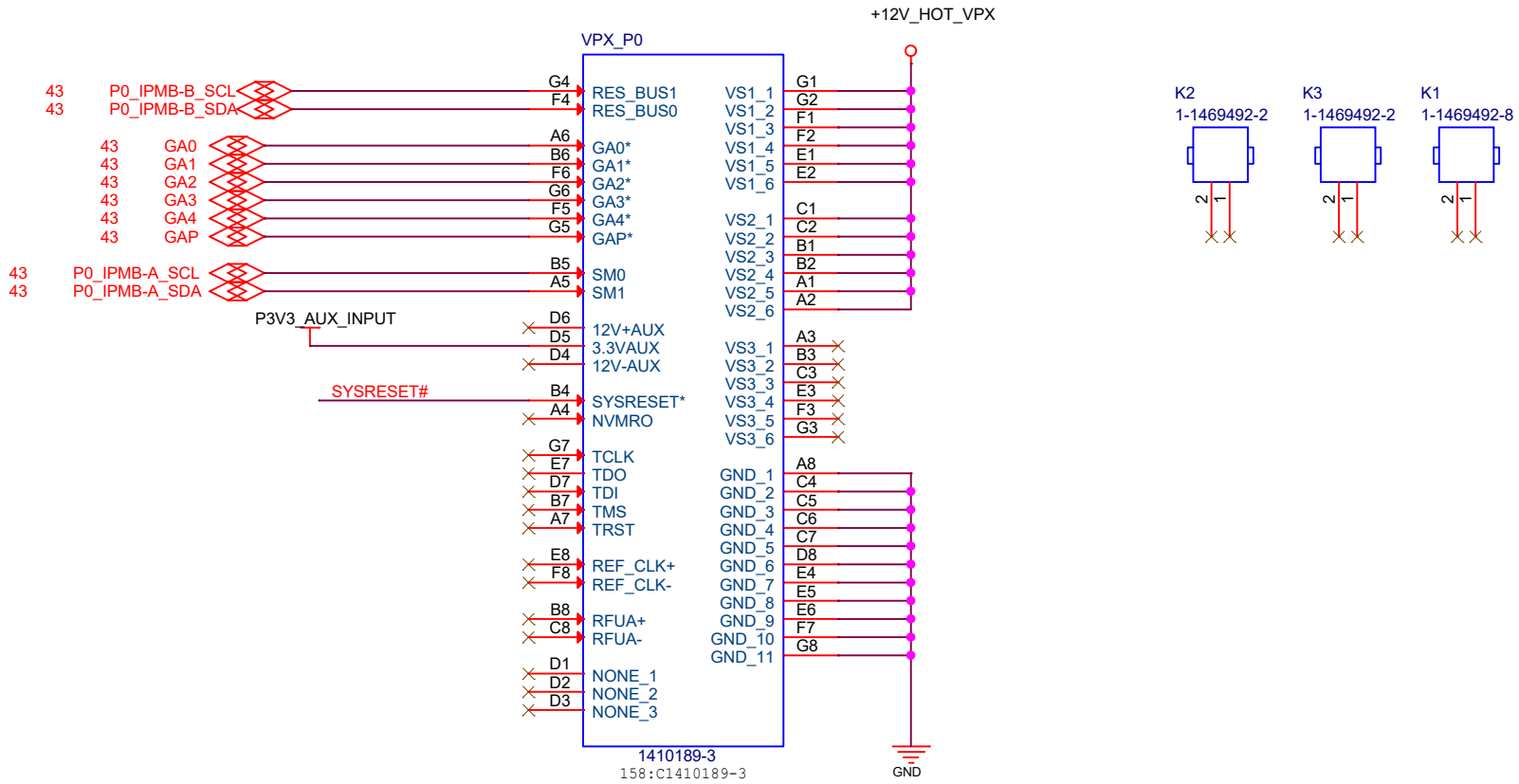


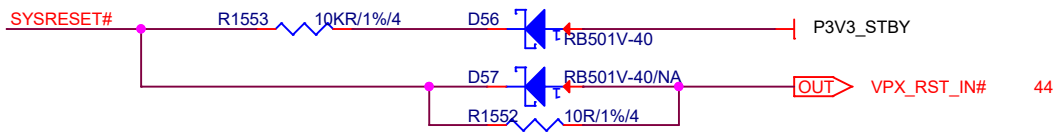


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|---|---|---|---|
| Title <Title> | | | |
| Size A4 | Document Number <Doc> | | Rev <RevCode> |
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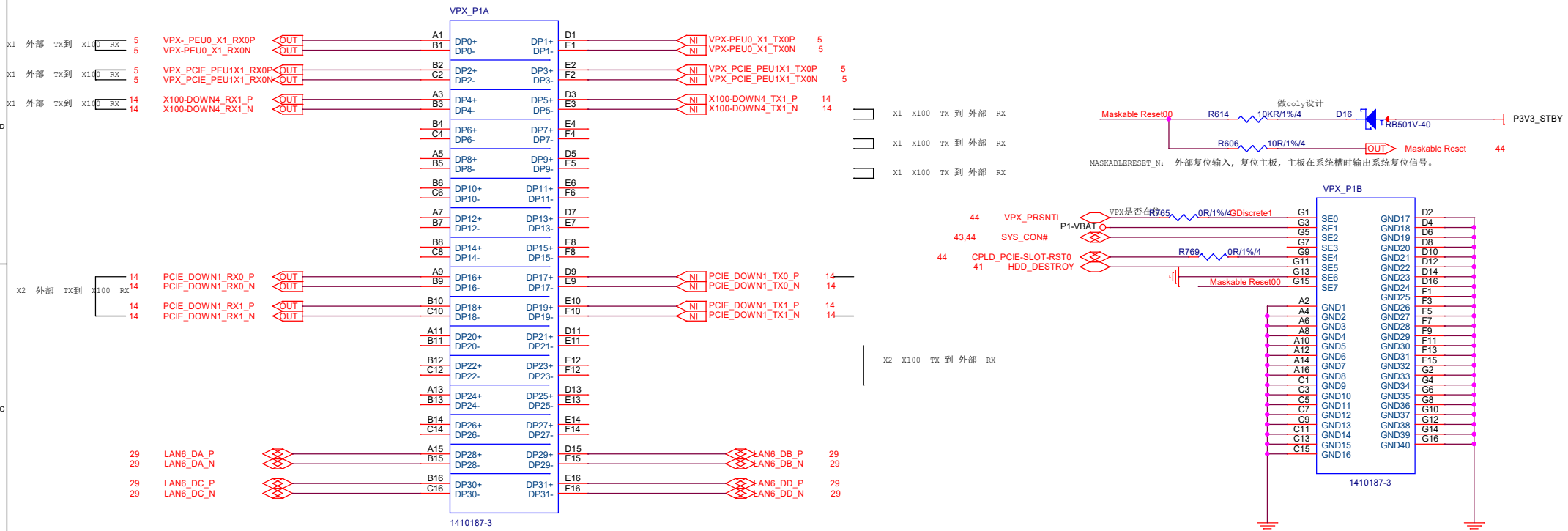


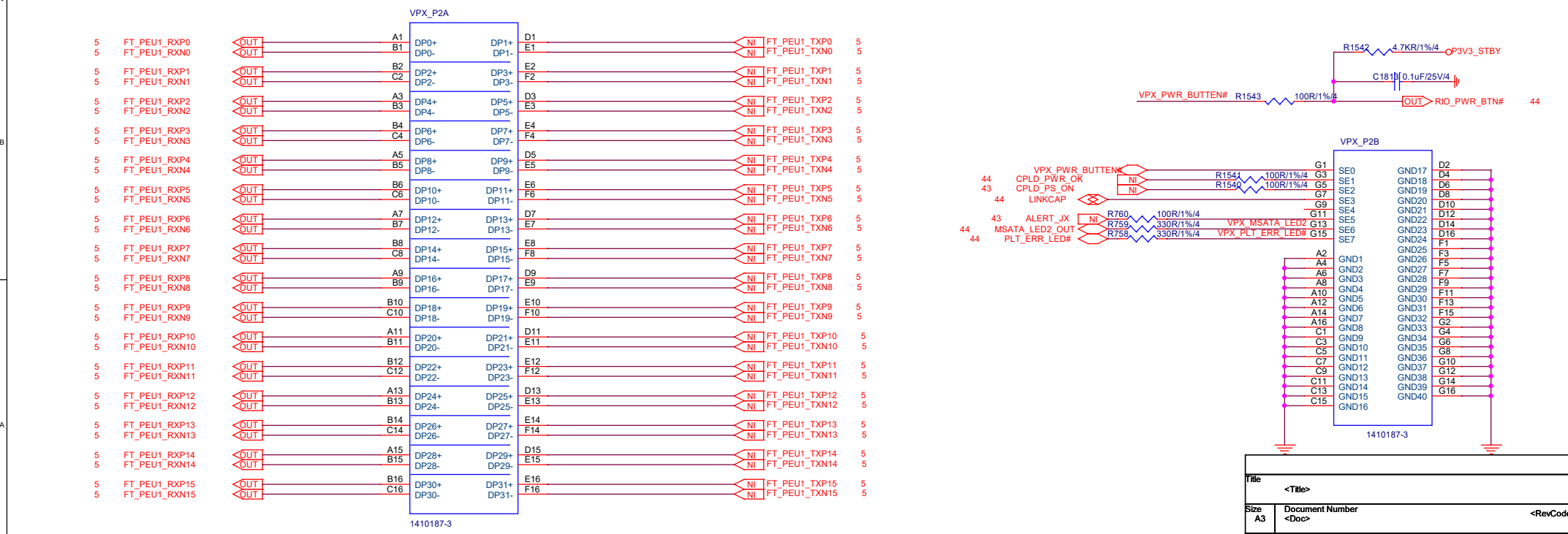


| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A3 | Document Number <Doc> | | <RevCode> Rev |
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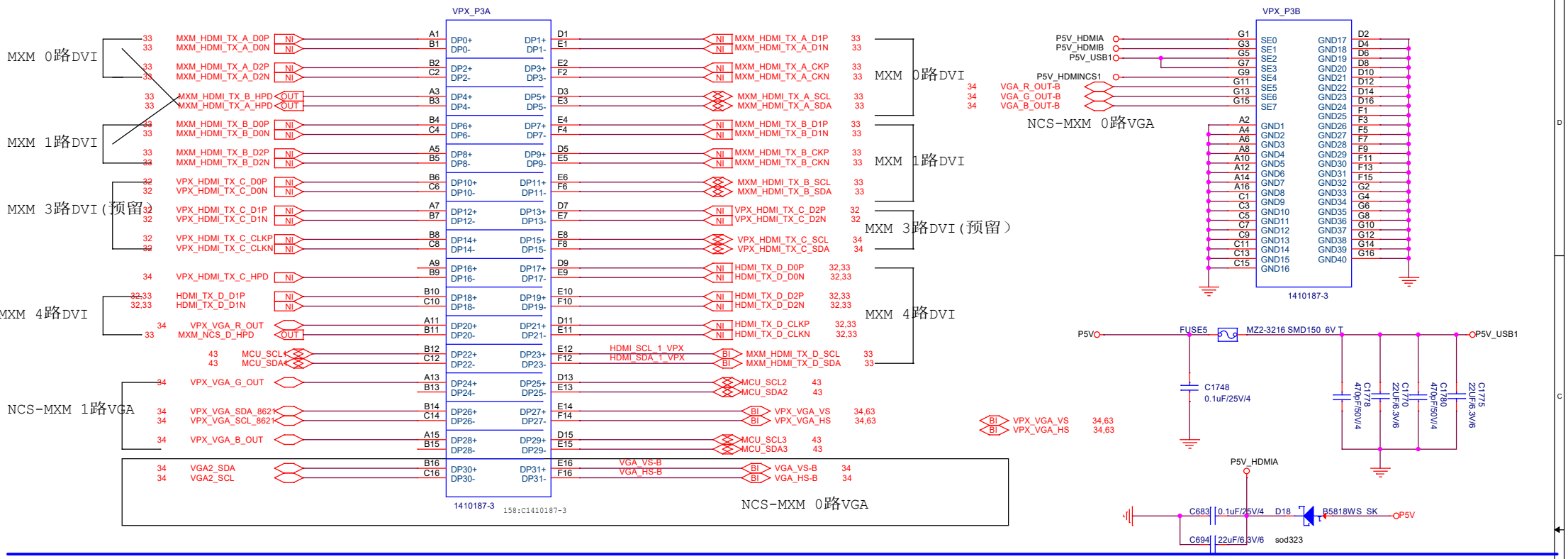


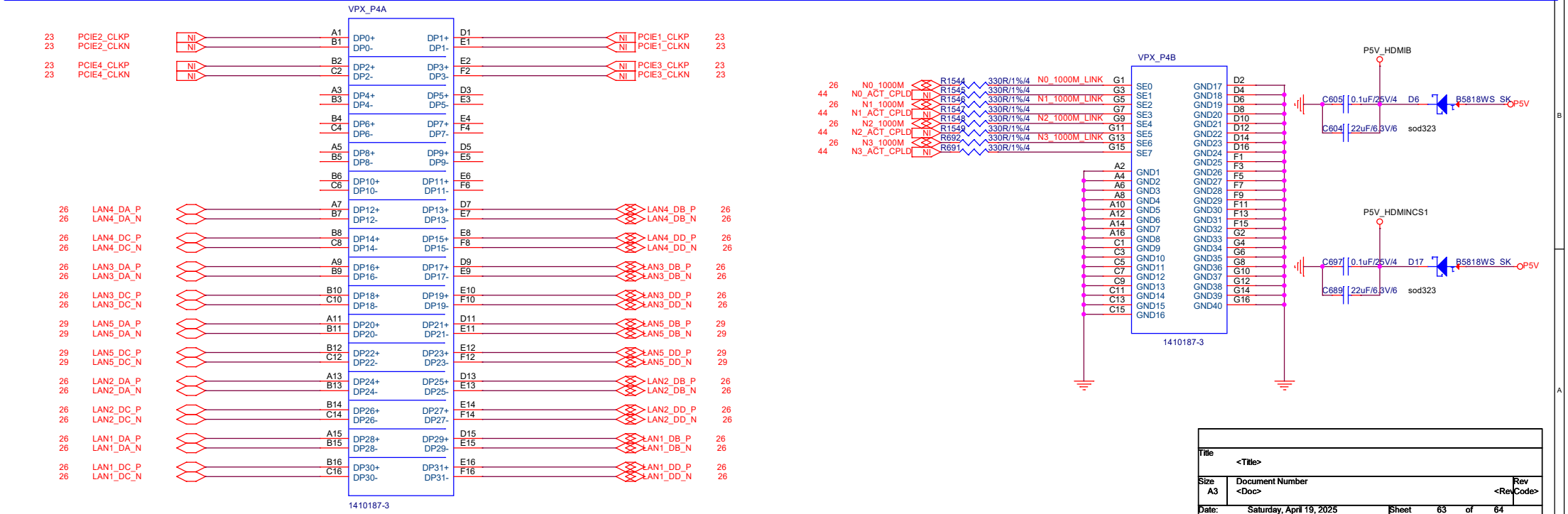


| | | | |
|---|---|---|---|
| Title | <Title> | | |
| Size A3 | Document Number <Doc> | | Rev <RevCode> |
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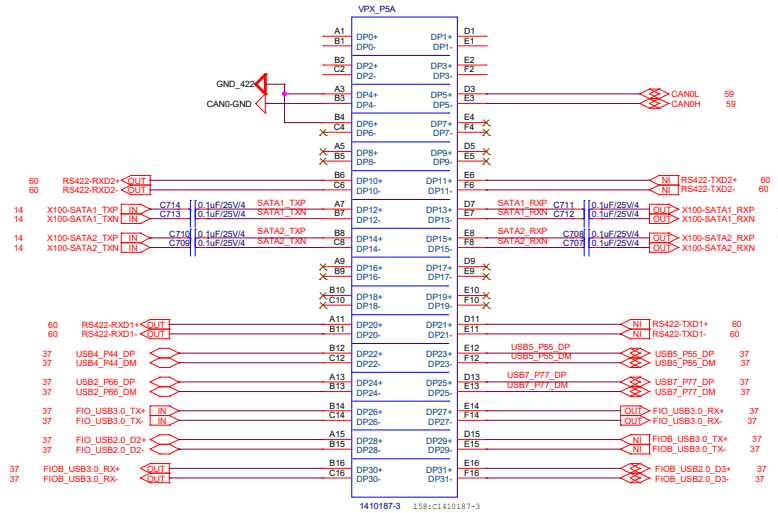


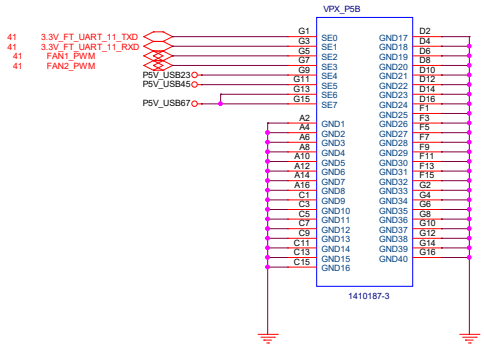


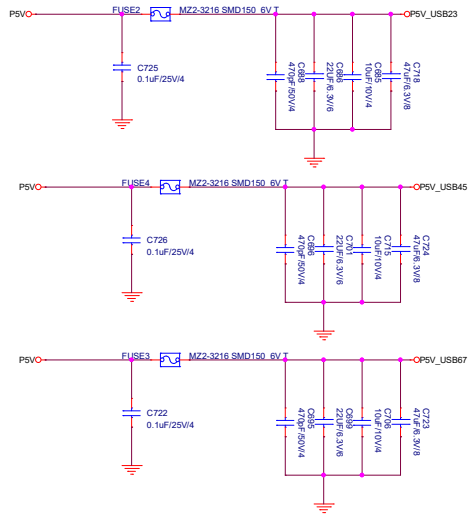


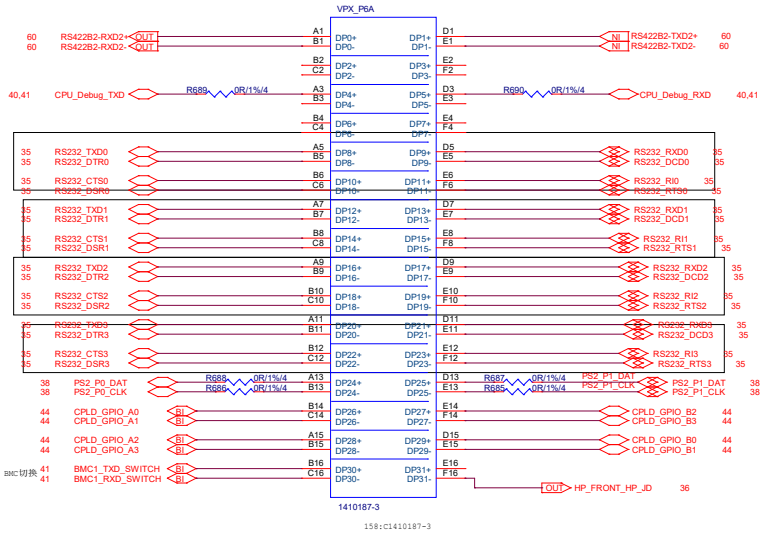


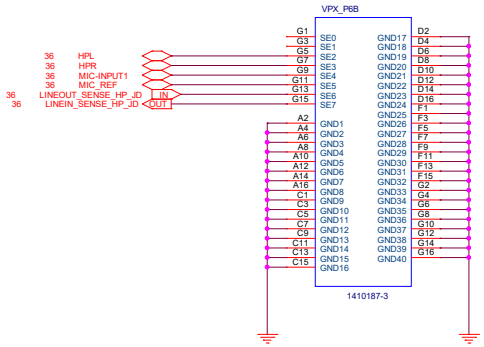

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| Title | <Title> | | |
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