```
1   // divided_clocks[0] = 25MHz, [1] = 12.5Mhz, ... [23] = 3Hz, [24] = 1.5Hz,
2   // [25] = 0.75Hz
3   module clock_divider (clock, reset, divided_clocks);
4       input logic reset, clock;
5       output logic [31:0] divided_clocks = 0;
6
7       always_ff @(posedge clock) begin
8           divided_clocks <= divided_clocks + 1;
9       end
10  endmodule
11
```