

EE/CSE 371 Project Proposal

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EE/CSE 371

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Lab Proposal

Proposal

Project behavior: using a VGA controller and ROM (that will be used as our counter), we will create a stopwatch that can start and pause when the user presses a switch. This stopwatch will display each second on the VGA terminal as an analog clock and will also utilize the HEXs from the FPGA board to display the same time in digital display.

Features: we will be using ROM as our memory storage for each x and y coordinate for the arm of the clock and a counter that goes through the logic for each second that needs to be displayed. We have decided on the color of our analog stopwatch and were thinking of making the outline red and the clock arm to be blue.

Modules:

- 2 ROM modules
 - ROM1: holds x coordinates
 - ROM2: holds y coordinates
 - Clock_arm will call on these two ROMs the output of which will go into the line_drawer module
- Counter: A counter module will be created that works on a slower clock to count each second.
- Clock_outline: draws the outline of the analog clock onto a VGA monitor along with the outlines for every five seconds (just like a clock) by calling on the circle_drawer module and line_drawer module.
- Line_drawer: line algorithm taken from lab 5, that makes a line on the VGA terminal based on the coordinates provided to it.
- Circle_drawer: circle algorithm taken from lab 5, that makes a circle on the VGA terminal based on the start point and the radius.
- Clock_arm: uses line_drawer as well as outputs from ROMs to create the 'arm' of the analog stopwatch that moves every second based on the counter.
- Seven_seg: used from previous labs for HEX display of the stopwatch.
HEX1-HEX0 will display the seconds while HEX2 will display the minutes for the stopwatch.

- Clock_divider: used from previous labs, will be the clock for 'counter' module
- video_driver: modules that were given to us for the VGA controller.

User interaction: the user will be able to start and pause the stopwatches, there will be a reset key (KEY[3]) to reset the stopwatch. SW[9] will be used by the user to stop the stopwatch at any point of time.

Top-level block diagram

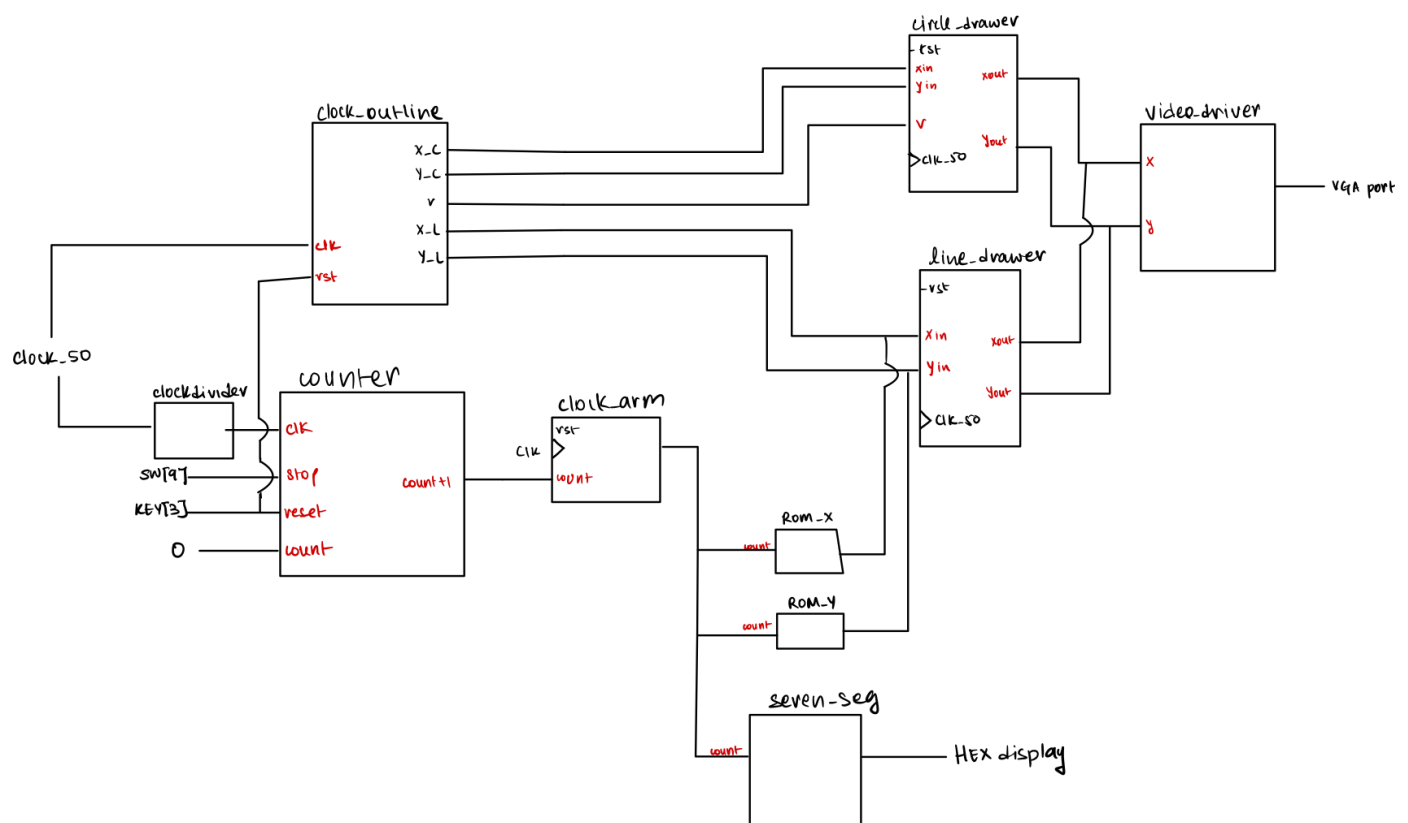


Figure 1: Rough block diagram of the top-level module

Sketch

Sketch of our lab 6 that uses the VGA controller and DE1_SoC HEX display.

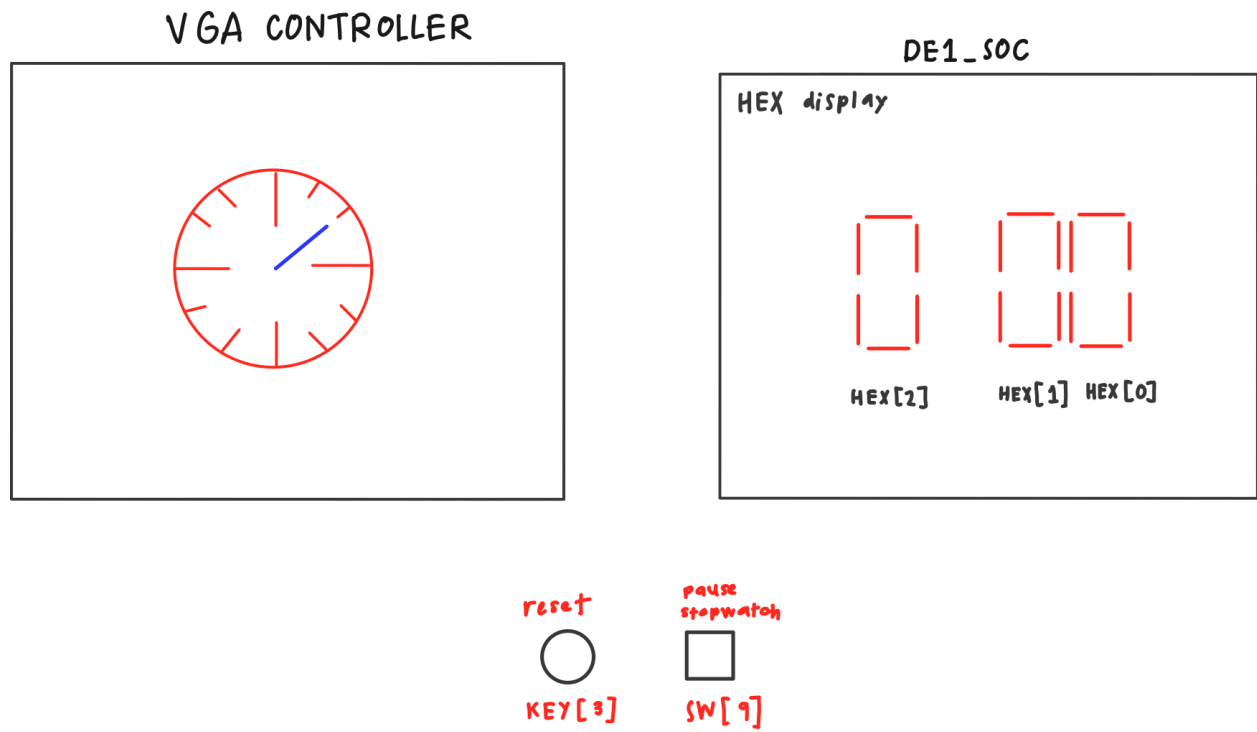


Figure 2: rough visual sketch of lab 6