

# PCIe Error Handling in Switchtec

# References

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## Device Specification

[Device Specification - Switchtec PSX 96xG3 PCIe Storage Switch Issue 9](#)

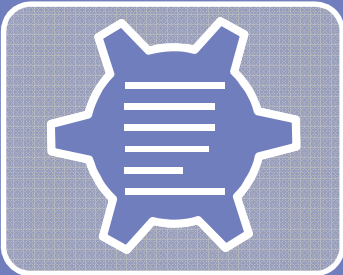
[Device Specification - Switchtec PFX 96xG3 PCIe Fanout Switch Issue 8](#)



## Chiplink

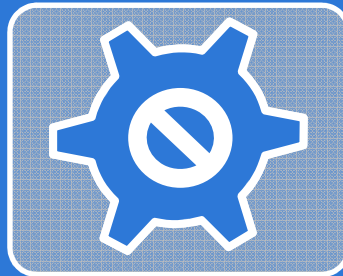
[ChipLink Diagnostic Tool - Core Installer \(Windows\) v1.34.19 \[Config v1.5.0.36 \(51\)\]](#)

# Key Features



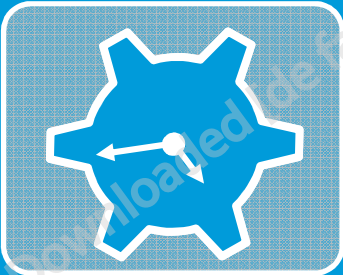
## AER

- Advanced Error Reporting
- PCI-SIG Base Specification 3.1



## DPC

- Downstream Port Containment
- PCI-SIG Base Specification 3.1



## CTS

- Completion Timeout Synthesis
- Switchtec Proprietary



AER



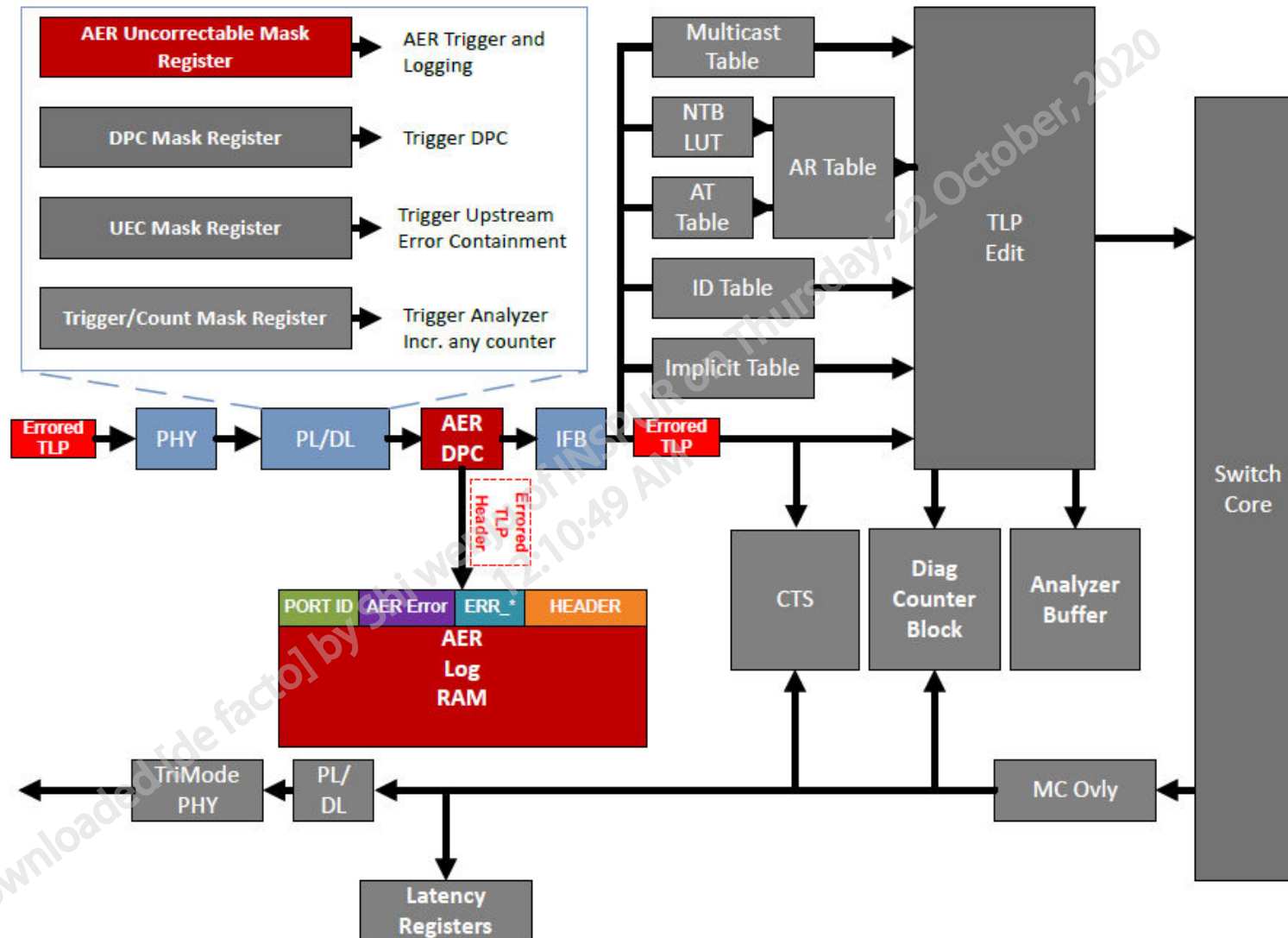
# AER Overview

DevSpec  
§:9.1

- Switchtec AER is fully compatible with PCI-SIG Base Specification 3.1
- AER is configured by host through Advance Error Reporting PCIe Capability entry
- AER detects correctable and uncorrectable errors and logs the TPL header
- The PFX/PSX uses a combination of both HW and FW
  - HW handles error detection
  - FW handles error reporting and logging
- PSX allows for additional customization from the default error handling procedure through the API

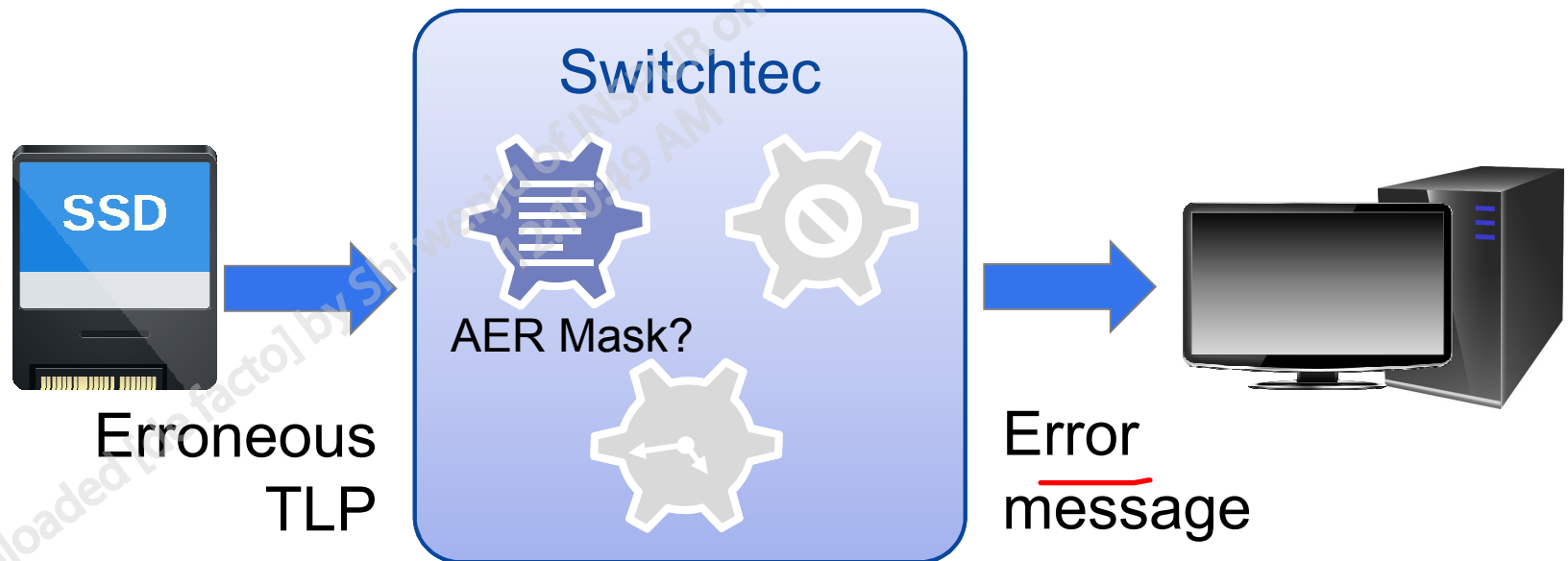
# AER Hardware

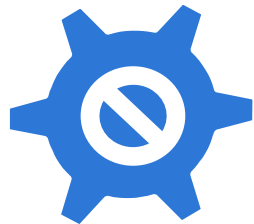
DevSpec  
§:9.1



# AER Walkthrough

- HW checks TLPs for correctable and uncorrectable errors
- Switch compares TLP errors to AER masks
- AER is invoked if error is unmasked
- TLP header is logged by FW and host is notified of AER event





DPC





# DPC Overview

DevSpec  
§:9.2

- Switchtec DPC is fully compatible with PCI-SIG Base Specification 3.1
- DPC is configured by host through the DPC Extended Capability PCIe Capability entry
- Upon detection of an unmasked and uncorrectable error from the DSP
  - DPC discards the error
  - The DS Link LTSSM goes to DISABLE3
- DPC HW returns a UR or CA (depending on configuration)
- After DPC trigger status can be cleared in CSR or automatically (DPC auto-clear is a Switchtec feature)

# DPC Setup

## ChipLink Partition Setting

- DPC Completion Control:
  - UR or CA as per CSR
  - Disable DPC Completion
- Completion on Link Down with no DCP
  - UR: Unsupported Request
  - Disabled
- Time interval to automatically clear DCP Trigger (set to non 0 to enable feature)

Partition Instance # 0

Partition Config Valid ☒ Enabled

Partition Enable ☒ Enabled

Reset Partition on USP link down ☒ Enabled

Max Payload Size 128 bytes max payload size

Supported Max Payload Size 512 bytes max payload size

Partition Port Map

P2P	Physical Port	Enabled on Boot			
USP	Port 40	<input checked="" type="checkbox"/>			
DSP #1	Port 0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
DSP #2	Port 8	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
DSP #3	Port 16	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
DSP #4	Port 24	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Add Port		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

USP Mode USP with NT EP

USP Port MGMT EP Index Management Endpoint Instance #0

USP Port NT EP Index NTB Setting Instance #0

Enable CTS on USP ☐ Enabled

DPC Completion Control Spec compatible completion generation

Non DPC Completion Control Always return UR

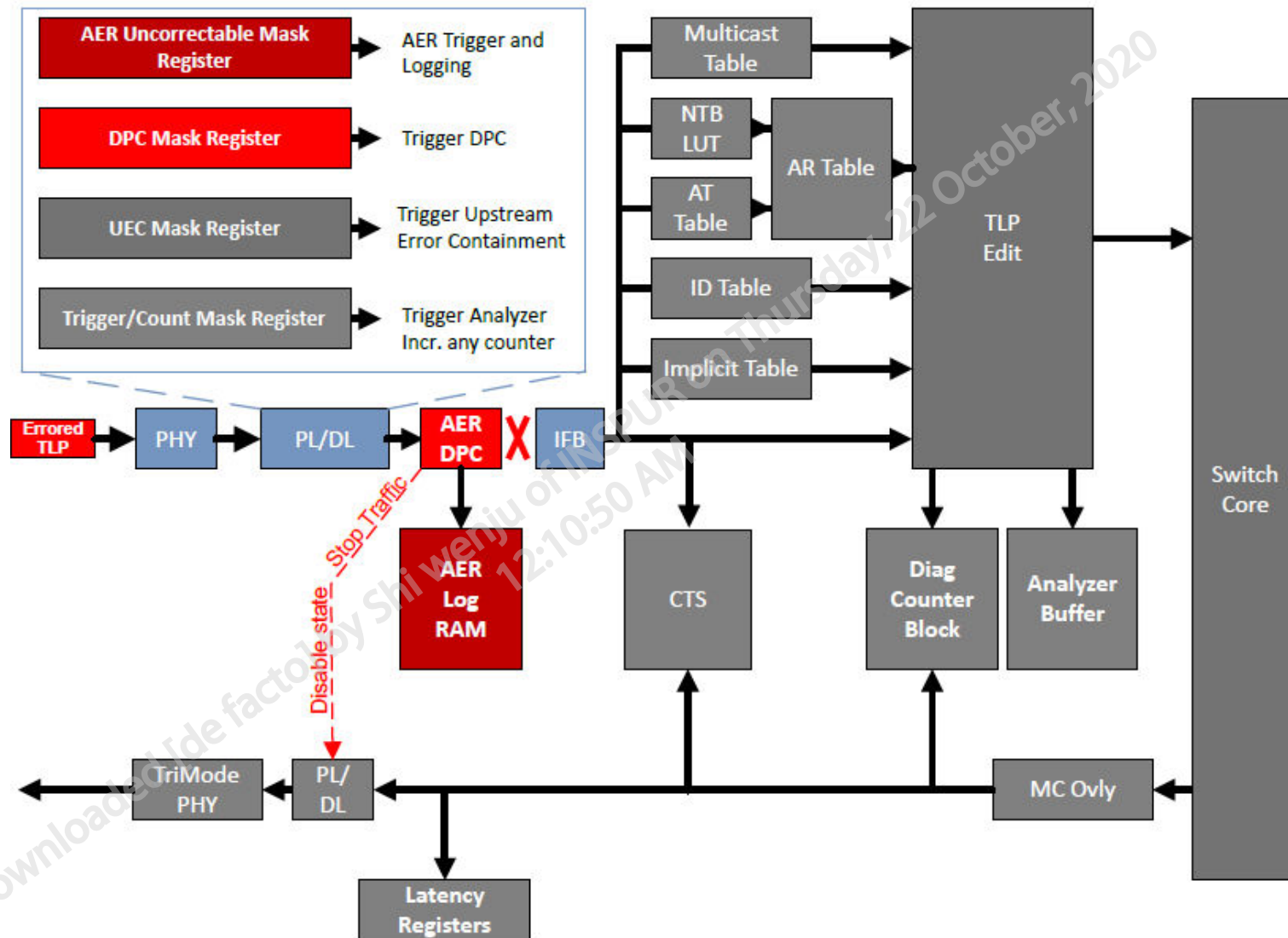
DPC Auto Clear Interval 0

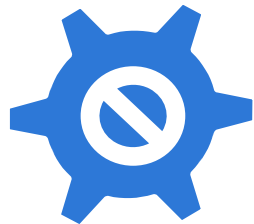
CTS - Synthesized CPL For Configuration Non-Posted Request UR

CTS - Synthesized CPL For Non Configuration Non-Posted Request UR

# DPC Hardware

DevSpec  
§:9.2



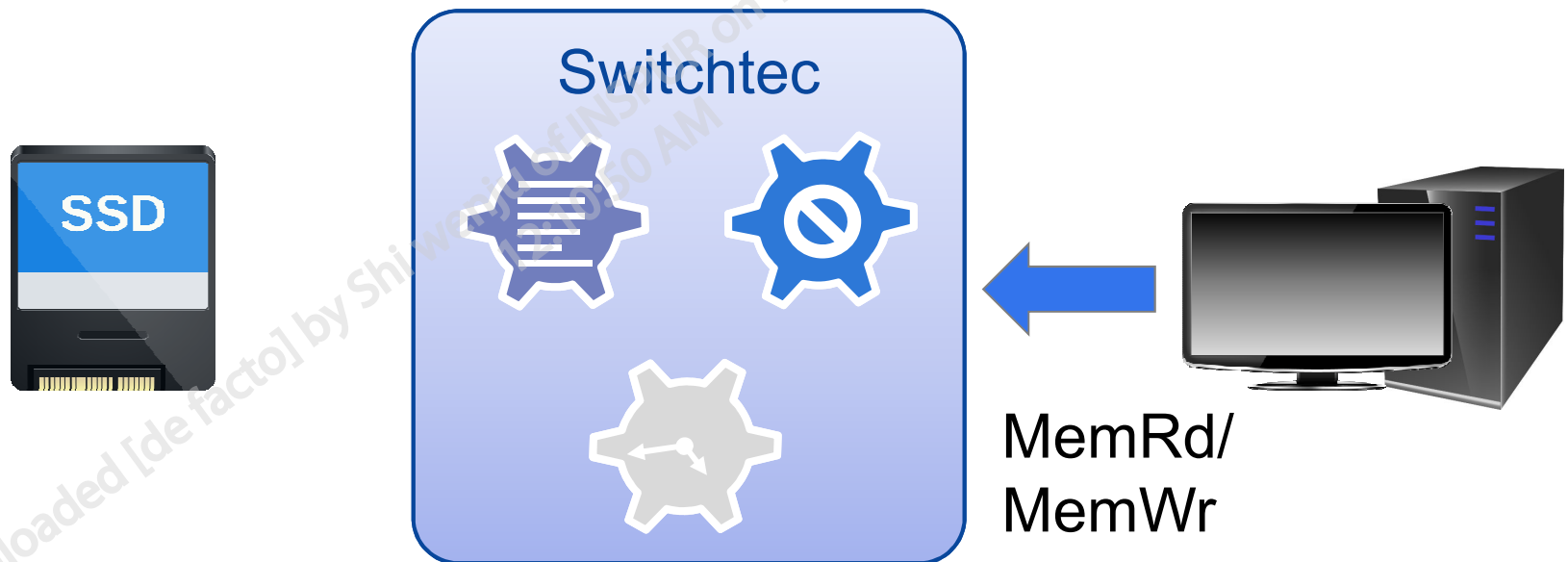


# DPC Walkthrough #1

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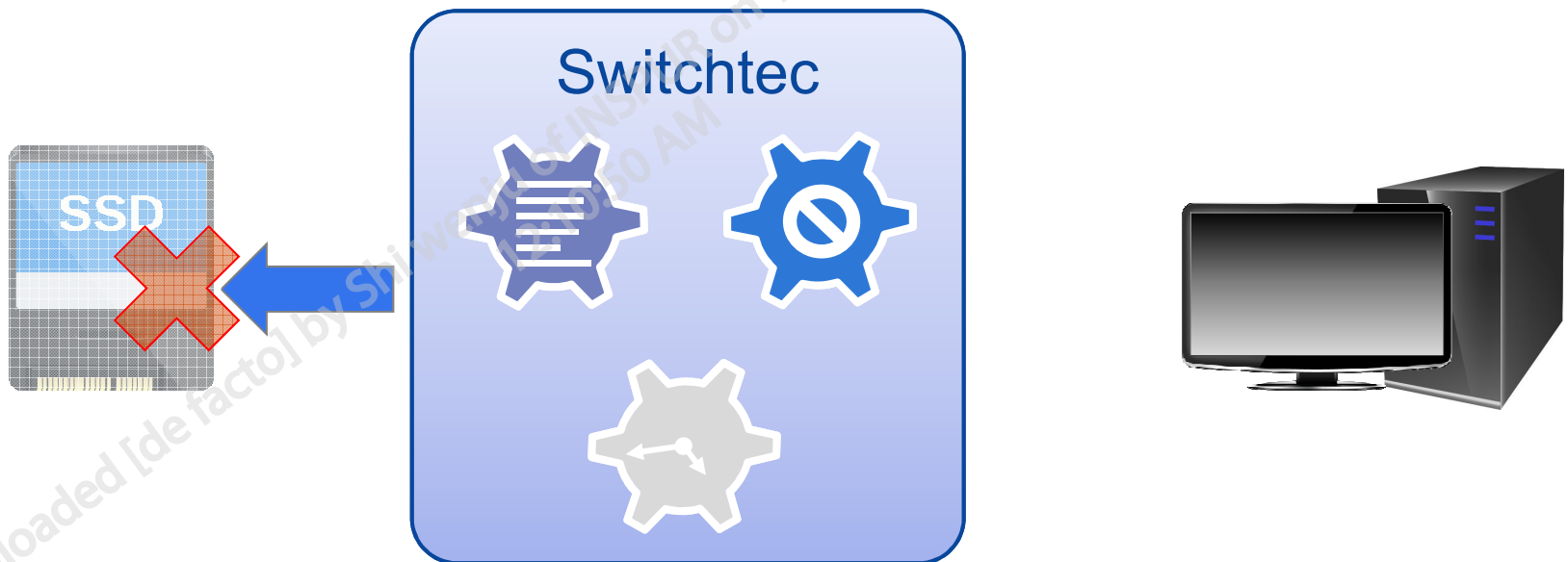
# DPC Walkthrough #1

- Host sends a posted or non posted to the EP



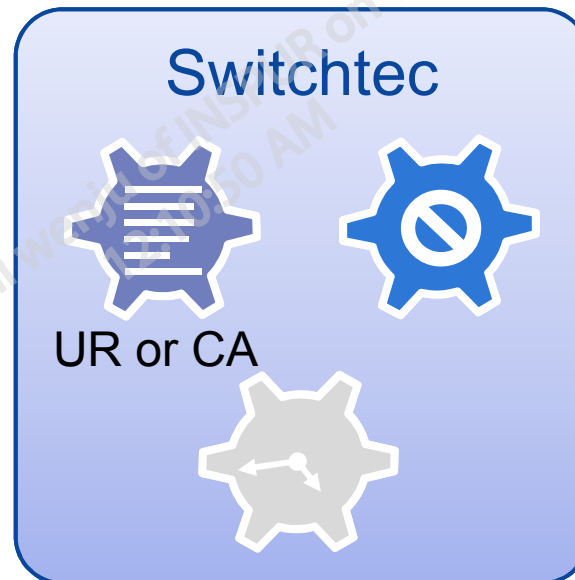
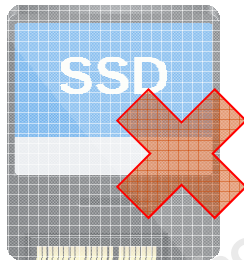
# DPC Walkthrough #1

- Drive is removed before the TLP reaches the egress port
- Posted TLPs are silently discarded



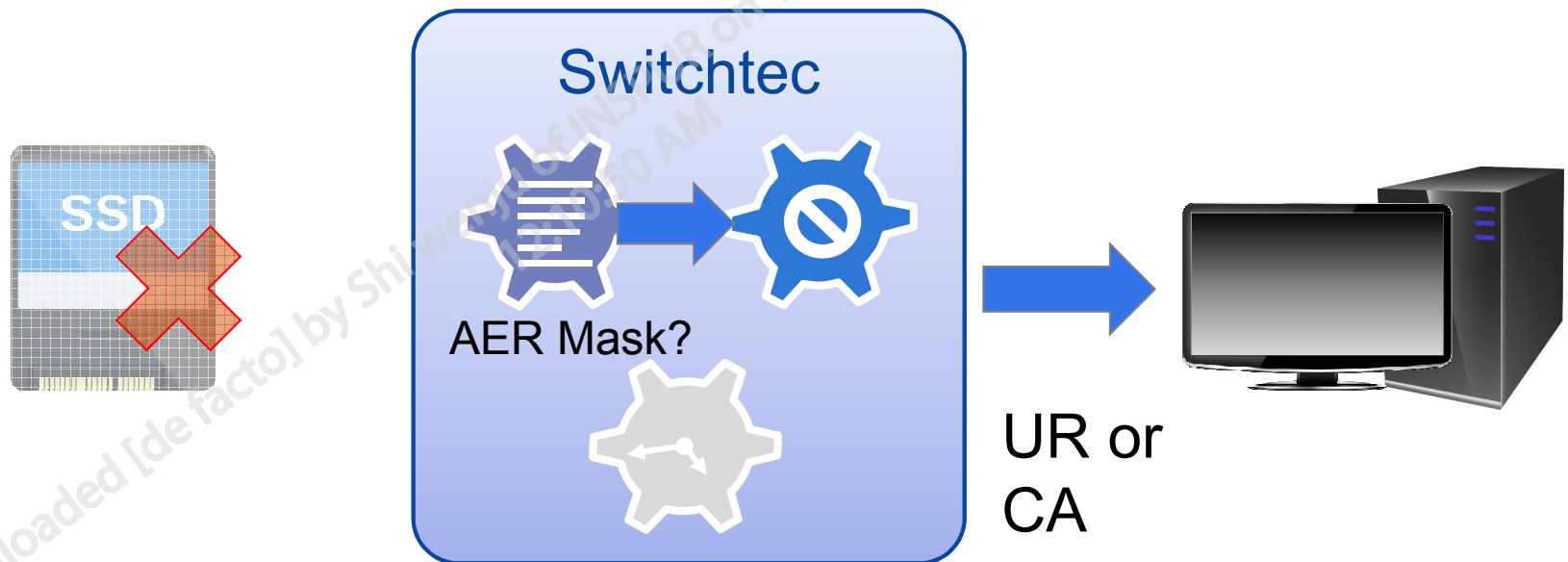
# DPC Walkthrough #1

- Any NP TLPs are flagged as unrouteable, an uncorrectable error is generated
- A Unsupported Request (UR) or Completer Abort (CA) completion is generated for the error which are both tagged in AER



# DPC Walkthrough #1

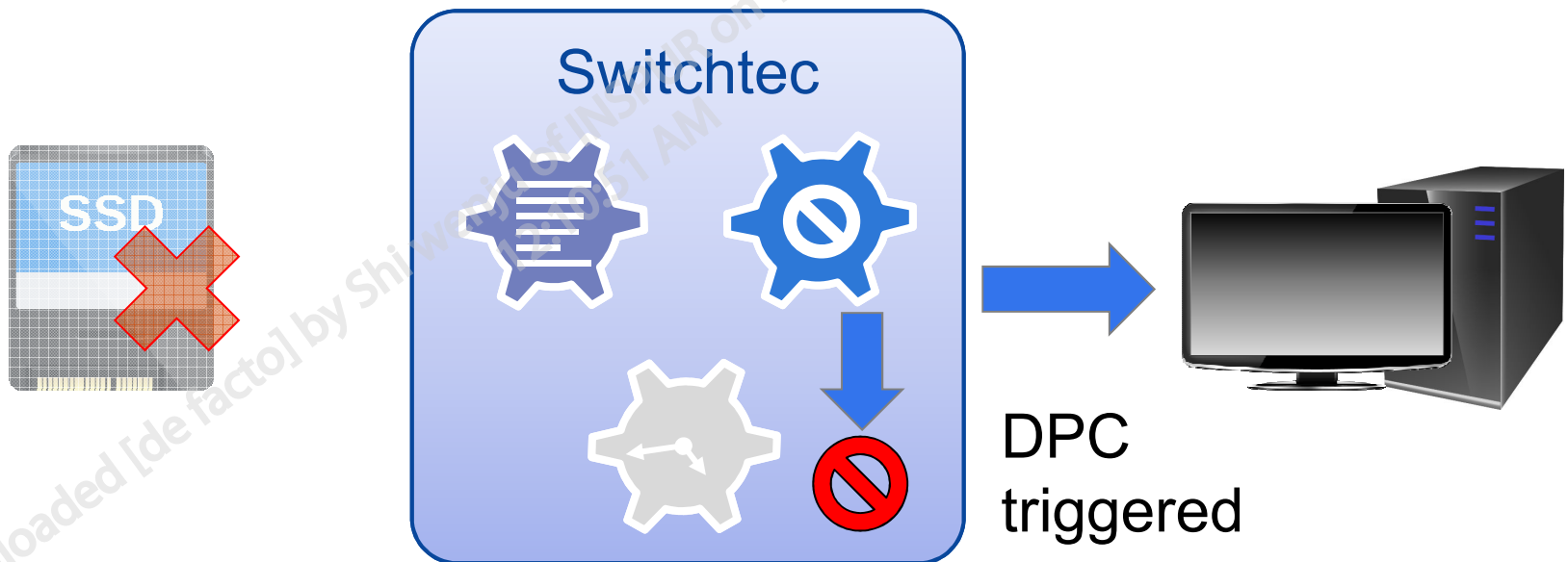
- Switch checks AER masks to see if UR/CA error is masked
- If not masked, DPC triggers and AER does not generate ERR\_NON\_FATAL

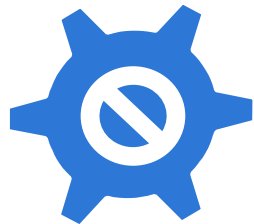




# DPC Walkthrough #1

- Any TLPs in the downstream port buffer are silently discarded
- Host is notified that DPC has triggered



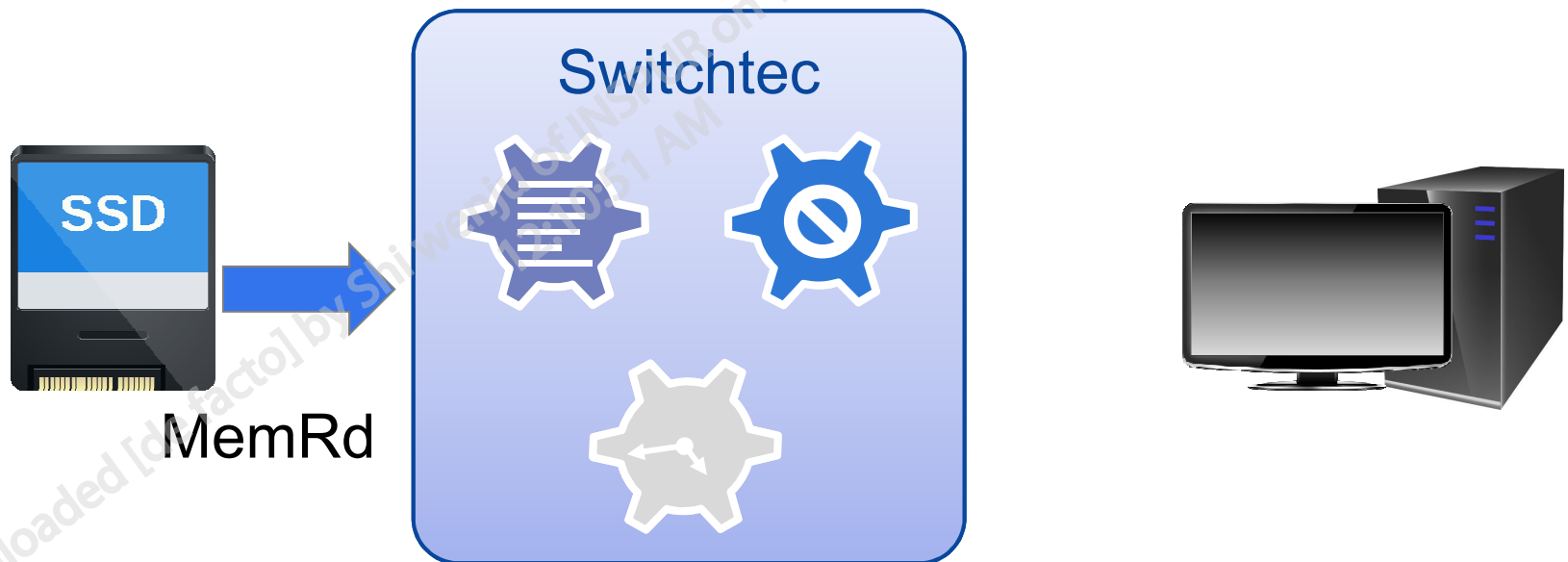


## DPC Walkthrough #2

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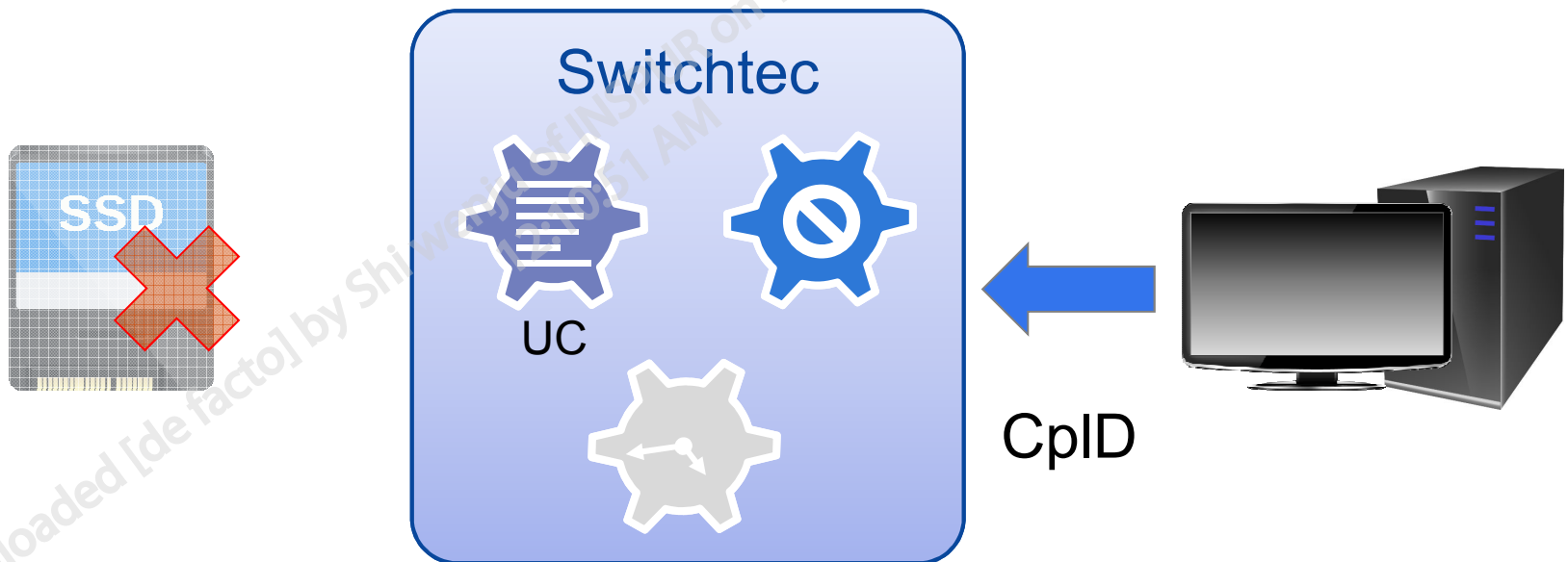
# DPC Walkthrough #2

- EP sends NP to host (like MemRd)



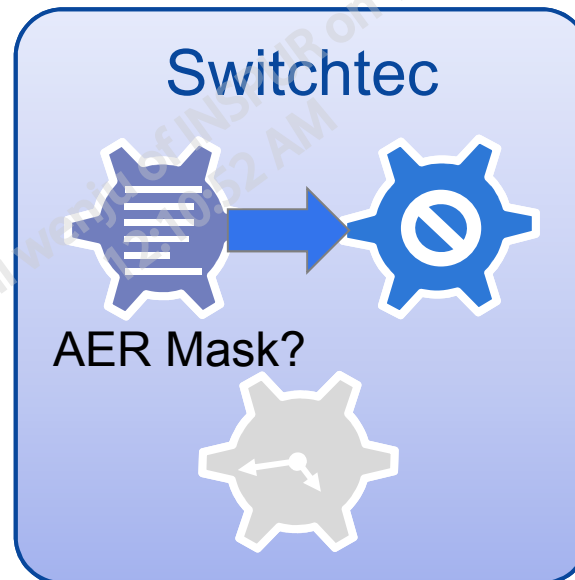
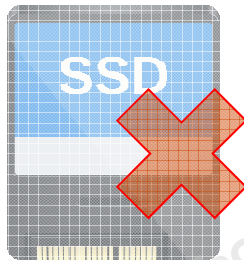
# DPC Walkthrough #2

- Host sends CplD back to EP but EP is removed
- CplD has no destination and AER marks it as unexpected completion (UC)



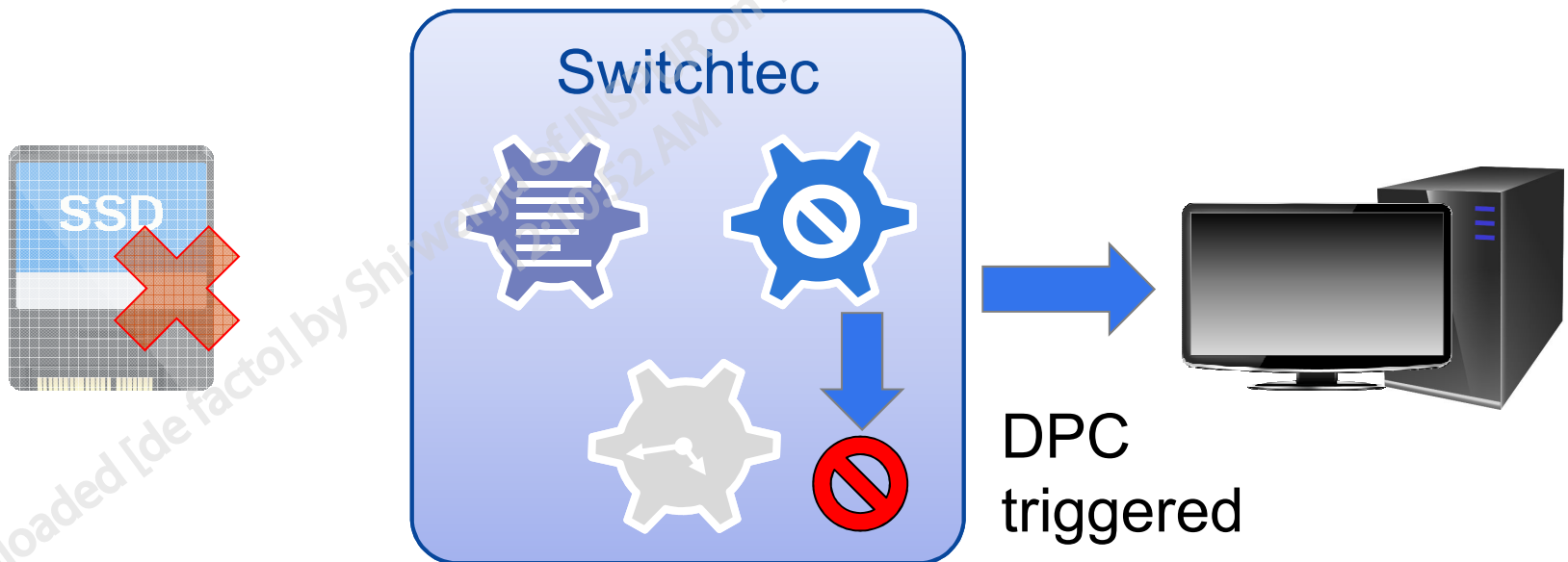
# DPC Walkthrough #2

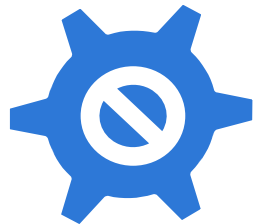
- Switch checks that UC is not masked with AER
- If not masked, then DPC triggers and AER takes no further action



# DPC Walkthrough #2

- DPC silently discards the UC
- Host is notified that DPC has triggered



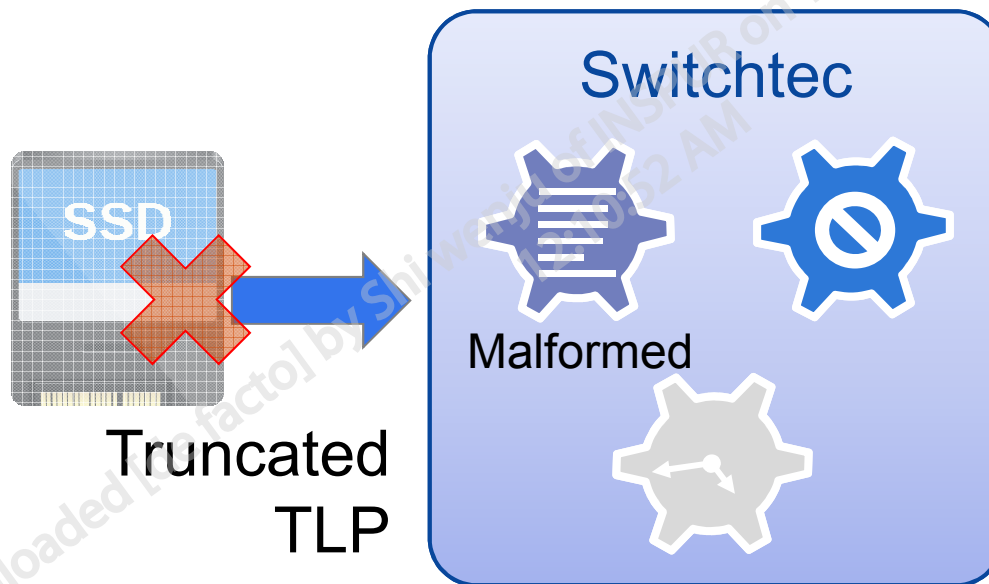


## DPC Walkthrough #3

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# DPC Walkthrough #3

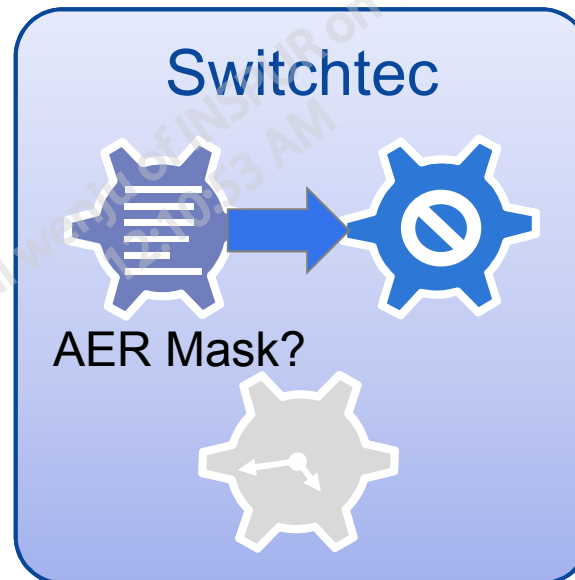
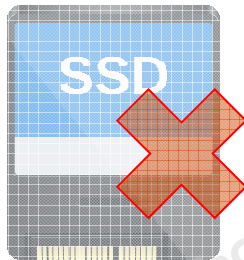
- EP sends a TLP towards the host that is truncated due to EP removal
- TLP is marked as malformed by AER





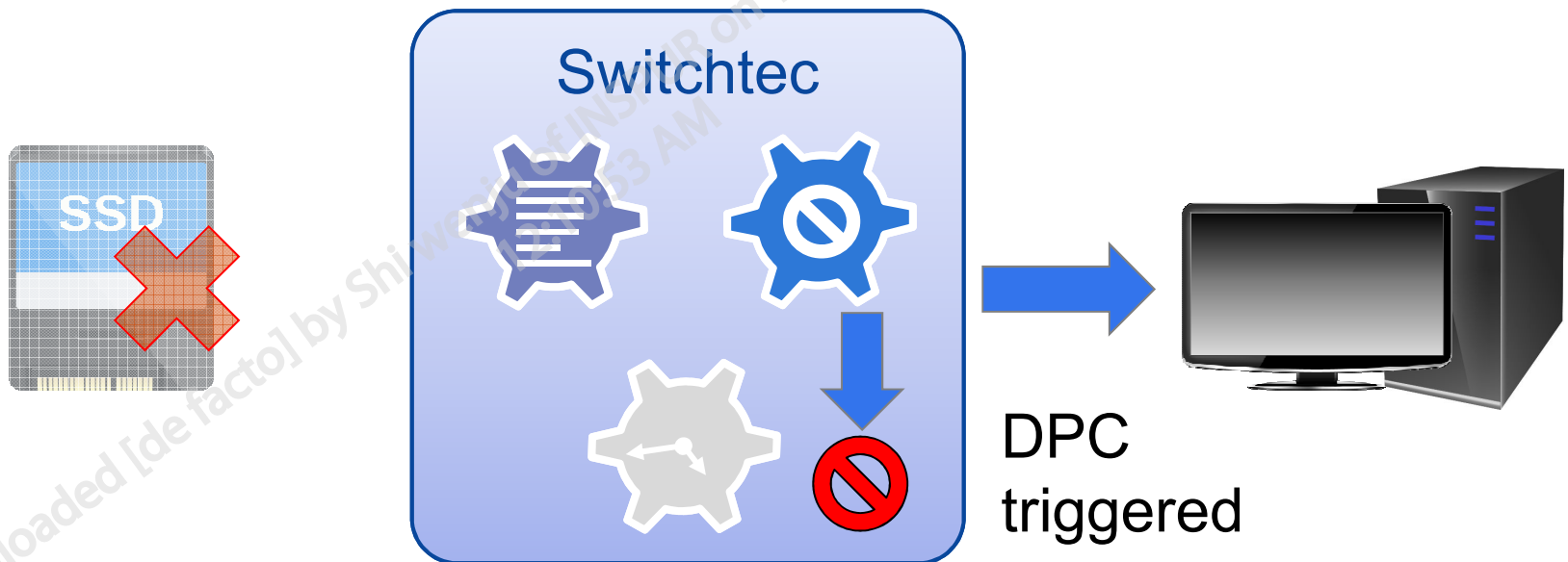
# DPC Walkthrough #3

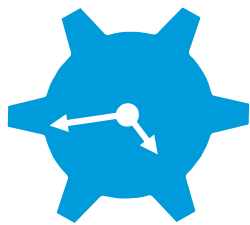
- Switch checks AER masks
- DPC will trigger if “Malformed TLP Error” is unmasked



# DPC Walkthrough #3

- Error is logged in AER
- Malformed TLP is discarded
- Host is notified that DPC has triggered





CTS



# CTS Overview

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- Microsemi Proprietary mechanism on handling of outstanding non-posted (NP) requests made by the Host
- If a completion does not return after a configurable time period host synthesizes a completion
- CTS can be configured to synthesize UR or an all ones successful completion (SC)
- Without CTS, Host may enter into an error state due to uncompleted NP transactions (Host TMO)

# CTS ChipLink Setup

## ChipLink Partition Setting

- Enable CTS on Partition USP
- Select Cfg TLP Comp Synthesis Type
  - UR: Unsupported Request
  - SC: All ones Success
  - No CPL: No completion
- Select MemRd TLP Comp Synthesis Type
  - UR: Unsupported Request
  - SC: All ones Success
  - No CPL: No completion

**Partition Instance # 0** + -

Partition Config Valid ☒ Enabled ?

Partition Enable ☒ Enabled ?

Reset Partition on USP link down ☒ Enabled ?

Max Payload Size 128 bytes max payload size ?

Supported Max Payload Size 512 bytes max payload size ?

Partition Port Map

P2P	Physical Port	Enabled on Boot			
USP	Port 40	<input checked="" type="checkbox"/>			
DSP #1	Port 0	<input checked="" type="checkbox"/>	<span style="color: green;">+</span>	<span style="color: red;">-</span>	<span style="color: gray;">▲</span>
DSP #2	Port 8	<input checked="" type="checkbox"/>	<span style="color: green;">+</span>	<span style="color: red;">-</span>	<span style="color: gray;">▲</span>
DSP #3	Port 16	<input checked="" type="checkbox"/>	<span style="color: green;">+</span>	<span style="color: red;">-</span>	<span style="color: gray;">▲</span>
DSP #4	Port 24	<input checked="" type="checkbox"/>	<span style="color: green;">+</span>	<span style="color: red;">-</span>	<span style="color: gray;">▲</span>
Add Port			<span style="color: green;">+</span>	<span style="color: red;">-</span>	<span style="color: gray;">▲</span>

USP Mode USP with NT EP ?

USP Port MGMT EP Index Management Endpoint Instance #0 ? ?

USP Port NT EP Index NTB Setting Instance #0 ? ?

Enable CTS on USP ☒ Enabled ?

DPC Completion Control Spec compatible completion generation ?

Non DPC Completion Control Always return UR ?

DPC Auto Clear Interval 0 ?

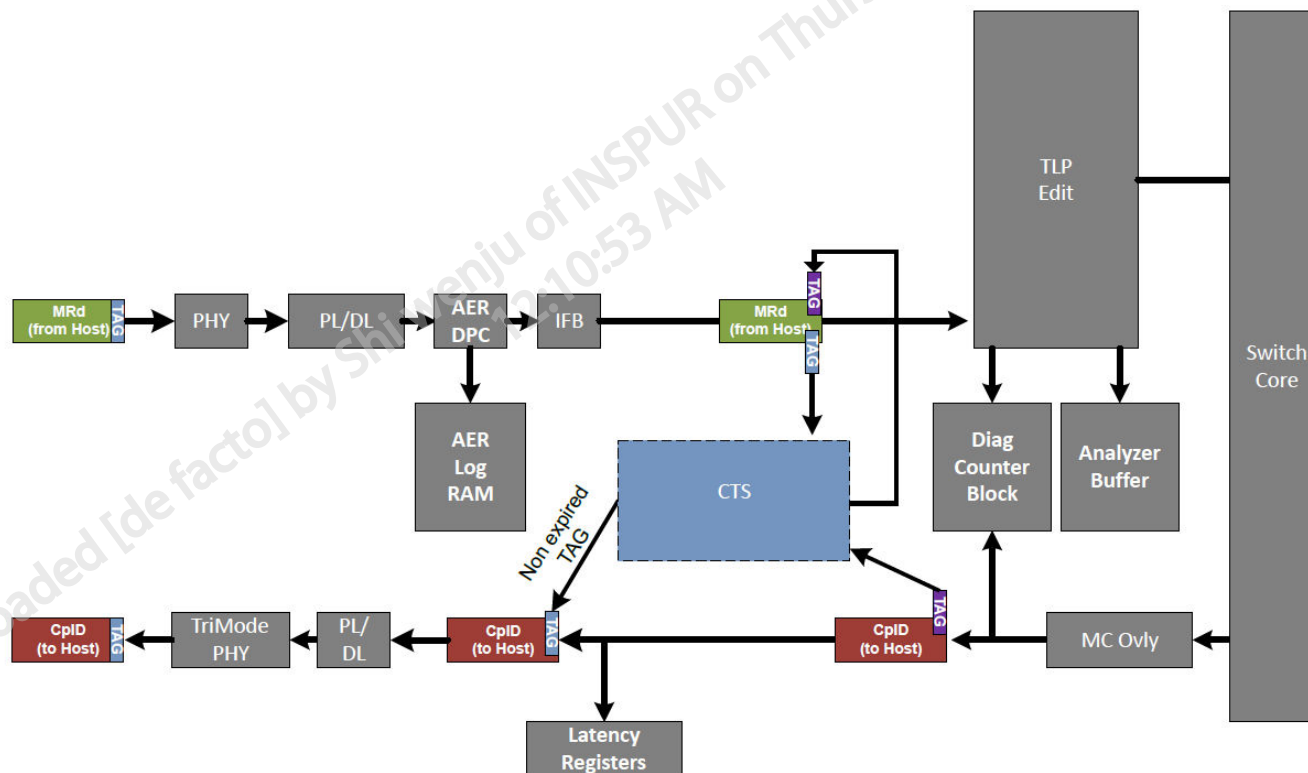
CTS - Synthesized CPL For Configuration Non-Posted Request UR ?

CTS - Synthesized CPL For Non Configuration Non-Posted Request UR ?

# MemRd with Normal Completion

DevSpec  
§:9.5

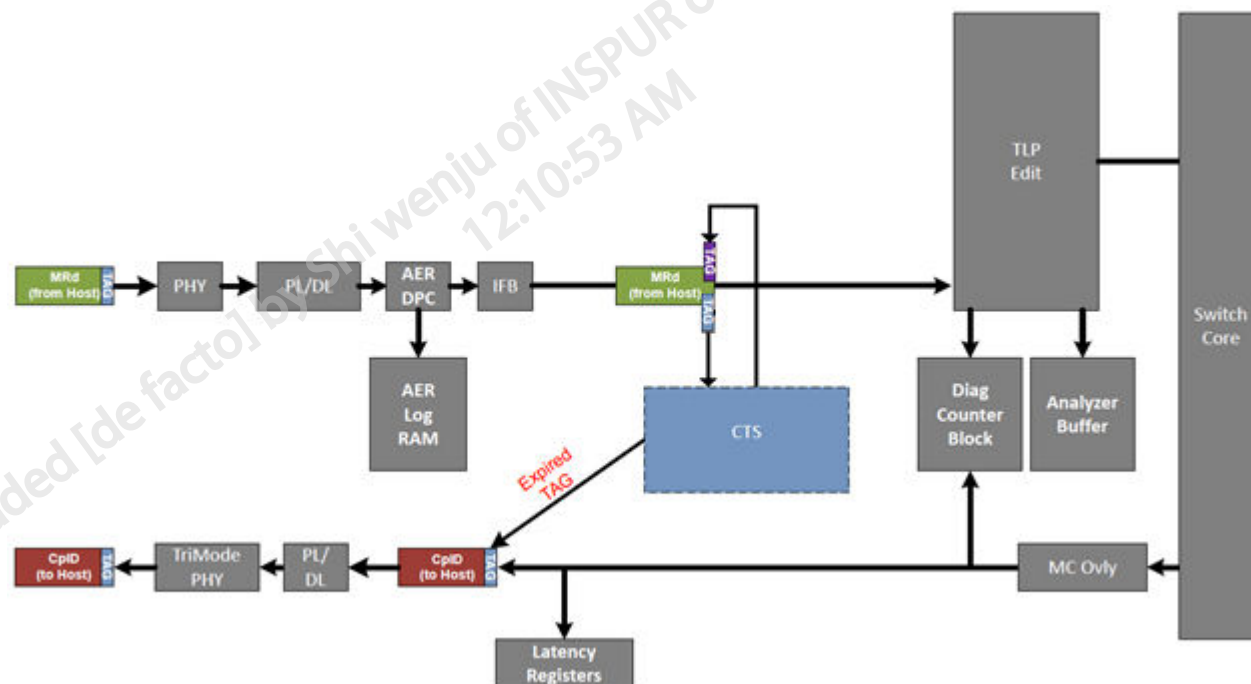
- USP Ingress MemRd TLP **TAG** is saved in CTS RAM and replaced by internal CTS **TAG**
- Upon completion, the CTS **TAG** is used to look-up the TLP **TAG** within the CTS RAM and is added to the responding CpID TLP

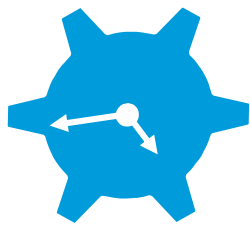


# MemRd with Expired Tag

DevSpec  
§:9.2

- USP Ingress MemRd TLP **TAG** is saved in CTS RAM and replaced by internal CTS **TAG**
- If the originating MemRd TLP times out, CTS will synthesis an all ones SC completion or UR. The timed out CTS **TAG** is used to look-up the TPL **TAG** within the CTS RAM and is added to the responding CpID TPL.





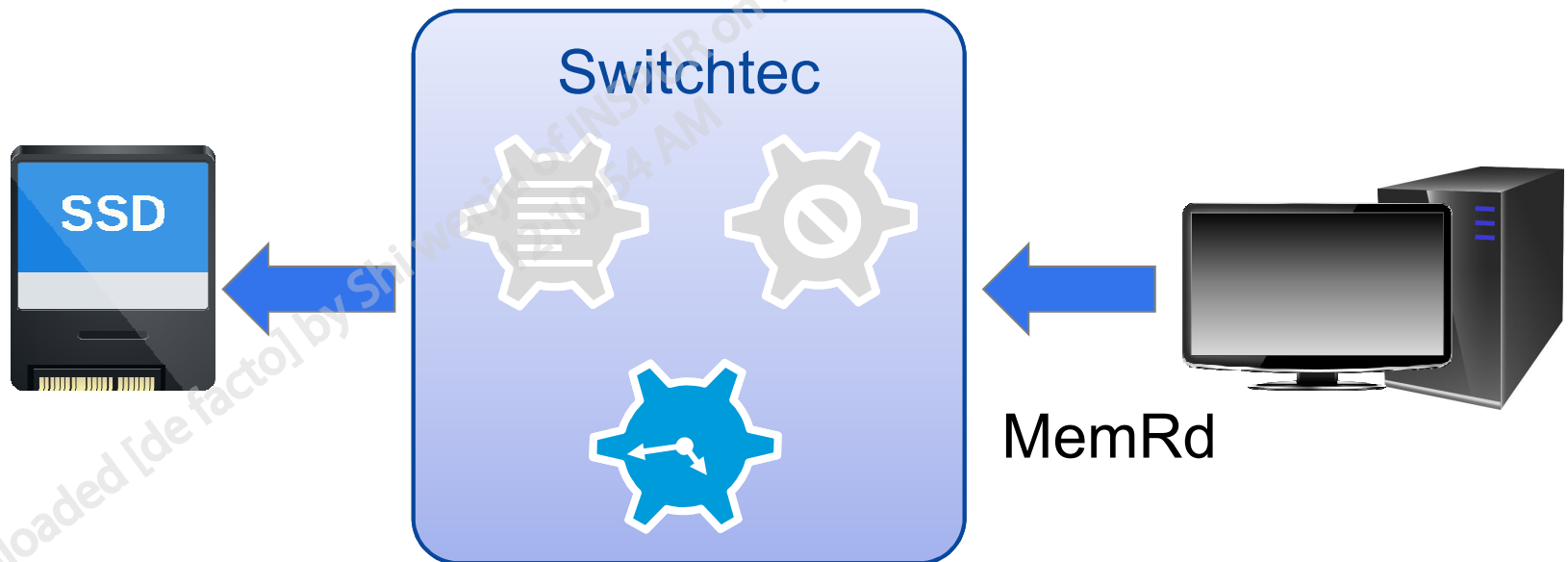
# CTS Walkthrough

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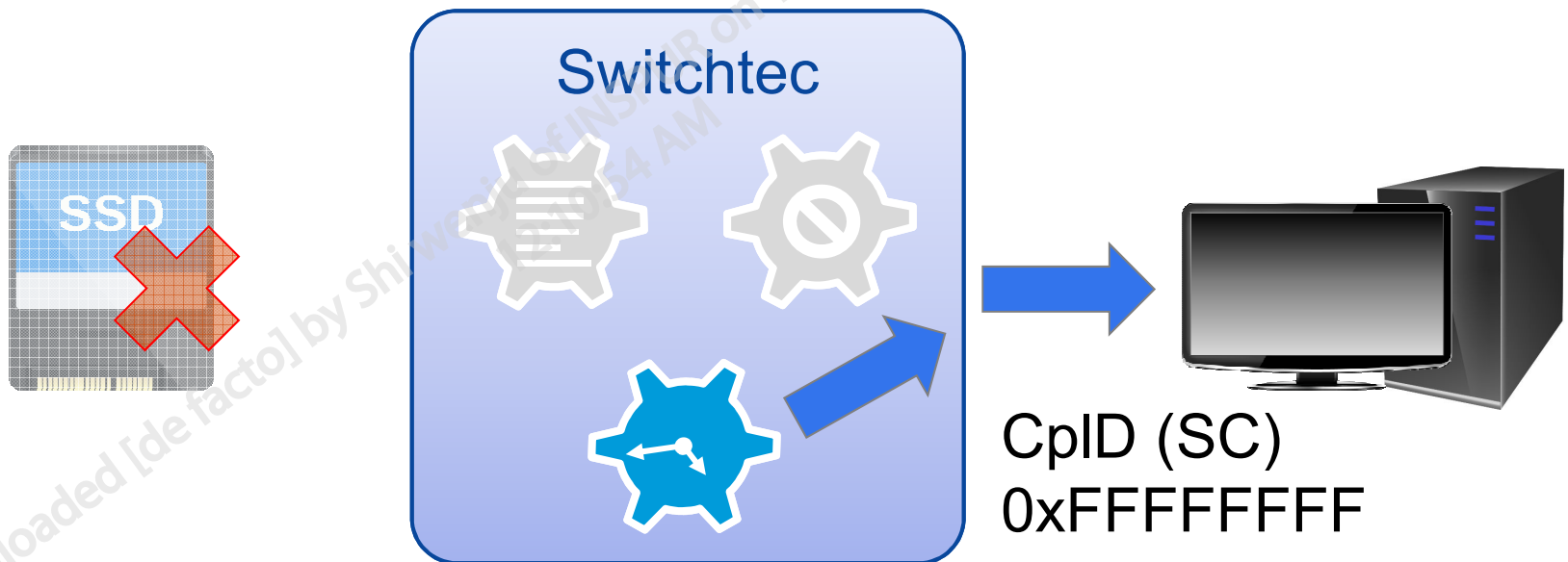
# CTS Walkthrough

- Switchtec Proprietary
- Host sends a MemRd to the EP



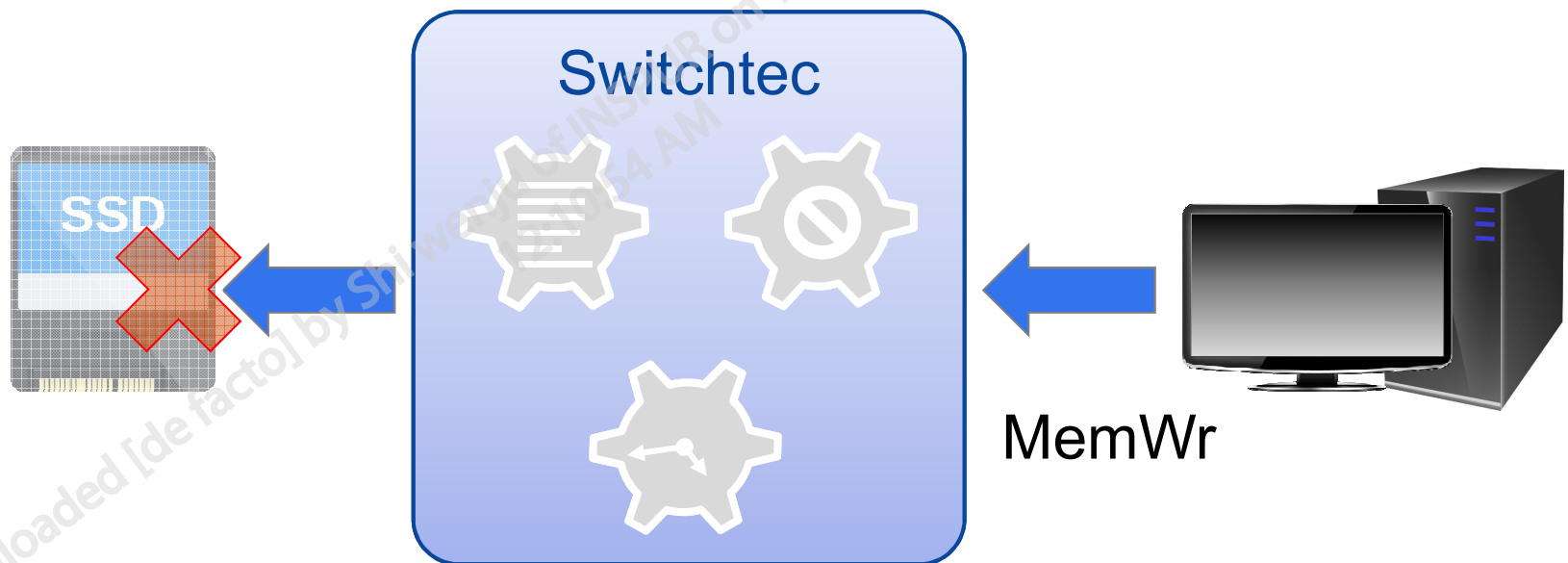
# CTS Walkthrough

- Drive is removed after the NP TLP exits the egress port
- CTS triggers:
  - Switch synthesizes a successful completion (SC) with All-1s data or UR



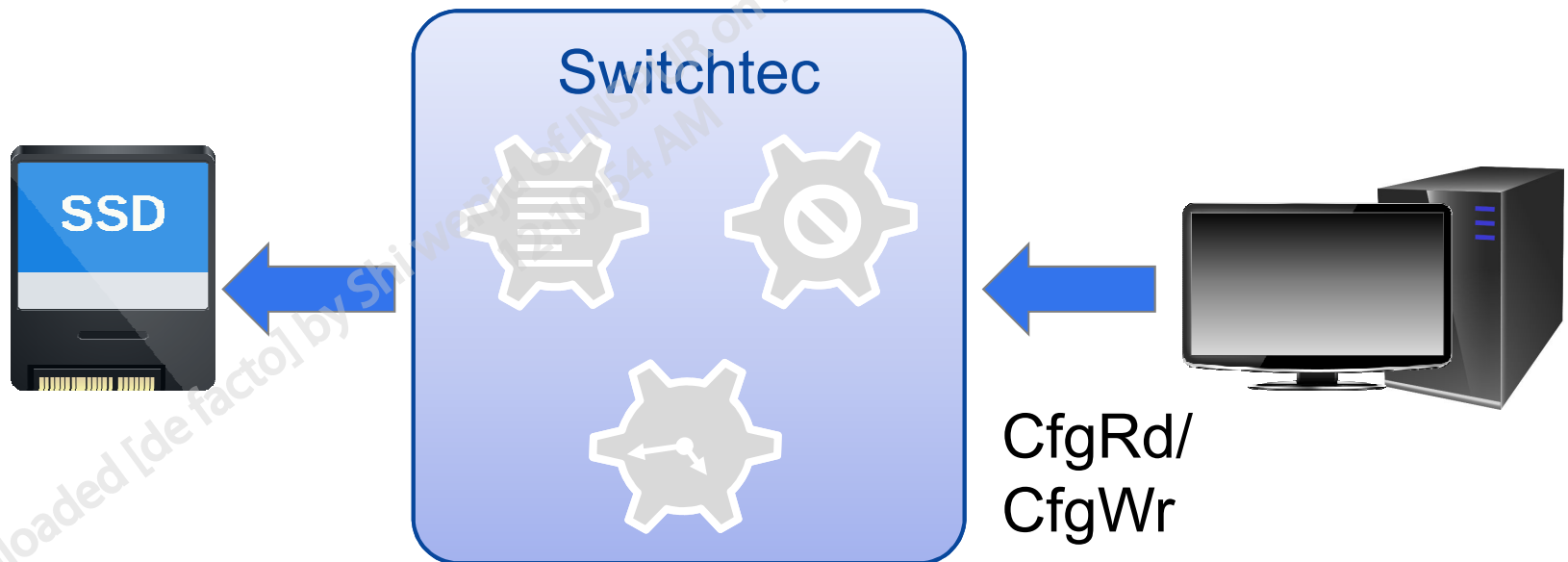
# CTS Walkthrough

- Posted transactions (like MemWr) do not have completions
- These transactions are not tracked and cannot trigger CTS



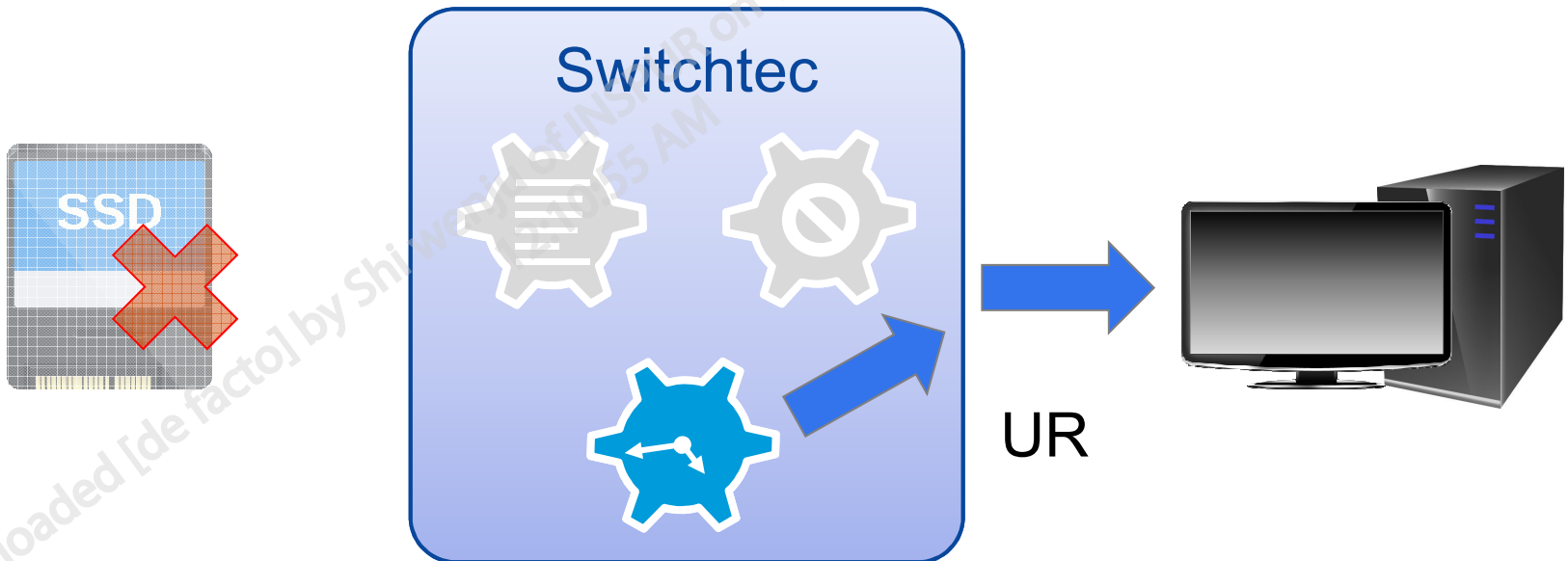
# CTS Walkthrough

- Host sends a config cycle to an EP



# CTS Walkthrough

- EP is removed before completion can be returned
- CTS triggers:
  - Switch synthesizes an unsupported request (UR)



# Questions?



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