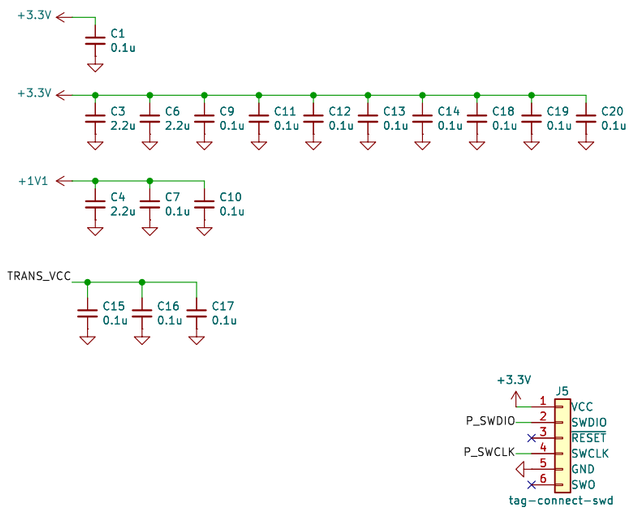
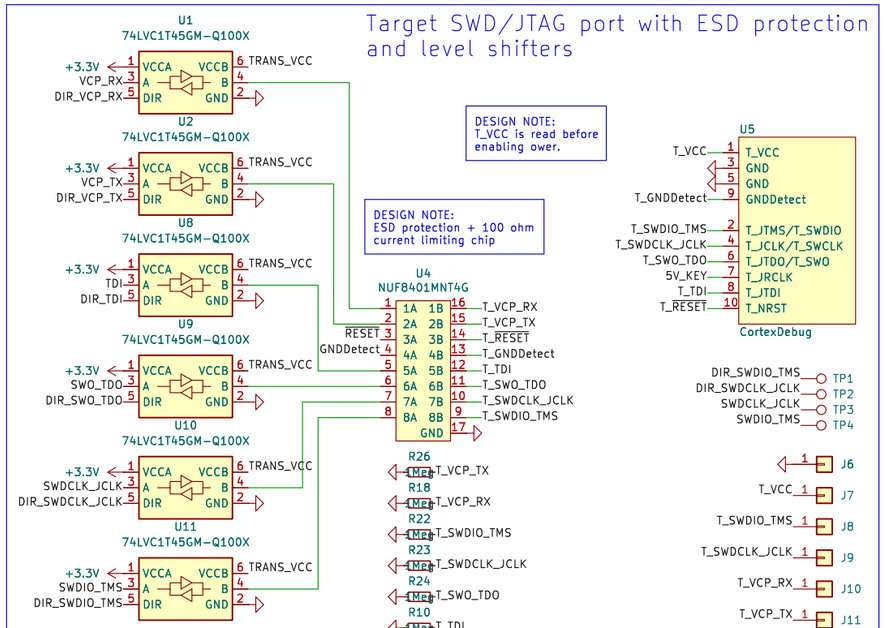
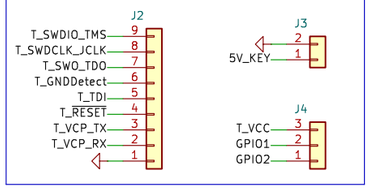
Decoupling capacitors and SWD header



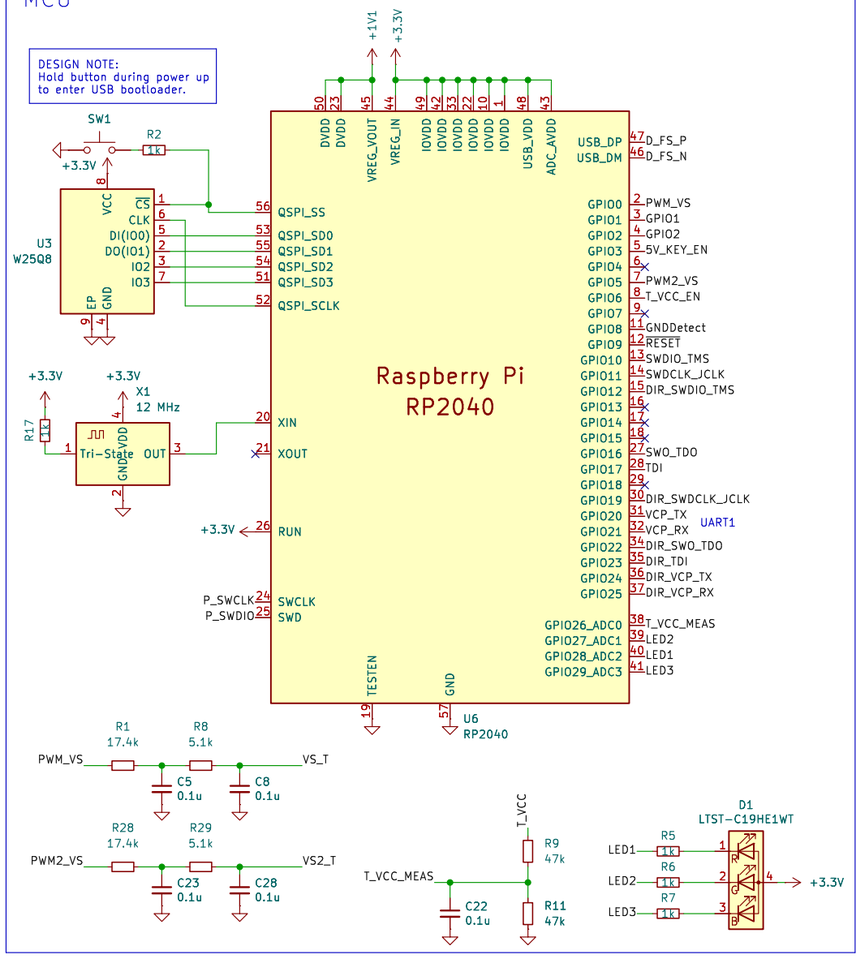
Target SWD/JTAG port with ESD protection and level shifters



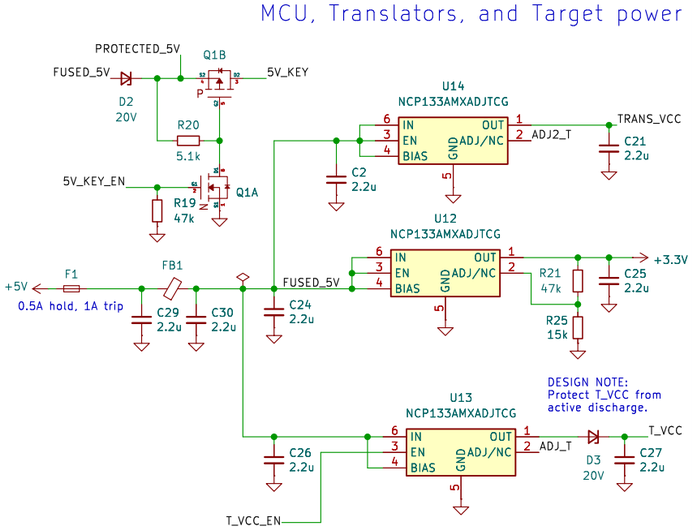
Board-edge castellated vias



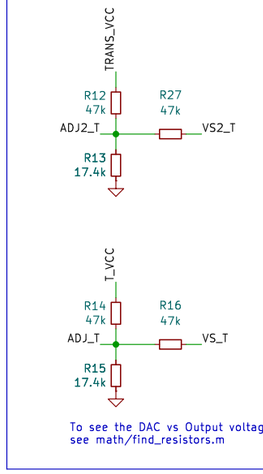
MCU



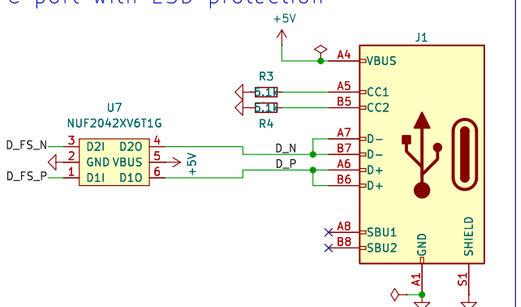
MCU, Translators, and Target power



Target voltage feedback with PWM DAC control



USB-C port with ESD protection



T1 Tab

T2 Tab

Designed by: Emil Fresk
Twitter / Github: @korken89
Link: https://github.com/probe-rs/rs-probe

Sheet: /
File: rs-probe.kicad_sch

Title: The Rusty Probe

Size: A3	Date: 2022-11-28	**Rev: 0**
KiCad E.D.A. 8.0.3		Id: 1/1