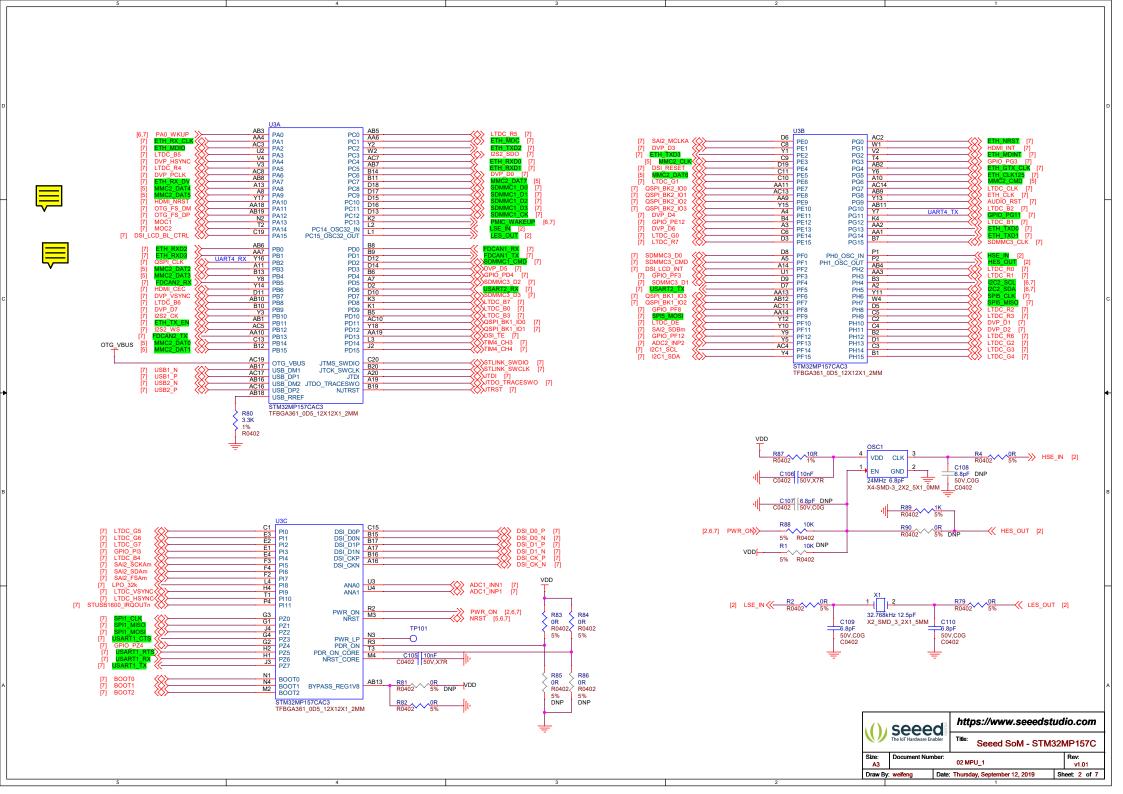
## Schematic: Seeed SoM - STM32MP157C

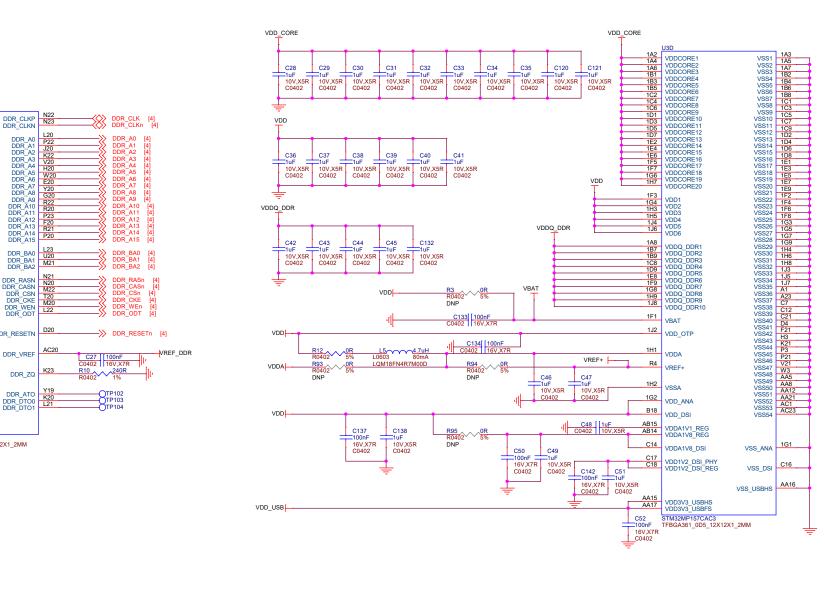
## Revision History

SHEET	SHEET NAME
01	Title/Revision History
02	MPU_1
03	MPU_2
04	DDR3
05	eMMC
06	PMU
07	PINOUT/LED

DATE	REVISION	DESCRIPTION	
2019/05/21	Seeed SoM - STM32MP157C_v1.0_SCH_190521	Initial Release	
2019/09/04	Seeed SoM - STM32MP157C_v1.01_SCH_190904		
2019/12/13	Seeed SoM - STM32MP157C v1.01 SCH 191213	Change R5,R6 from 1k to 2k	







[4] DDR\_D10 [4] DDR\_D11 [4] DDR\_D12 [4] DDR\_D13 [4] DDR\_D15 DDR\_DQS1 DDR\_DQSN1 W21 W23 T23 DDR\_DQ10 DDR\_DQ11 DDR\_DQ12 DDR\_DQ13 DDR\_DQ14 DDR\_DQ15 W22 Y21 U22 U23 DDR\_BA0 DDR\_BA1 DDR\_BA2 DDR\_DQS1P DDR\_DQS1N DDR\_DQM1 V22 DDR DQM1 B22 DDR\_DOM1

X D22 DDR DO16

X D23 DDR DO16

X D23 DDR DO18

X D21 DDR DO19

X D21 DDR DO20

X D22 DDR DO20

X D22 DDR DO22

X D22 DDR DO22

X D23 DDR DO25

X D23 DDR DO25

X D25 DDR DO25

X D27 DDR DOS2P

X D27 DDR DOS2P DDR\_CSN DDR\_CKE M20
DDR\_WEN L22
DDR\_ODT DDR\_RESETN XY23 Y22 AB21 AB20 DDR VREF DDR DQ24 DDR\_DQ24
DDR\_DQ25
DDR\_DQ26
DDR\_DQ27
DDR\_DQ28
DDR\_DQ29
DDR\_DQ30
DDR\_DQ31 DDR\_ZQ AC22 AC21 AA23 AA22 AB22 AB23 AA20 DDR\_ATO DDR\_DTO0 DDR\_DTO1 DDR\_DQS3P DDR\_DQS3N DDR\_DQM3 STM32MP157CAC3 TFBGA361\_0D5\_12X12X1\_2MM

DDR\_DQ0
DDR\_DQ1
DDR\_DQ1
DDR\_DQ2
DDR\_DQ3
DDR\_DQ4
DDR\_DQ5
DDR\_DQ6
DDR\_DQ7
DDR\_DQ7
DDR\_DQ70
DDR\_DQ80P

DDR\_DQS0N DDR\_DQM0

DDR\_DQ8 DDR\_DQ9 DDR\_DQ10

E22

J21 J22 H22 G21

G22 G23 H23

DDR\_D0 DDR\_D1

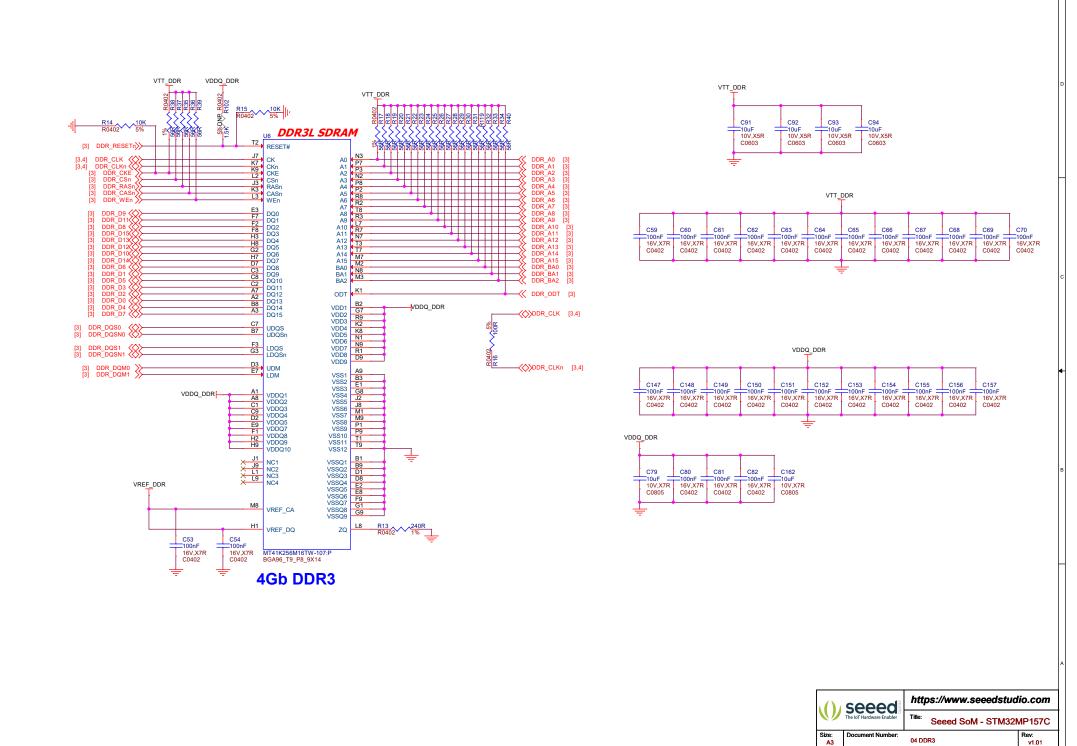
DDR\_D2 DDR\_D3

DDR\_D8

DDR\_D9 <

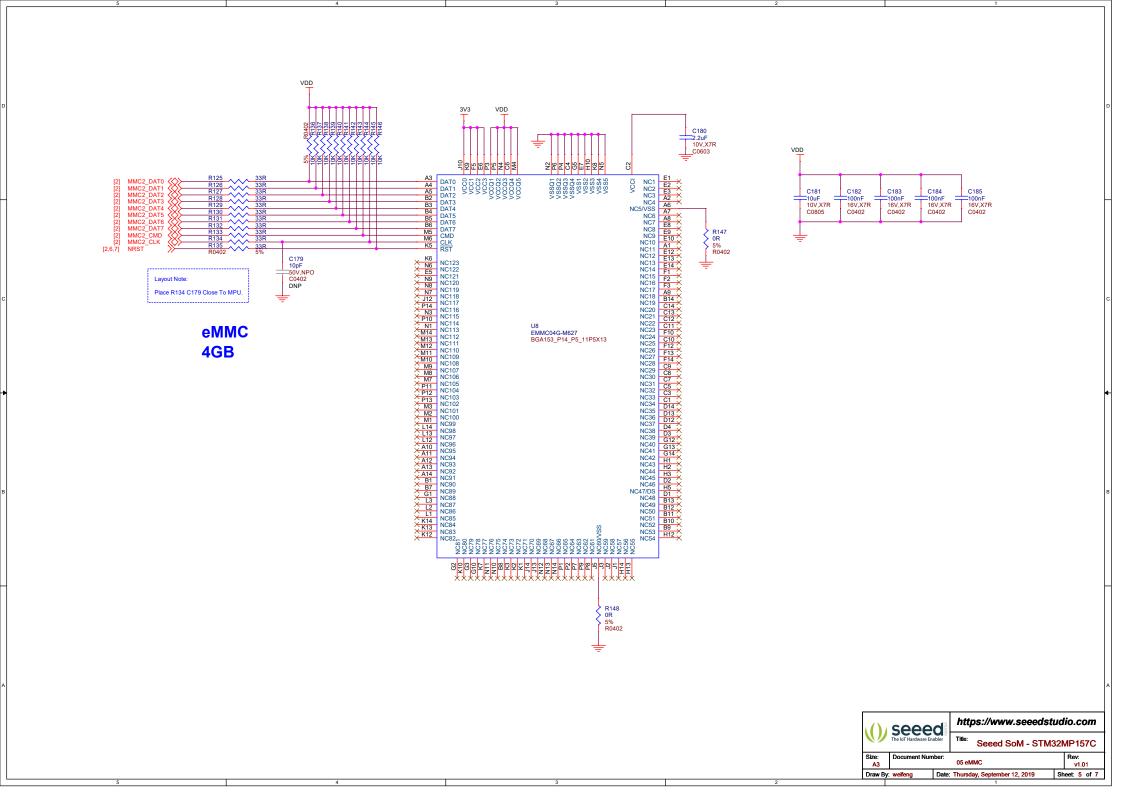
[4] DDR\_D3 [4] DDR\_D4 [4] DDR\_D5 [4] DDR\_D6 [4] DDR\_D7 DDR\_DQS0 DDR\_DQSN0

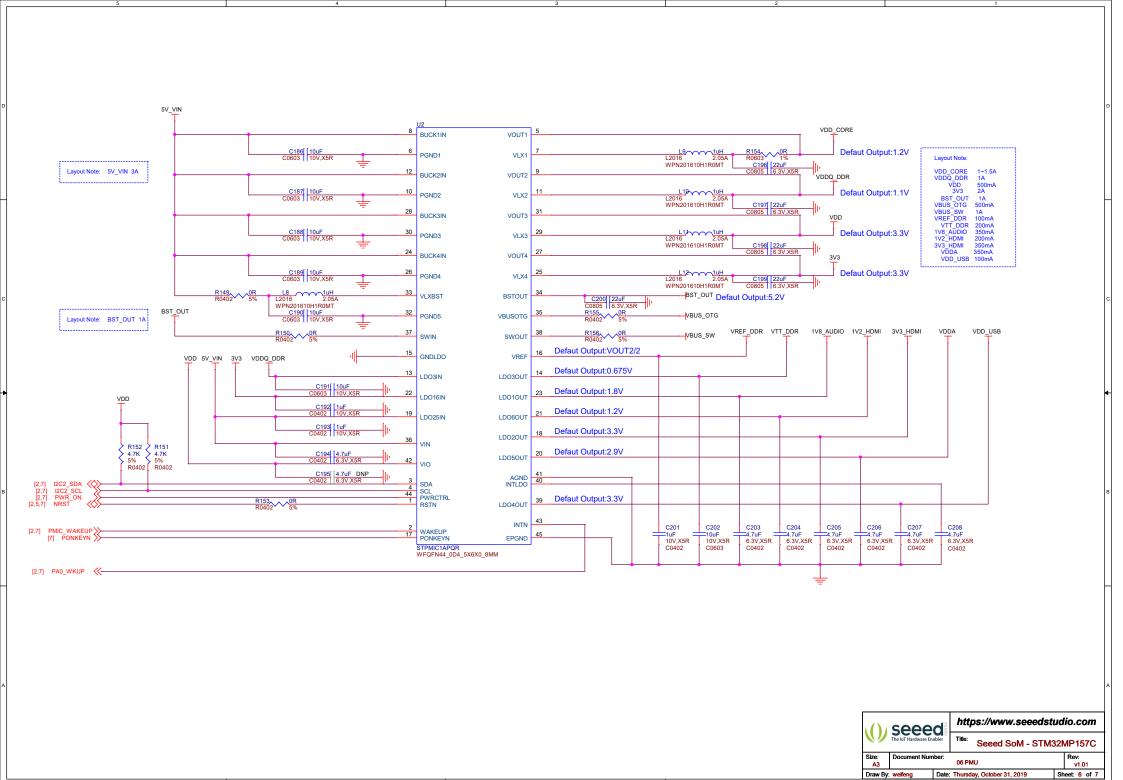
https://www.seeedstudio.com seeed Seeed SoM - STM32MP157C Size: 03 MPU\_2 v1.01 Sheet: 3 of 7 Date: Thursday, September 12, 2019 Draw By: weifeng

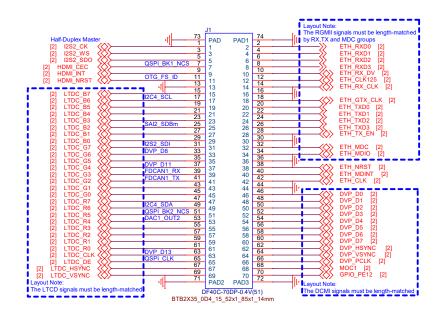


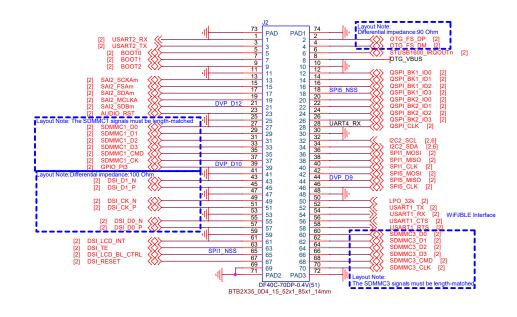
Sheet: 4 of 7

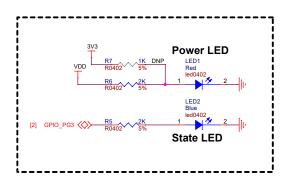
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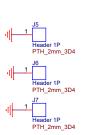


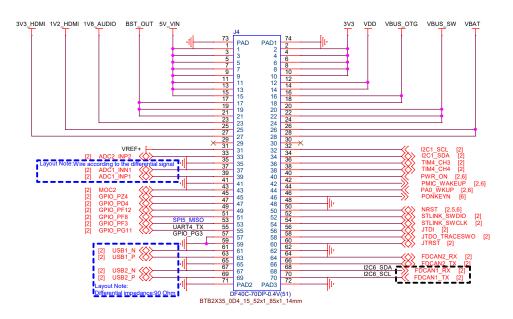












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07 PINOUT/LED

Date: Friday, December 13, 2019

Seeed SoM - STM32MP157C

v1.01 Sheet: 7 of 7

seeed

Size:

Draw By: welfeng