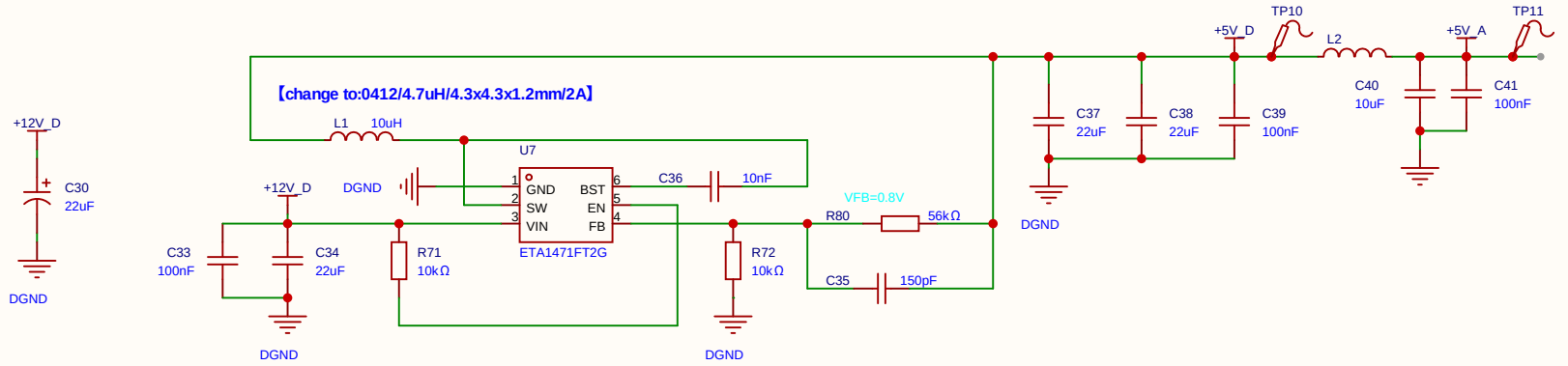
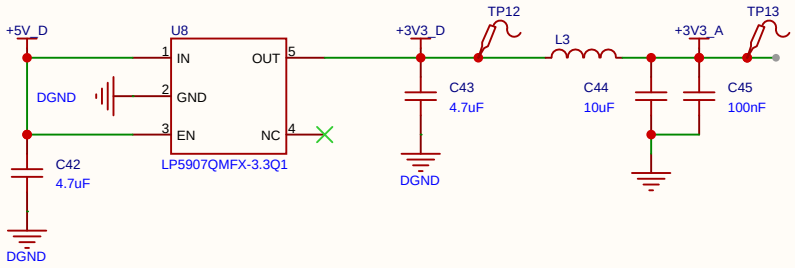
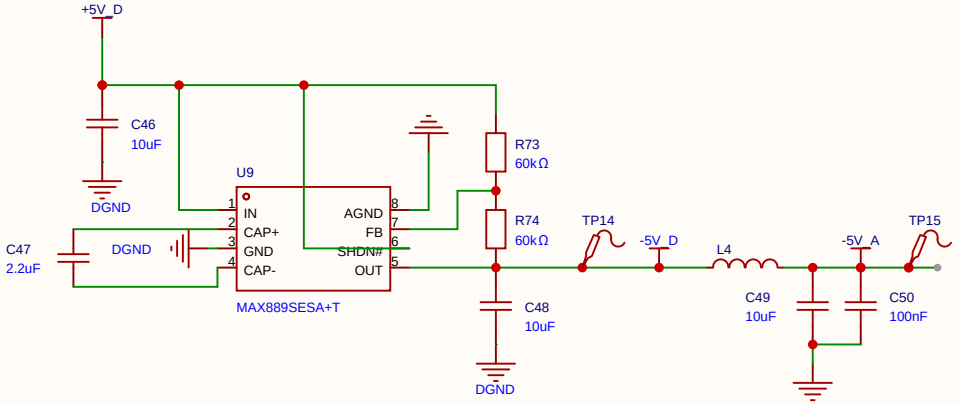


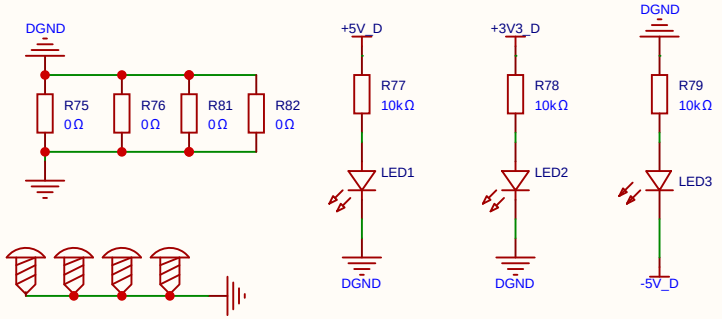
+12V_D ~ +5V_D(+5V_A)



+5V_D ~ +3V3_D(+3V3_A)



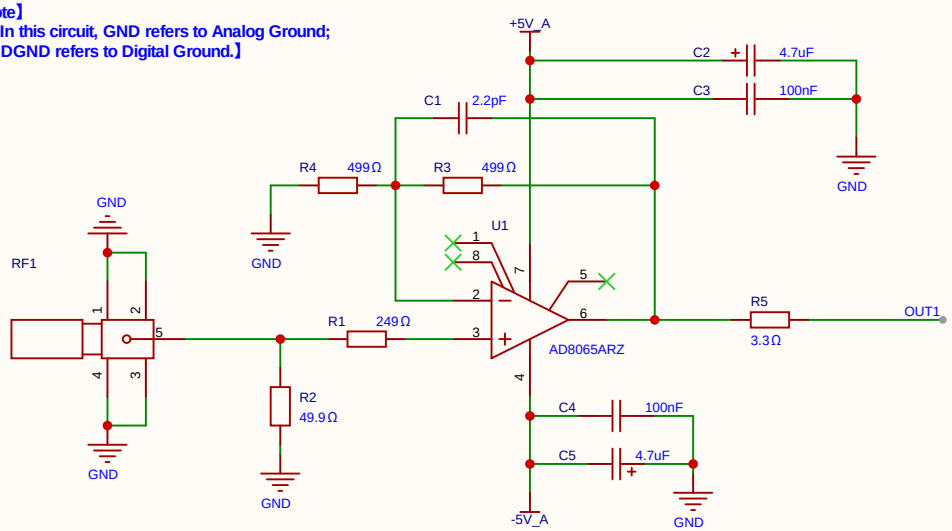
+5V_D ~ -5V_D(-5V_A)

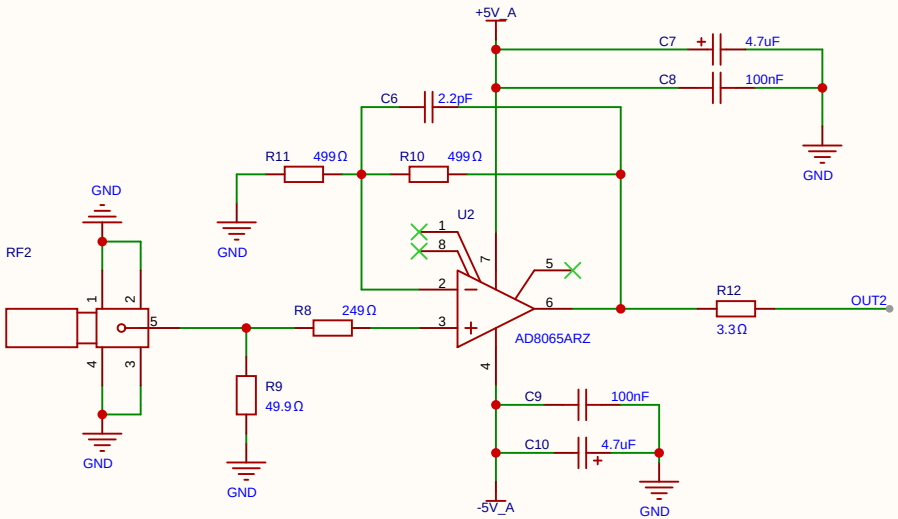


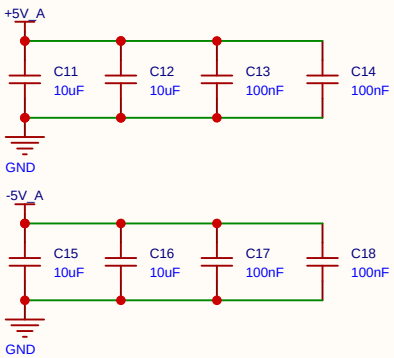
原理图	Schematic1	创建日期	2025-10-17
		更新日期	2026-02-05
板子	Board1	图页	POWER
绘制		100MSps_ADC采样板	
审阅			
		版本	尺寸
		V1.0	A4
		页 1 共 3	
嘉立创EDA		嘉立创EDA	

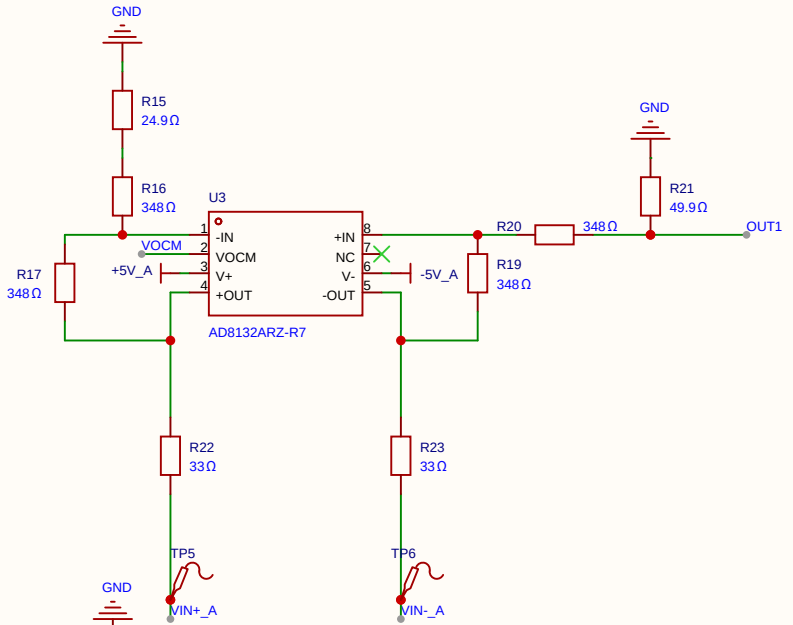
【Blue: Note】

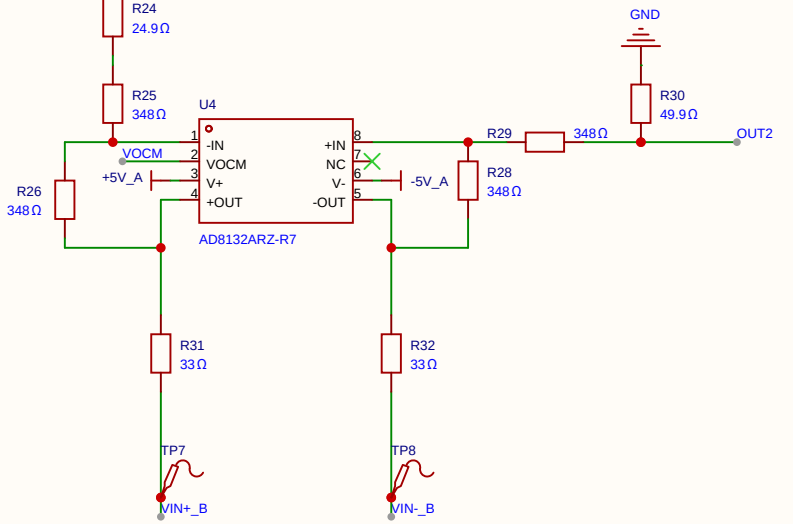
【Note】
【(1) In this circuit, GND refers to Analog Ground;
DGND refers to Digital Ground.】



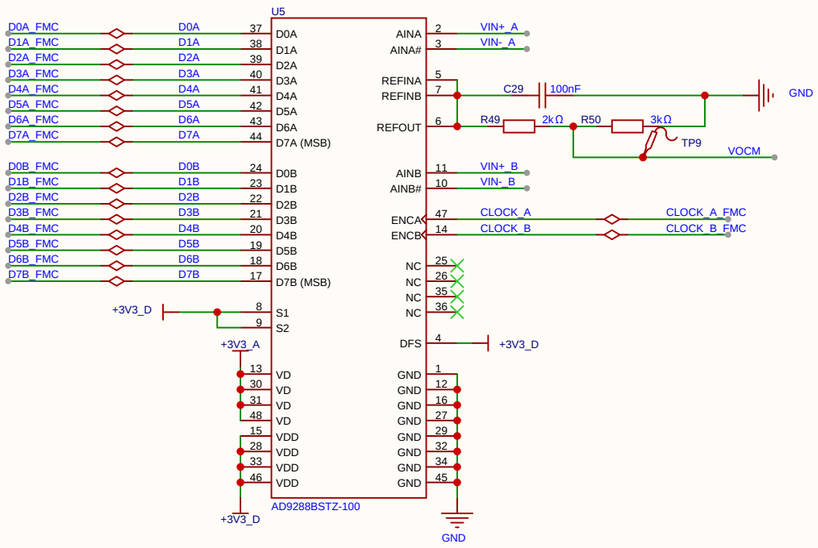


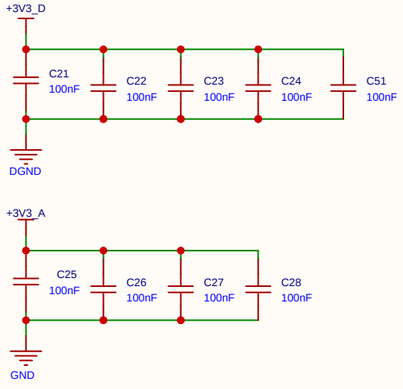


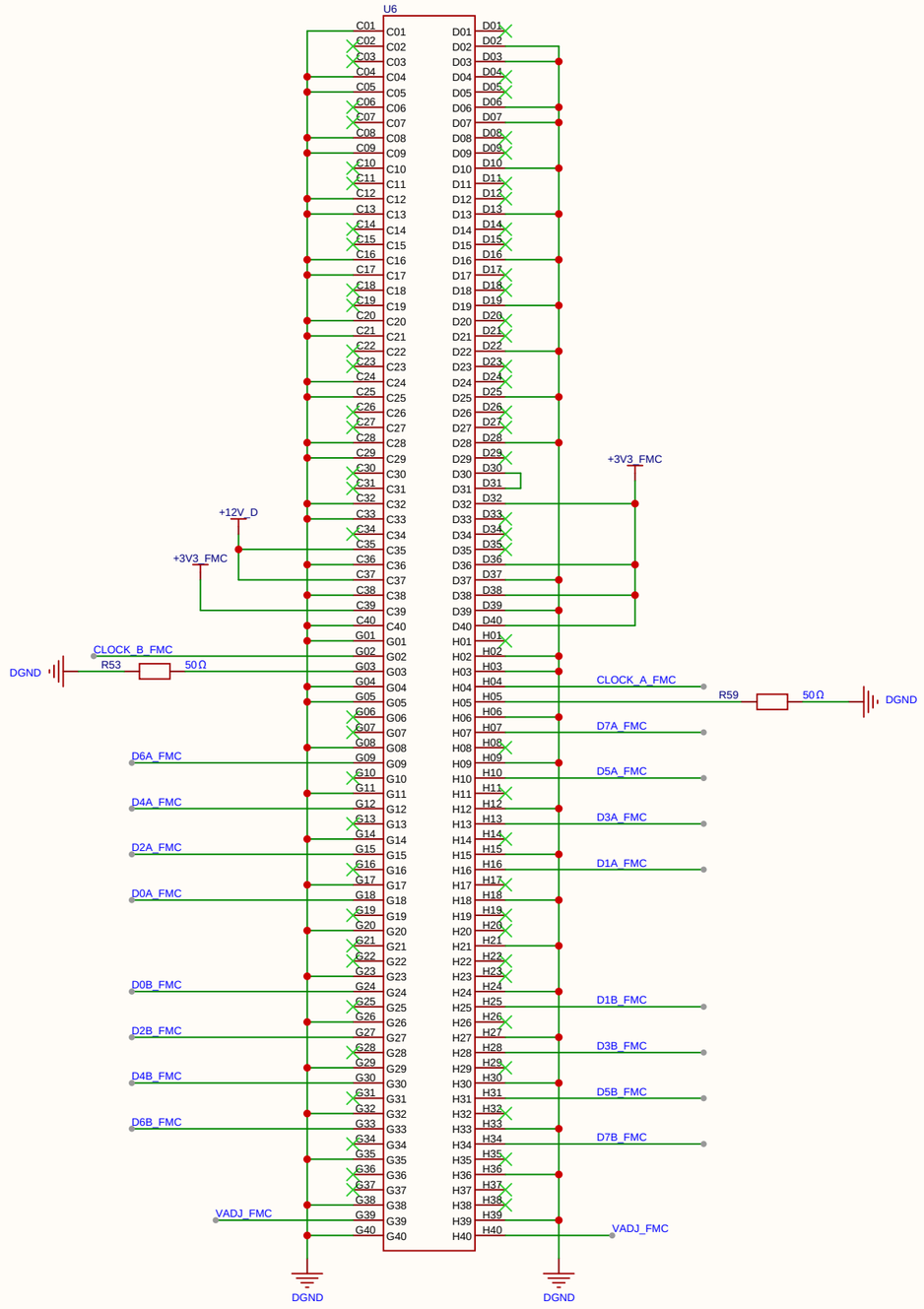




原理图	Schematic1	创建日期	2025-10-17
		更新日期	2026-02-05
板子	Board1	图页	ADC_Front-End
绘制		100MSps_ADC采样板	
审阅			
		版本	尺寸
嘉立创EDA		V1.0	A4
		页 2 共 3	
		嘉立创EDA	







原理图	Schematic1	创建日期	2025-10-17
		更新日期	2026-01-30
板子	Board1	图页	ADC+FMC
绘制		100MSps_ADC采样板	
审阅			
		版本	尺寸	页 3 共 3
嘉立创EDA		V1.0	A4	嘉立创EDA