

Siyuan Chai

CONTACT INFORMATION	siyuanc3@illinois.edu https://schai.me	
EDUCATION	University of Illinois , Urbana Champaign, IL Computer Science Ph.D. Start Aug. 2021 Advisor: Prof. Tianyin Xu Northwestern University , Evanston, IL M.S. Computer Science, B.S. Electrical Engineering Graduated June 2021 GPA: 4.0/4.0 (Summa Cum Laude)	
SKILLS	Programming languages: C/C++, Assembly, Python, Java, Go, JavaScript, MATLAB System-level Development: Unix/Linux, QEMU, Docker, GDB, Make, Linker, LLVM, OpenMP Artificial Intelligence: CUDA, PyTorch, Tensorflow, Keras, Image Processing, Computer Vision Hardware: Raspberry Pi, Arduino, VHDL, Verilog, 3D printing, SOLIDWORKS Web Development: HTML, CSS, Flask, Django, React	
RESEARCH EXPERIENCE	UIUC Xlab , Prof. Tianyin Xu Aug. 2021 to Present <i>Support Linux Kernel for Elastic Cuckoo Page Table</i> <ul style="list-style-type: none">Adapting Linux kernel, primarily the memory management portion, to support Elastic Cuckoo Page Table (ECPT), a hash page table that aims to replace paging by enabling memory-level parallelismExtensively modified memory translation portion of QEMU to simulate ECPT's hardware behaviorExploring the design space like page management, allocation and cache policy in linux running on ECPT NU Compilers Group , Prof. Simone Campanoni Jan. 2021 to July 2021 <i>Enhance Parallelism by Utilizing Commutative Loop iterations</i> <ul style="list-style-type: none">Coded a LLVM pass to tell the commutativity of <load, ALU operation, store> triplet across loop iterationsExtend the idea to develop tools for loop iteration commutativity for further utilization of parallelism NU Parallelism Group , Prof. Peter Dinda June 2020 to May 2021 <i>CARAT CAKE: Replacing Paging via Compiler/Kernel Cooperation</i> <ul style="list-style-type: none">Designed and implemented CARAT CAKE, an allocation level address space which aims to replace virtual memory and paging with protection checks inserted at compile time and allocations tracked in runtimeImplemented a competitive paging address space with support for red black tree and splay tree data structures to track VA-PA mapping, Transparent Huge Pages, and PCID; performance measured with Performance Monitoring CounterDesigned runtime protection check with address mapping data structures Image & Video Processing Lab , Prof. Aggelos Katsaggelos June 2019 to July 2021 <i>DeepCOVID-XR</i> <ul style="list-style-type: none">Designed and implemented a CNN model to flag out positive COVID cases based on patients' chest X-ray images	

	<ul style="list-style-type: none"> • Outperformed experienced radiologists with an accuracy of 85% compared to 76 - 82% and AUC of 0.935 compared to 0.819 - 0.856 	
PUBLICATIONS AND WORKING PAPERS	<ol style="list-style-type: none"> 1. Ramsey M Wehbe, Jiayue Sheng, Shinjan Dutta, Siyuan Chai, Amil Dravid, Semih Barutcu, Yunan Wu, Donald R. Cantrell, Nicholas Xiao, Hatice Savas, Rishi Agrawal, Nishant Parekh, Aggelos K. Katsaggelos. "Deepcovid-xr: An artificial intelligence algorithm to detect covid-19 on chest radiographs trained and tested on a large us clinical dataset." <i>Radiological Society of North America</i>. [Online]. Available: https://doi.org/10.1148/radiol.2020203511. 2. Brian Suchy, Souradip Ghosh, Aaron Nelson, Zhen Huang, Drew Kersnar, Siyuan Chai, Michael Cuevas, Gaurav Chaudhary, Alex Bernat, Nikos Hardavellas, Simone Campanoni, Peter Dinda. "CARAT CAKE: Replacing Paging via Compiler/Kernel Cooperation." <i>Submitted for ASPLOS 2022</i>. 	
WORK EXPERIENCE	Research Intern , Tencent Network Group <i>Service Driven Network Verification tool</i> <ul style="list-style-type: none"> • Contributed to design a scalable network verification that supports quantitative query and covers all data plane with global formal modeling and local simulation • Designed easy-to-use geo-based intent language for network verification 	June 2021 to Aug. 2021
PROJECTS	C-style Language Compiler , CS 322 Compiler Construction <ul style="list-style-type: none"> • Created, from scratch, a compiler to translate C-style language to x86_64 assembly • Implemented features including graph-coloring register allocation, liveness analysis, instruction selection with tiling, control flow graph, and memory access checking Middle End Analysis for a C-based API , CS 323 Code Analysis & Transformation <ul style="list-style-type: none"> • Coded a LLVM pass to reduce calls to a custom C-based API by implementing analysis like reaching-definition, constant propagation and folding, alias analysis for the specific API, function inlining, and dead code elimination 	
PROFESSIONAL ACTIVITIES	SOSP 2021 : Artifact Evaluation Committee, Slack Co-chair	
TEACHING EXPERIENCE	Peer Mentor (Undergraduate TA) - Northwestern University <ul style="list-style-type: none"> Spring 2021 CS 336 - Design & Analysis of Algorithms with Prof. Jason Hartline Winter 2021 CS 343 - Operating Systems with Prof. Peter Dinda Winter 2020 CS 336 - Design & Analysis of Algorithms with Prof. Konstantin Makarychev Fall 2019 CS 336 - Design & Analysis of Algorithms with Prof. Jason Hartline Spring 2019 CS 336 - Design & Analysis of Algorithms with Prof. Jason Hartline Teaching Assistant - Washington University in St. Louis <ul style="list-style-type: none"> Spring 2018 ESE 205 Introduction to Engineering Design with Prof. James Feher 	
AWARDS AND HONORS	Dean's List , all quarters ACM-ICPC, Mid-Central Regional, Top 20% VEX Robotics International Championship, Top 4 Alliance	2017 - 2021 2018 2016