COL215: Digital Logic and System Design

Special Laboratory Semester, AY 2021-22

Department of Computer Science & Engineering

Lab Assignment - 3

4-Digit 7-Segment Display

Learning Objective:

Learn how to use on-board clock and generate timing/refreshing signals.

Specification:

Design and implement a circuit that takes a 4-digit decimal/hexadecimal number from slide switches and displays it on seven segment displays of BASYS3 FPGA board. Use on-board clock and find valid range of refresh rates.

Details:

This assignment builds over Assignment 2, extending from a single digit display to a multi-digit display by introducing proper timing and refreshing signals. It requires addition of a 4:1 multiplexer and a timing circuit to the 7-segment decoder designed in Assignment 2. Each of the 4 inputs and the output of the multiplexer are 4 bits, representing a decimal or hexadecimal digit. The timing circuit has two roles – (a) it produces 2-bit select input for the multiplexer and (b) it produces signals for the anodes.