

COL215

Assignment-3

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1 Introduction

In lab we Design and implement a circuit that takes a 4-digit decimal/hexadecimal number from slide switches and displays it on seven segment displays of BASYS3 FPGA board. Use on-board clock and find valid range of refresh rates. For simulation and implementation of our VHDL code, we use viavdo software.

2 Steps Performed in this Assignment

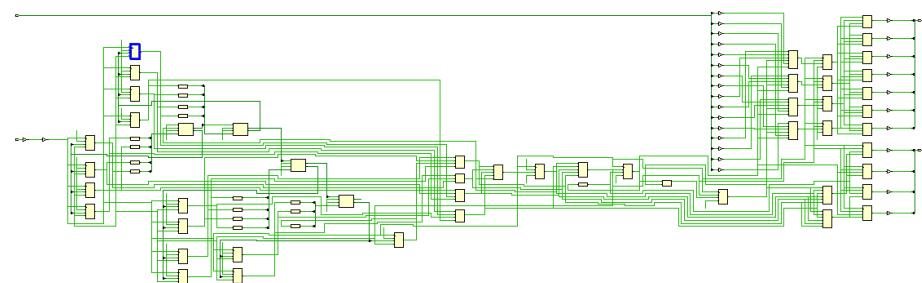
1. We create an entity for our inputs and outputs (here we are using 16 Buttons for the input and 4 7-segment for the output).
2. We create the truth table.
3. From the truth table, we create a k-map and find each output in terms of inputs.
4. In the architecture of our VHDL code, we make a process of a combinational circuit using the logical expressions for each output segment
5. In another process over clock, with every rising edge of the clock, we increment the counter till a fixed value and after that value, we change the counter to 0 and increment the anode counter and corresponding to a particular anode counter, we display a particular anode.
6. We run simulation on the code and checks the outputs.
7. Then we write the constraints file for our code.
8. After this we Synthesize and implement our project and generate a bitstream.
9. Finally, we download the bitstream in the FPGA board and check outputs for all possible values (0-9, and A-F) for all the anodes/7-segment displays.

3 Resources Utilization

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
-N a3		32	26	28	1

Primitives		
Ref Name	Used	Functional Category
FDRE	22	Flop & Latch
IBUF	17	IO
LUT1	16	LUT
OBUF	11	IO
LUT4	10	LUT
LUT6	6	LUT
FDSE	4	Flop & Latch
CARRY4	4	CarryLogic
LUT5	2	LUT
LUT3	1	LUT
LUT2	1	LUT
BUFG	1	Clock

4 Digital Circuit of the Code



5 Expressions Derivation Truth Table

B3	B2	B1	B0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

Use Karnaugh map for finding the boolean expression for the outputs.

K-Map

2)

		B ₂ B ₃	00	01	11	10
		B ₀ B ₁	00	0	0	1
		01	0	0	0	0
		11	0	1	0	0
		10	1	0	1	0

$$A = \bar{B}_0 \bar{B}_1 \bar{B}_2 \bar{B}_3 + B_0 B_1 \bar{B}_2 B_3 + \bar{B}_1 \bar{B}_2 \bar{B}_3 B_0 \\ + B_0 \bar{B}_1 B_2 B_3$$

3)

		B ₂ B ₃	00	01	11	10
		B ₀ B ₁	00	0	1	0
		01	0	0	1	1
		11	0	1	1	0
		10	0	0	0	1

$$B = B_0 B_1 B_3 + \bar{B}_0 B_1 B_2 + B_0 \bar{B}_1 B_2 \bar{B}_3 + \bar{B}_0 \bar{B}_1 B_2 B_3$$

3)

		B ₂ B ₃	00	01	11	10
		B ₀ B ₁	00	0	1	0
		01	1	0	1	0
		11	0	0	1	0
		10	0	0	0	0

$$C = \bar{B}_0 B_1 \bar{B}_2 \bar{B}_3 + \bar{B}_0 B_2 B_3 + B_1 B_2 B_3$$

$\stackrel{4}{\Leftrightarrow}$

$B_0 B_1$	$B_2 B_3$	00	01	11	10
00	0	0	0	1	
01	0	1	0	0	
11	0	0	1	1	
10	1	0	0	0	

$$D = B_0 B_1 B_2 + \bar{B}_0 \bar{B}_1 B_2 \bar{B}_3 + \bar{B}_0 B_1 \bar{B}_2 B_3 \neq B_0 \bar{B}_1 \bar{B}_2 \bar{B}_3$$

$\stackrel{5}{\Leftrightarrow}$

$B_0 B_1$	$B_2 B_3$	00	01	11	10
00	0	0	0	1	
01	0	0	0	0	
11	1	0	0	1	
10	1	1	0	1	

$$E = B_0 \bar{B}_3 + B_0 \bar{B}_1 \bar{B}_2 + \bar{B}_1 B_2 \bar{B}_3$$

$\stackrel{6}{\Leftrightarrow}$

$B_0 B_1$	$B_2 B_3$	00	01	11	10
00	0	0	0	0	
01	1	0	0	0	
11	1	0	0	1	
10	1	0	1	0	

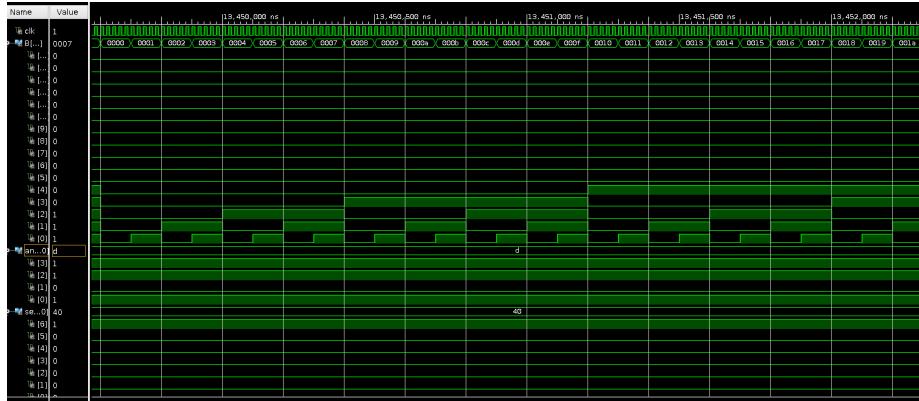
$$F = B_0 \bar{B}_1 B_2 B_3 + B_1 \bar{B}_2 \bar{B}_3 \\ + B_0 \bar{B}_2 \bar{B}_3 + B_0 B_1 \bar{B}_3$$

$\stackrel{7}{\Leftrightarrow}$

$B_0 B_1$	$B_2 B_3$	00	01	11	10
00	1	0	1	0	
01	0	0	0	0	
11	0	0	0	1	
10	1	0	0	0	

$$G_1 = \bar{B}_1 \bar{B}_2 \bar{B}_3 + \bar{B}_0 \bar{B}_1 B_2 B_3 + B_0 B_1 B_2 \bar{B}_3$$

6 Simulation of the Code



7 FPGA output

