

COL215

Assignment-7

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1 Introduction

In lab we design asynchronous serial receiver with band rate = 9600, 8 data bits, no parity bits and 1 stop bit. Connect this to the micro USB port of the BASYS 3 board. Use gtkterm on PC to test and demonstrate. For simulation and implementation of our VHDL code, we use vivado software.

2 Steps Performed in this Assignment

1. We create an entity for our inputs and outputs we define a clock and a vector for display the output in the seven segment.
2. From Assignment 5, we use the 4 digit-seven segment display code.
3. We define a process on clock that basically increase the counter on the rising edge.
4. after that we make a process over the clock_input that basically tells us about the which anode we need to glow(here we use only 2 rightmost anode).
5. In another process clk on rising edge we check if reset button is pressed or not if reset button is pressed than we set our seven segment output to 0 and otherwise we make cases for each state i.e idle,start,datashift,stop when will go to the next step and at which step and counter which we need to show the output on the seven segment display according the given input by the keyboard.
6. We run simulations on our code and check the outputs.
7. Then we write the constraints file for our code.
8. After this we Synthesize and implement our project and generate a bit-stream.

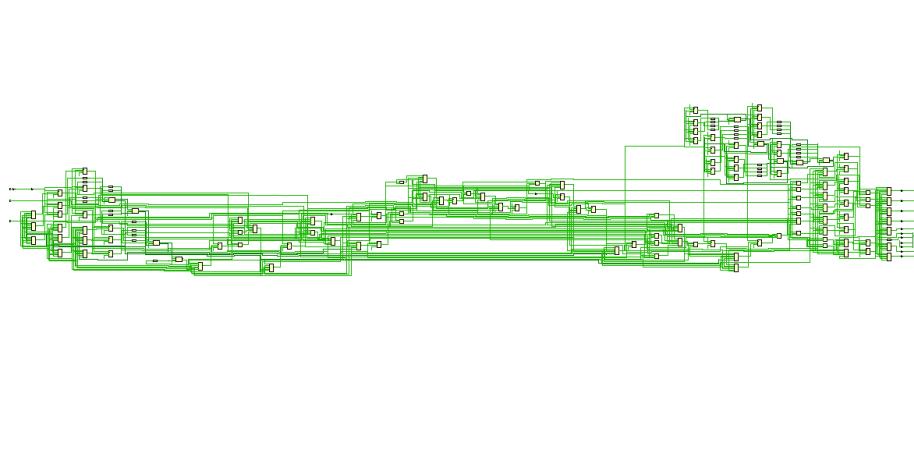
- Finally, we download the bitstream in the FPGA board and check outputs using the gtkterm by pressing the key on the keyboard.

3 Resources Utilization

The screenshot shows the Vivado Resource Utilization Report. The top section, "Hierarchy", displays a summary of resources for a specific component named "A7". The summary table has columns for Name, Slice LUTs (20800), Slice Registers (41600), Bonded IOB (106), and BUFGCTRL (32). The values are 93, 48, 14, and 1 respectively. Below this is a detailed table titled "Primitives" showing the usage of various primitives. The "Primitives" table has columns for Ref Name, Used, and Functional Category. The data is as follows:

Ref Name	Used	Functional Category
FDRE	48	Flop & Latch
LUT6	43	LUT
LUT1	34	LUT
LUT3	17	LUT
OBUF	11	IO
CARRY4	9	CarryLogic
LUT4	7	LUT
IBUF	3	IO
LUT5	2	LUT
LUT2	1	LUT
BUFG	1	Clock

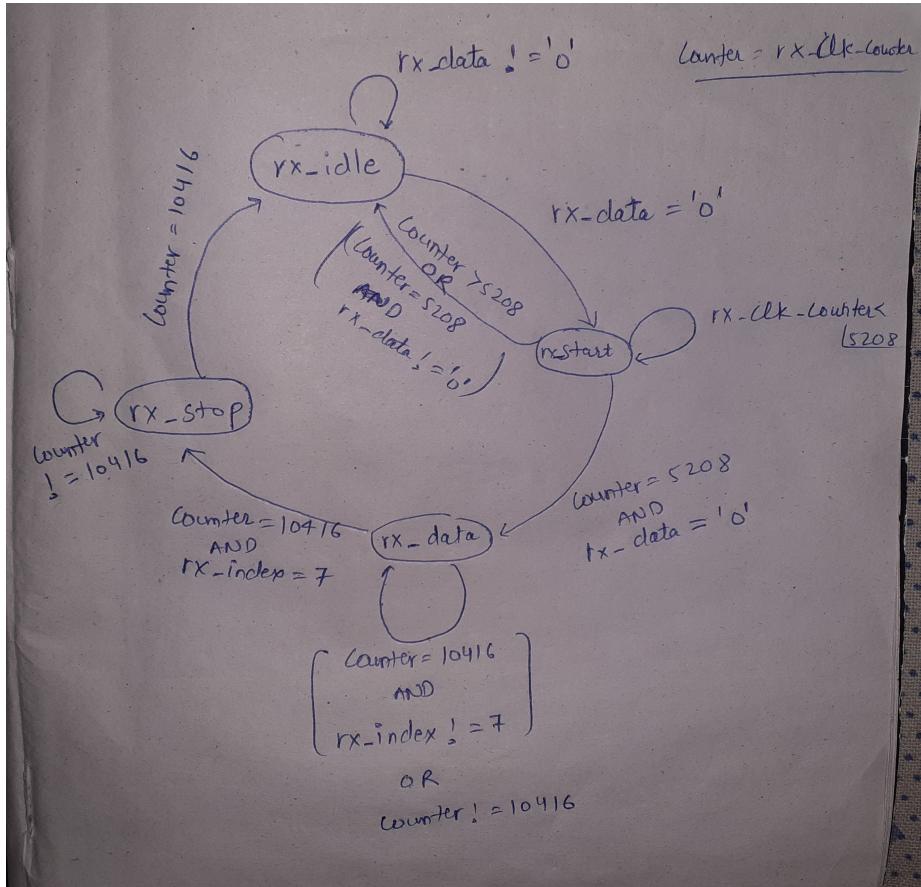
4 Digital Circuit of the Code



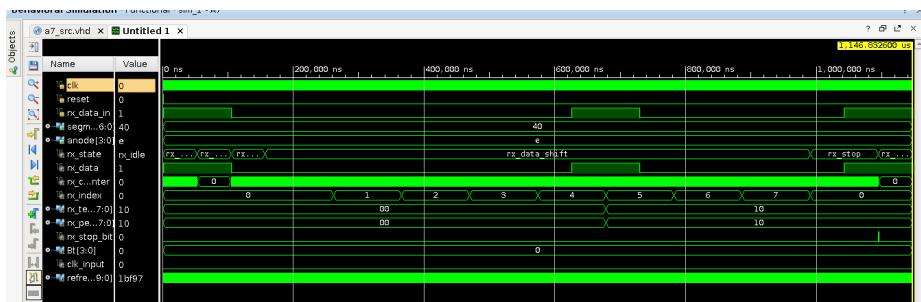
5 Expressions Derivation Truth Table

B3	B2	B1	B0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

6 FSM Diagram



7 Simulation of the Code



8 FPGA OUTPUT

