

COL215

Assignment-8

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1 Introduction

In lab we Design asynchronous serial transmitter to create a loop with the receiver with band rate = 9600, 8 data bits, no parity bits and 1 stop bit. Connect this to the micro USB port of the BASYS 3 board. Use gtkterm on PC to test and demonstrate. For simulation and implementation of our VHDL code, we use vivado software.

2 Steps Performed in this Assignment

1. We create an entity for our inputs and outputs we define a clock and a vector for display the output in the seven segment.
2. From Assignment 5, we use the 4 digit-seven segment display code.
3. We define a process on clock that basically increase the counter on the rising edge.
4. after that we make a process over the clock_input that basically tells us about the which anode we need to glow(here we use only 2 rightmost anode).
5. In another process clk on rising edge we make cases for each state i.e start ,idle,stop when will go to the next step and at which step and counter which we need to show the output on the seven segment display according the given input by the keyboard i.e the receiver part of the code.
6. In another process clk on rising edge we make cases for each state i.e idle,start,datashift,stop when will go to the next step and at which step and counter which we need to show the output on the seven segment display according the given input by the keyboard i.e the transmitter part of the code.

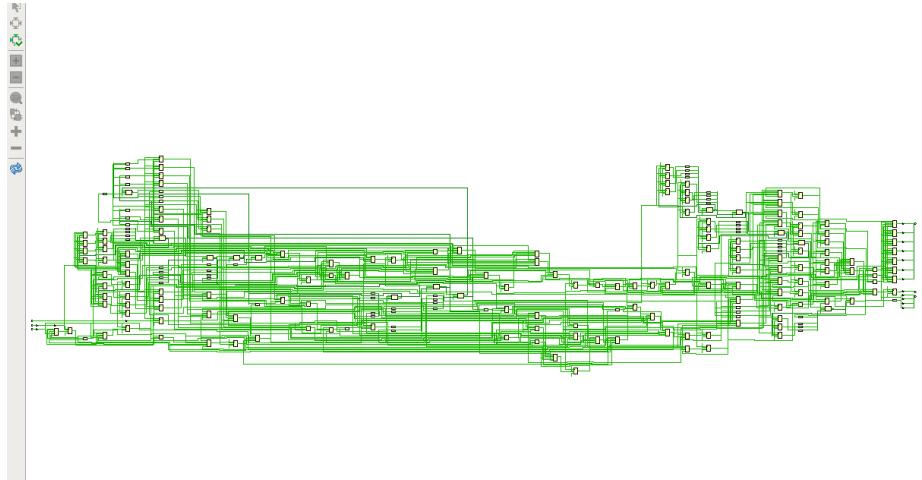
7. We run simulations on our code and check the outputs.
8. Then we write the constraints file for our code.
9. After this we Synthesize and implement our project and generate a bitstream.
10. Finally, we download the bitstream in the FPGA board and check outputs using the gtkterm by pressing the key on the keyboard.

3 Resources Utilization

Hierarchy					
	Name	1	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)
– A8		125	77	15	1

Primitives		
Ref Name	Used	Functional Category
FDRE	77	Flop & Latch
LUT1	47	LUT
LUT6	36	LUT
LUT5	25	LUT
LUT2	18	LUT
CARRY4	13	CarryLogic
OBUF	12	IO
LUT3	8	LUT
LUT4	7	LUT
IBUF	3	IO
BUFG	1	Clock

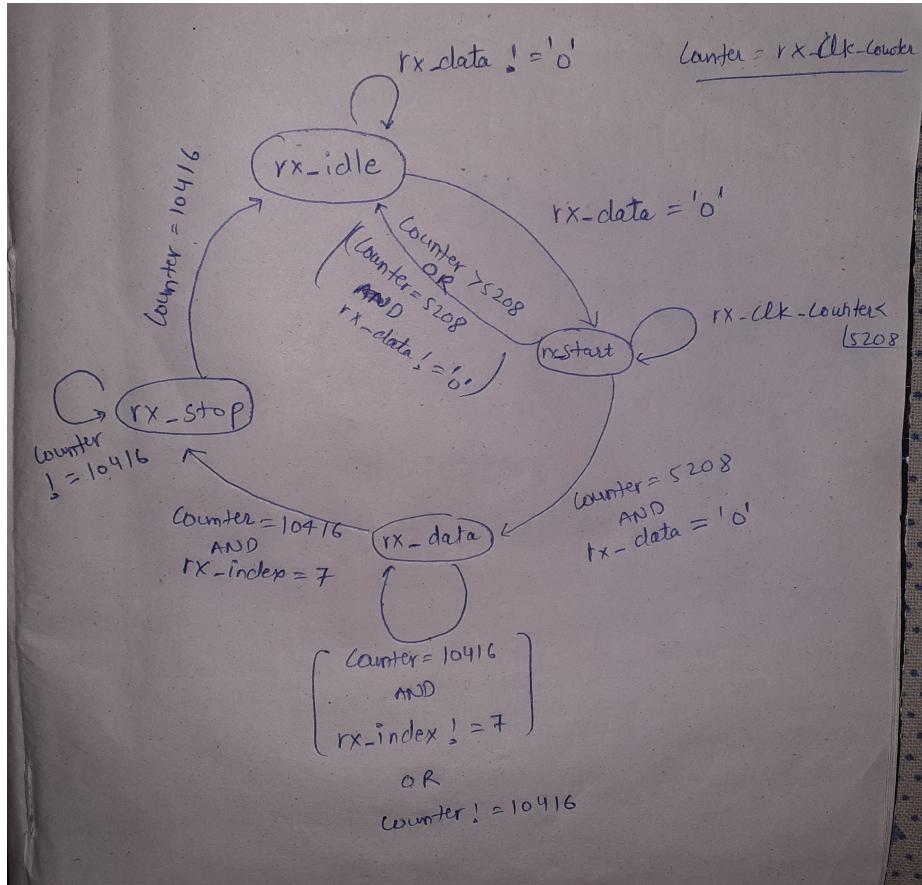
4 Digital Circuit of the Code



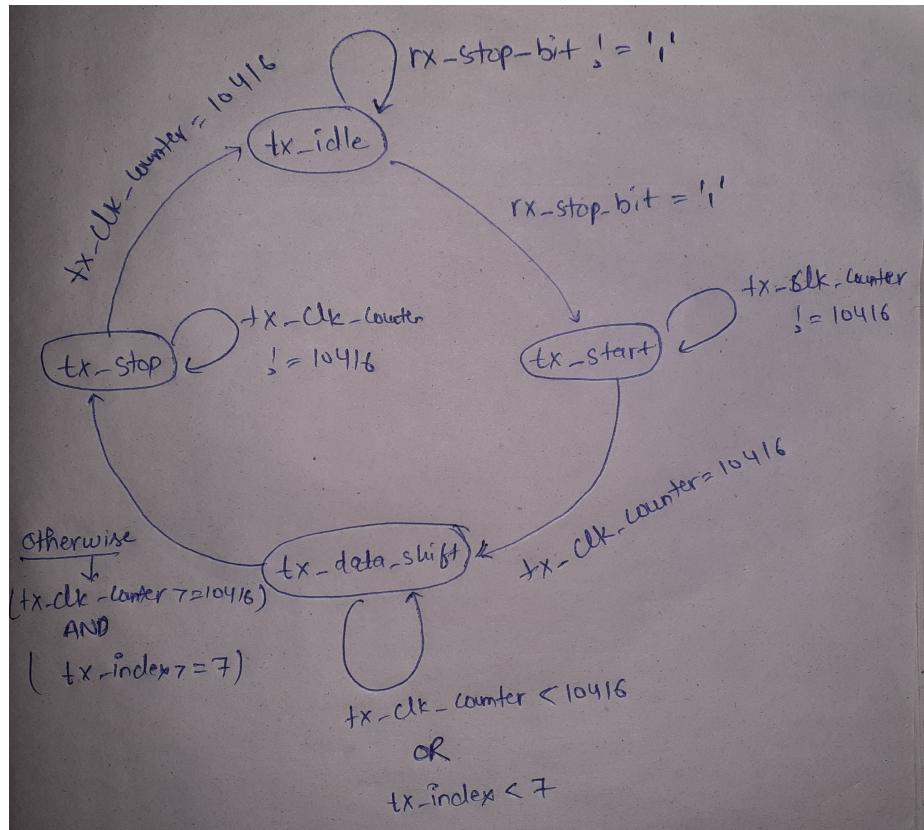
5 Expressions Derivation Truth Table

B3	B2	B1	B0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

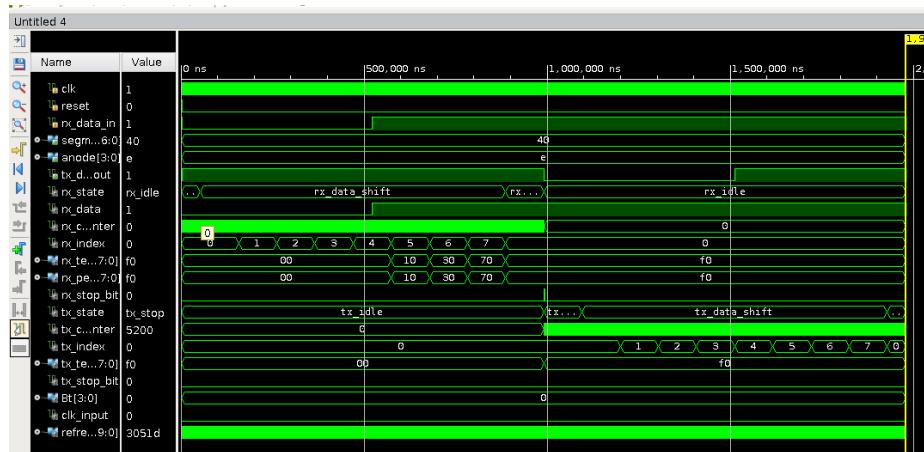
6 FSM Diagram reciever



7 FSM Diagram transmitter



8 Simulation of the Code



9 FPGA OUTPUT

