

# COL215

## Assignment-4

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### 1 Introduction

In lab we design a circuit that controls brightness of 7-segment LED displays using pulse width modulation. For simulation and implementation of our VHDL code, we use viavdo software.

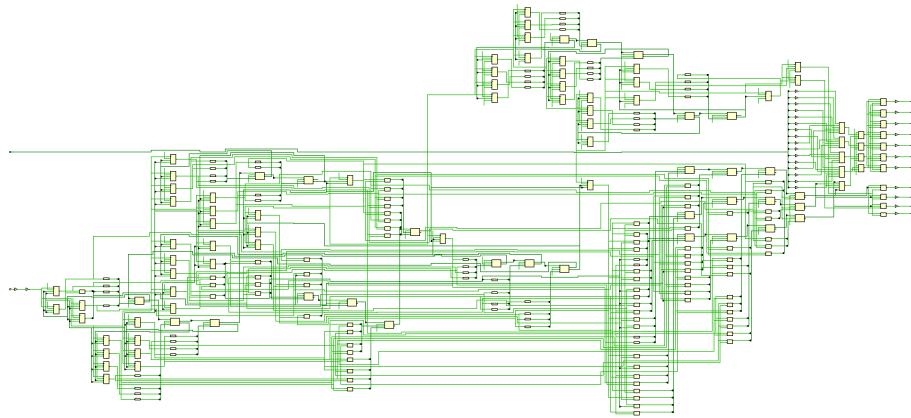
### 2 Steps Performed in this Assignment

1. We create an entity for our inputs and outputs (here we are using 16 Buttons for the input and 4 7-segments for the output).
2. From Assignment 3, we use the 4 digit-seven segment display code.
3. We define a process over clock, with every rising edge of the clock, we increment the counter till a fixed value and after that value, we change the counter to 0 and this process also takes the first two bits of the refresh clock as anode selector.
4. In another process over clk input (anode selector), we select the anode in decreasing order of the counter (refresh rate) i.e. the left most seven segment, which is supposed to be the brightest is on for all counter value. while the following segments are on till counter reaches 4000, 2000, 1000 respectively.
5. We run simulations on our code and check the outputs.
6. Then we write the constraints file for our code.
7. After this we Synthesize and implement our project and generate a bitstream.
8. Finally, we download the bitstream in the FPGA board and check outputs for all possible values (0-9, and A-F) for all the anodes/7-segment displays and also check the brightness of all the displays which decreases from left to right.

### 3 Resources Utilization

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)	
-N a4		122	58	28	1	
Primitives						
Ref Name	Used	Functional Category				
LUT2	80	LUT				
LUT1	56	LUT				
FDRE	54	Flop & Latch				
CARRY4	29	CarryLogic				
IBUF	17	IO				
OBUF	11	IO				
LUT4	7	LUT				
LUT6	4	LUT				
LDCE	4	Flop & Latch				
LUT3	3	LUT				
LUT5	1	LUT				
BUFG	1	Clock				

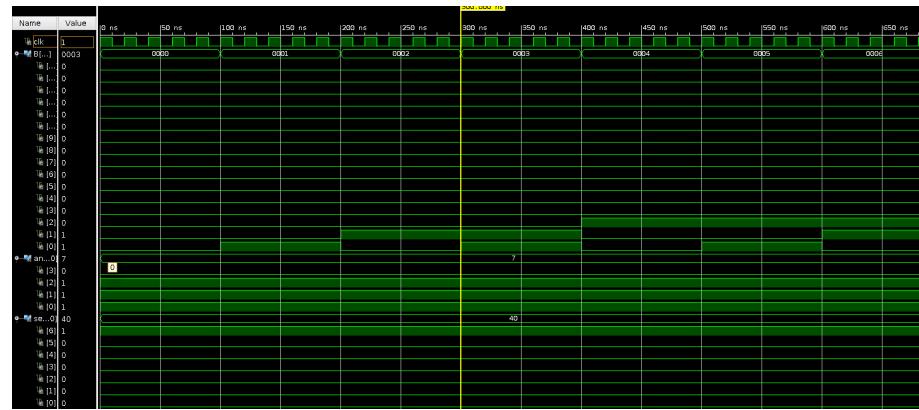
## 4 Digital Circuit of the Code



## 5 Expressions Derivation Truth Table

B3	B2	B1	B0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

## 6 Simulation of the Code



## 7 FPGA output

