COL215
Assignment-5

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1 Introduction

In lab we design that there are two push buttons which are used to enter the data set on the slide switches. When button-1 is pressed, 4 digits set on 16 slide switches are entered. When button-2 is pressed, four 2-bit brightness values set on rightmost 8 slide switches are entered. The digits scroll on the display from right to left in a cyclic manner, at a fixed rate. Four brightness levels specified are associated with the four digits. For simulation and implementation of our VHDL code, we use vivado software.

2 Steps Performed in this Assignment

1. We create an entity for our inputs and outputs (here we are using 16 Buttons for the input the digits and using 2 push down button for controlling the brightness and the digits to show on the 4 7-segments for the output).

2. We define a process for controlling the push down button that is if centre button is pressed than we need to show the digits pressed and if upper push down button is pressed than we need to show the brightness and for controlling the brightness we use the last 8 buttons.

3. From Assignment 4, we use the 4 digit-seven segment display code.

4. after that we make a process over the clock for rotating the numbers in this we just do basic thing that after some fixed interval the digit with segment1 shift to segment 2 and so on.

5. In another process over anode signal we just define the brightness control and for this we take that for low brightness we show it as 6250 and for 2nd brighter we show is 12500 and 3rd we use 50000 and 4th brighter we use 100000 and also map the brightness with the digit so that when digit is rotating the brightness is also rotating.

6. We run simulations on our code and check the outputs.
7. Then we write the constraints file for our code.
8. After this we Synthesize and implement our project and generate a bitstream.
9. Finally, we download the bitstream in the FPGA board and check outputs for both the push down buttons and also check the brightness control.

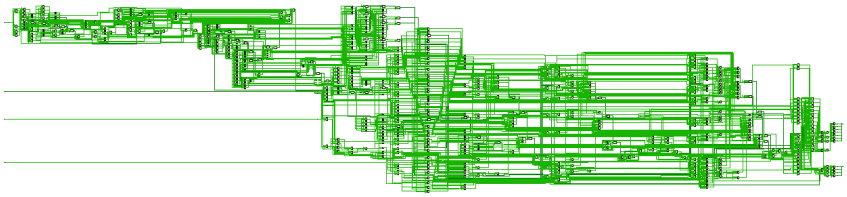
3 Resources Utilization

Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
a5_main	344	214	30	1

Primitives

Ref Name	Used	Functional Category
FDRE	124	Flop & Latch
LUT5	101	LUT
LUT1	97	LUT
LDCE	90	Flop & Latch
LUT3	58	LUT
CARRY4	52	CarryLogic
LUT6	50	LUT
LUT2	32	LUT
LUT4	24	LUT
IBUF	19	IO
OBUF	11	IO
BUFG	1	Clock

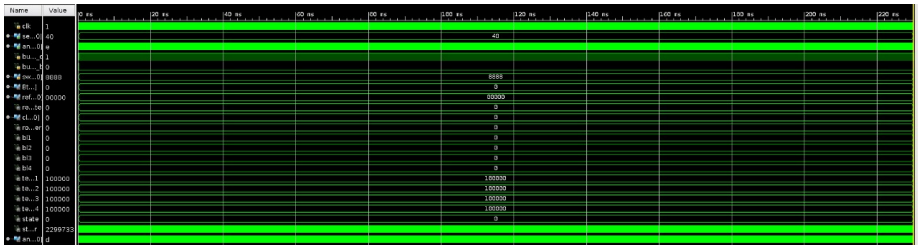
4 Digital Circuit of the Code



5 Expressions Derivation Truth Table

B3	B2	B1	B0	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

6 Simulation of the Code



7 FPGA OUTPUT