# COL215
# Assignment-2

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April 2022

## 1 Introduction

In lab we design a combination circuit that takes a decimal/hexadecimal digit encoded using 4 bits and produces 7-bit output for seven segment displays of BASYS3 FPGA board. For simulation and implementation of our VHDL code, we use viavdo software.

## 2 Steps Performed in this Assignment

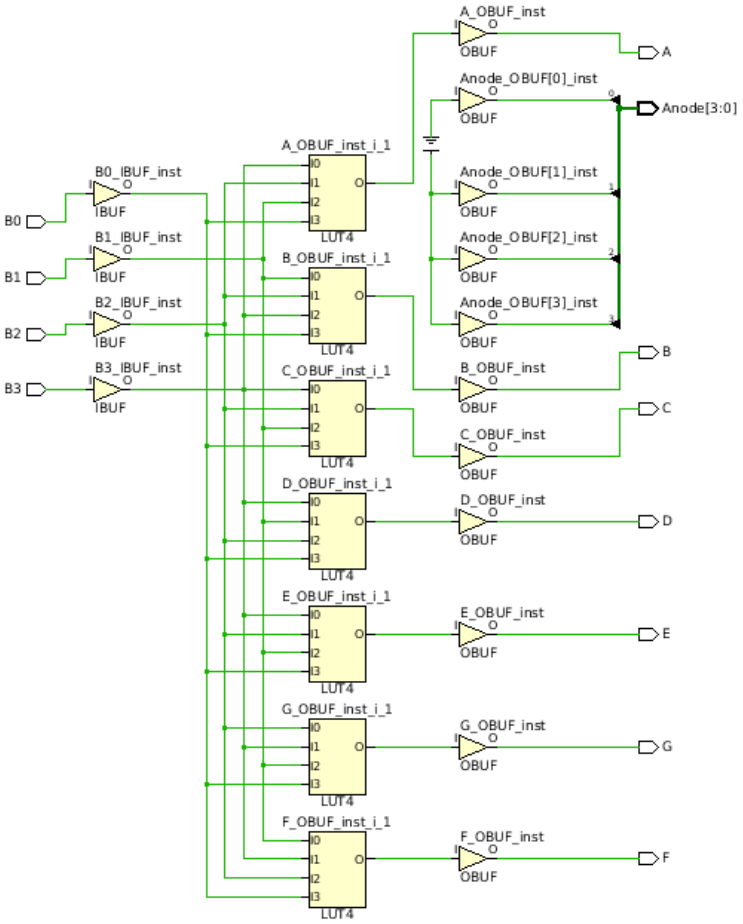
1. We create an entity for our inputs and outputs (here we are using 4 Buttons for the input and 7 segment for the output).
2. We crate the truth table.
3. From the truth table, we create a k-map and find each output in terms of inputs.
4. Then we write the architecture of our VHDL code and run simulations and check the outputs.
5. Then we write the constraints file for our code.
6. After this we Synthesize and implement our project and generate a bitstream.
7. Finally, we download the bitstream in the FPGA board and check outputs for all possible values (0-9, and A-F).

# 3 Resources Utilization

| Resource | Count |
|---|---|
| LUT Memory | 0 |
| LUT logic | 4 |
| DSP | 0 |
| Flip Flops | 0 |
| BRAM | 0 |

| Cell | Count |
|---|---|
| LUT4 | 7 |
| IBUF | 4 |
| OBUF | 11 |

# 4 Digital Circuit for 7 segment Display



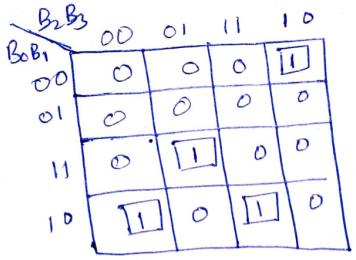
## 5 Expressions Derivation Truth Table

| B3 | B2 | B1 | B0 | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

Use Karnaugh map for finding the boolean expression for the outputs.

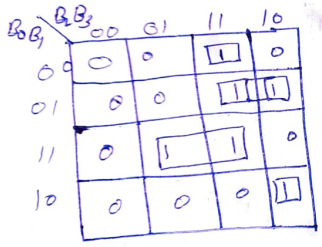
K - Map

1)



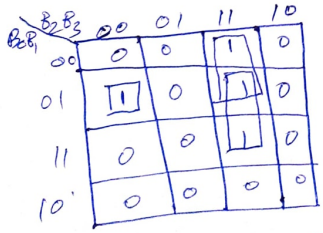

$A = \bar{B_0}\,\bar{B_1}\,B_2\,\bar{B_3} + B_0\,B_1\,\bar{B_2}\,B_3 + \bar{B_1}\,\bar{B_2}\,\bar{B_3}\,B_0 + B_0\,\bar{B_1}\,B_2\,B_3$

2)



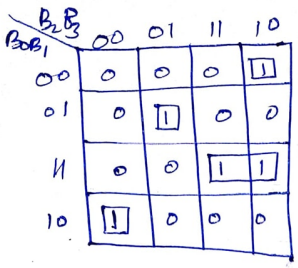

$B = B_0\,B_1\,B_3 + \bar{B_0}\,B_1\,B_2 + B_0\,\bar{B_1}\,B_2\,\bar{B_3} + \bar{B_0}\,\bar{B_1}\,B_2\,B_3$

3)



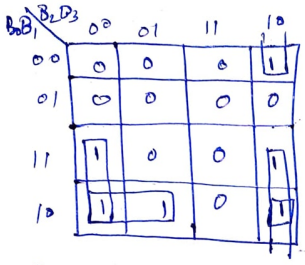

$C = \bar{B_0}\,B_1\,\bar{B_2}\,\bar{B_3} + \bar{B_0}\,B_2\,B_3 + B_1\,B_2\,B_3$

4)



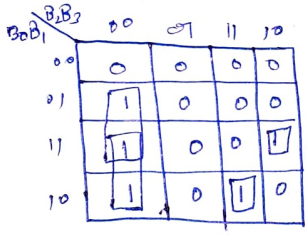

$$D = B_0 B_1 B_2 + \bar{B_0} \bar{B_1} B_2 \bar{B_3} + \bar{B_0} B_1 \bar{B_2} B_3 + B_0 \bar{B_1} \bar{B_2} \bar{B_3}$$

5)



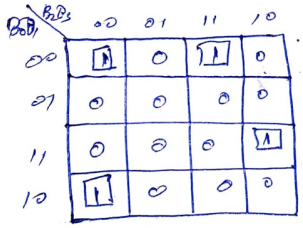

$$E = B_0 \bar{B_3} + B_0 \bar{B_1} \bar{B_2} + \bar{B_1} B_2 \bar{B_3}$$

6)



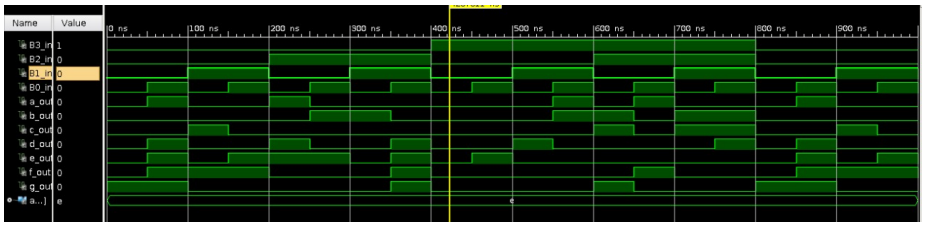

$$F = B_0 \bar{B_1} B_2 B_3 + B_1 \bar{B_2} \bar{B_3} + B_0 \bar{B_2} \bar{B_3} + B_0 B_1 \bar{B_3}$$

7)

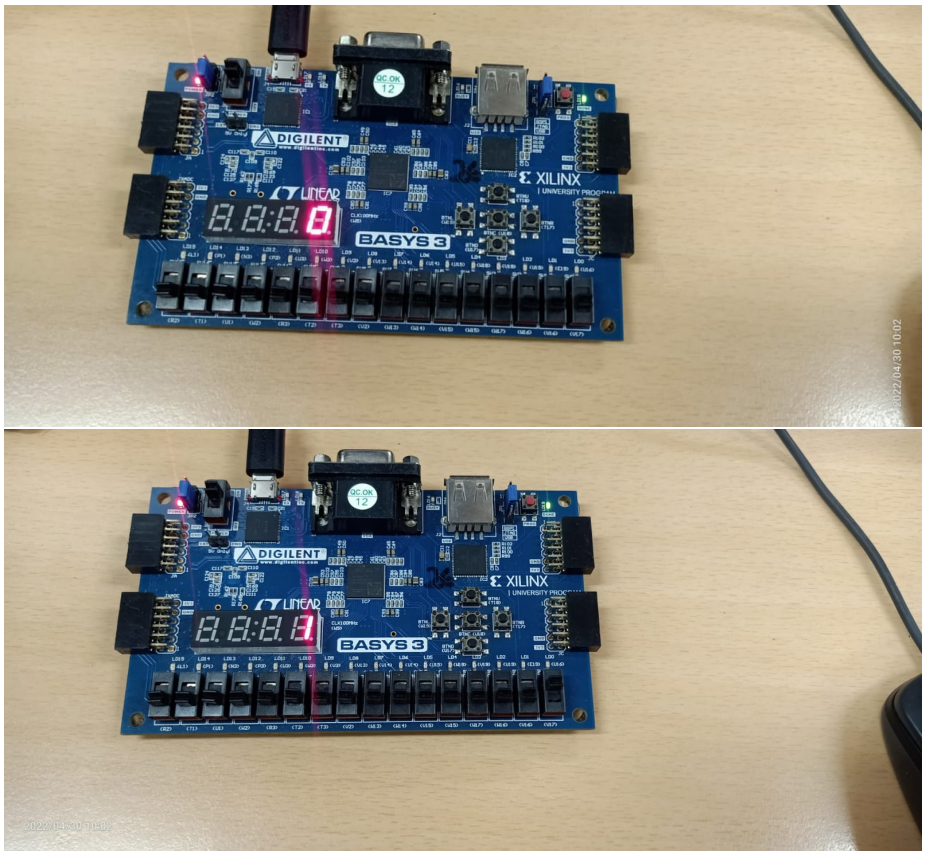


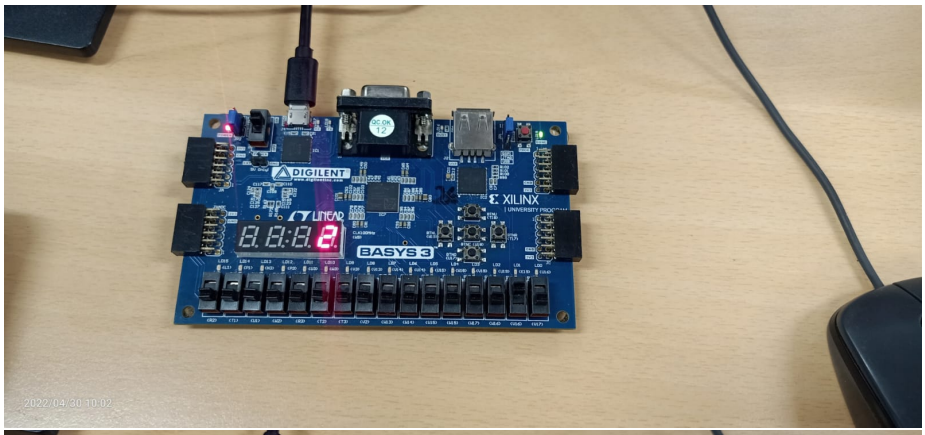

$$G_1 = \bar{B_1} \bar{B_2} \bar{B_3} + \bar{B_0} \bar{B_1} B_2 B_3 + B_0 B_1 B_2 \bar{B_3}$$

# 6 Simulation of 7 segment Display




# 7 FPGA output

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BASYS 3
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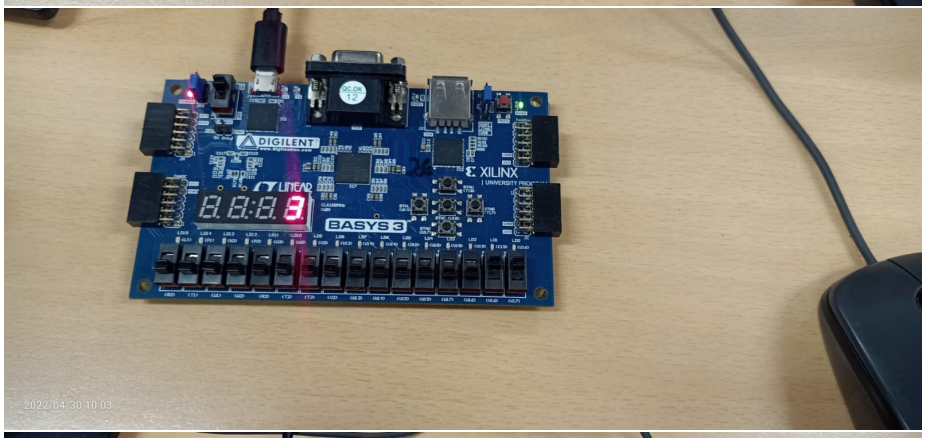
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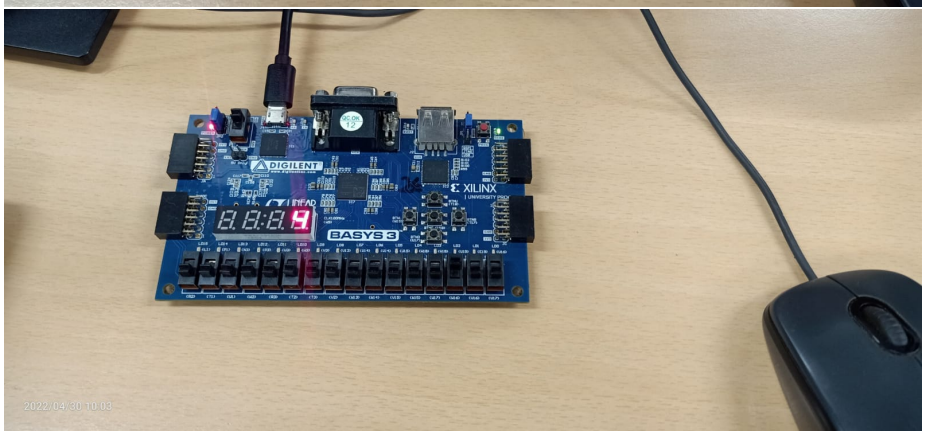
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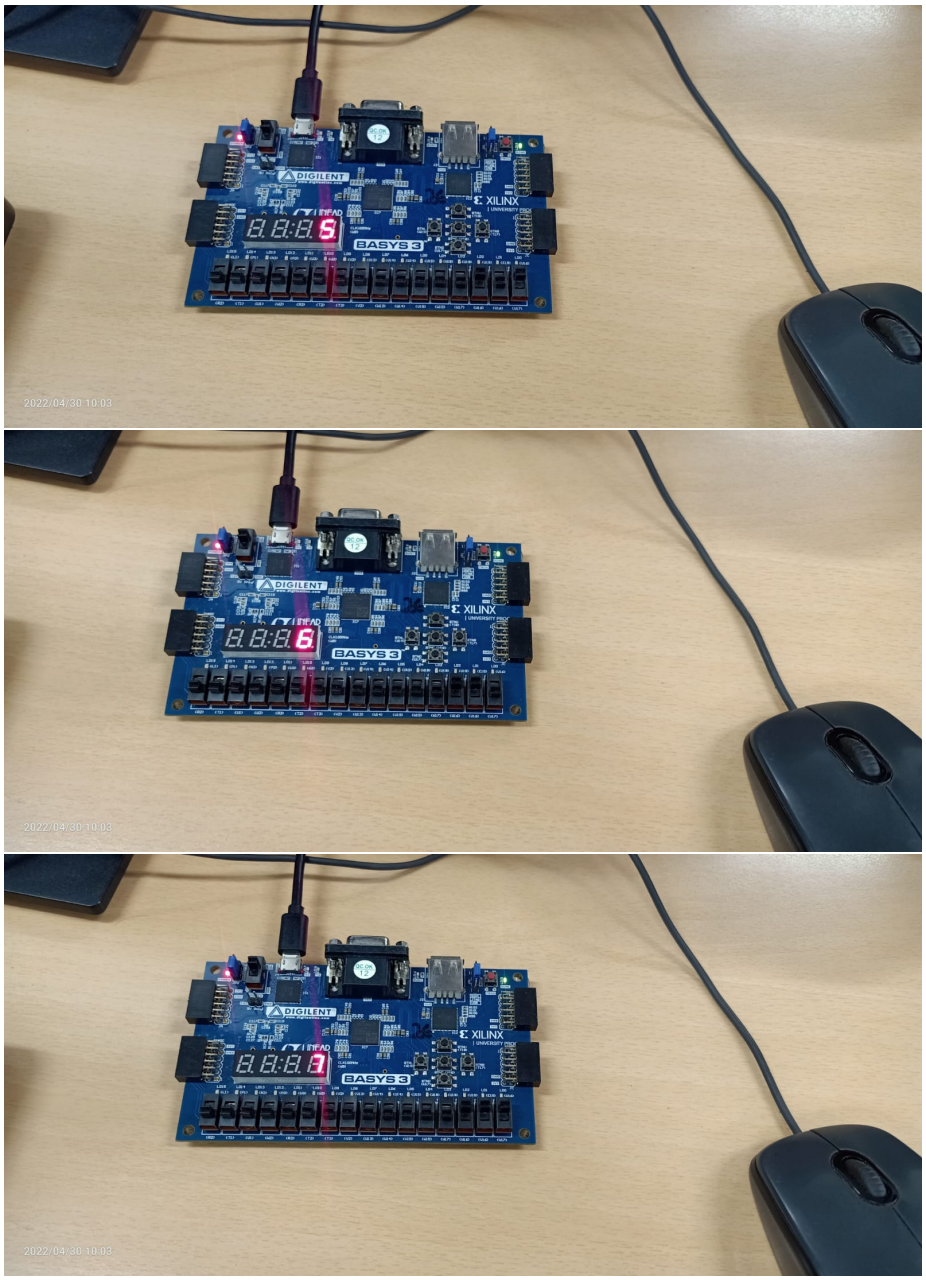
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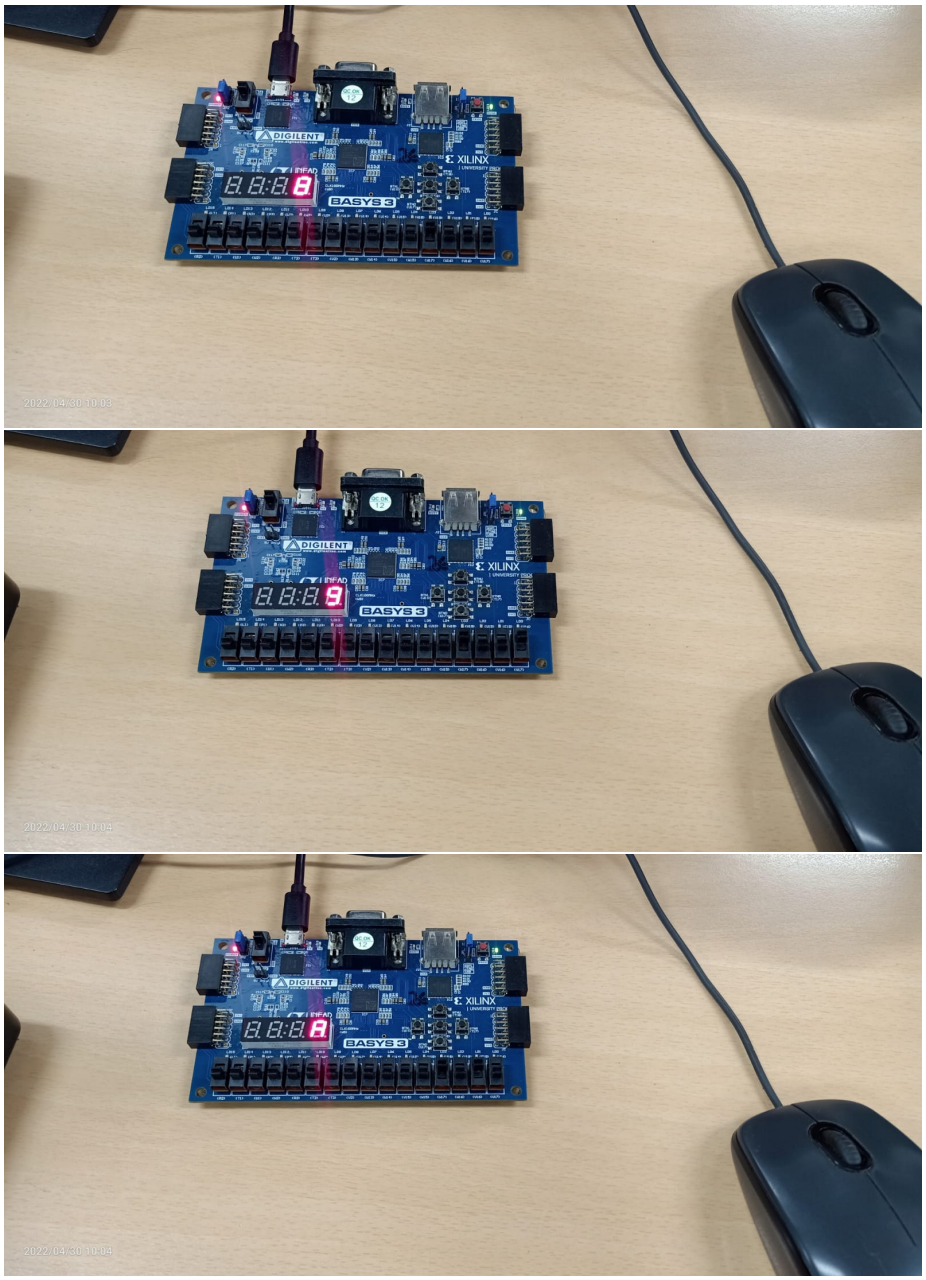
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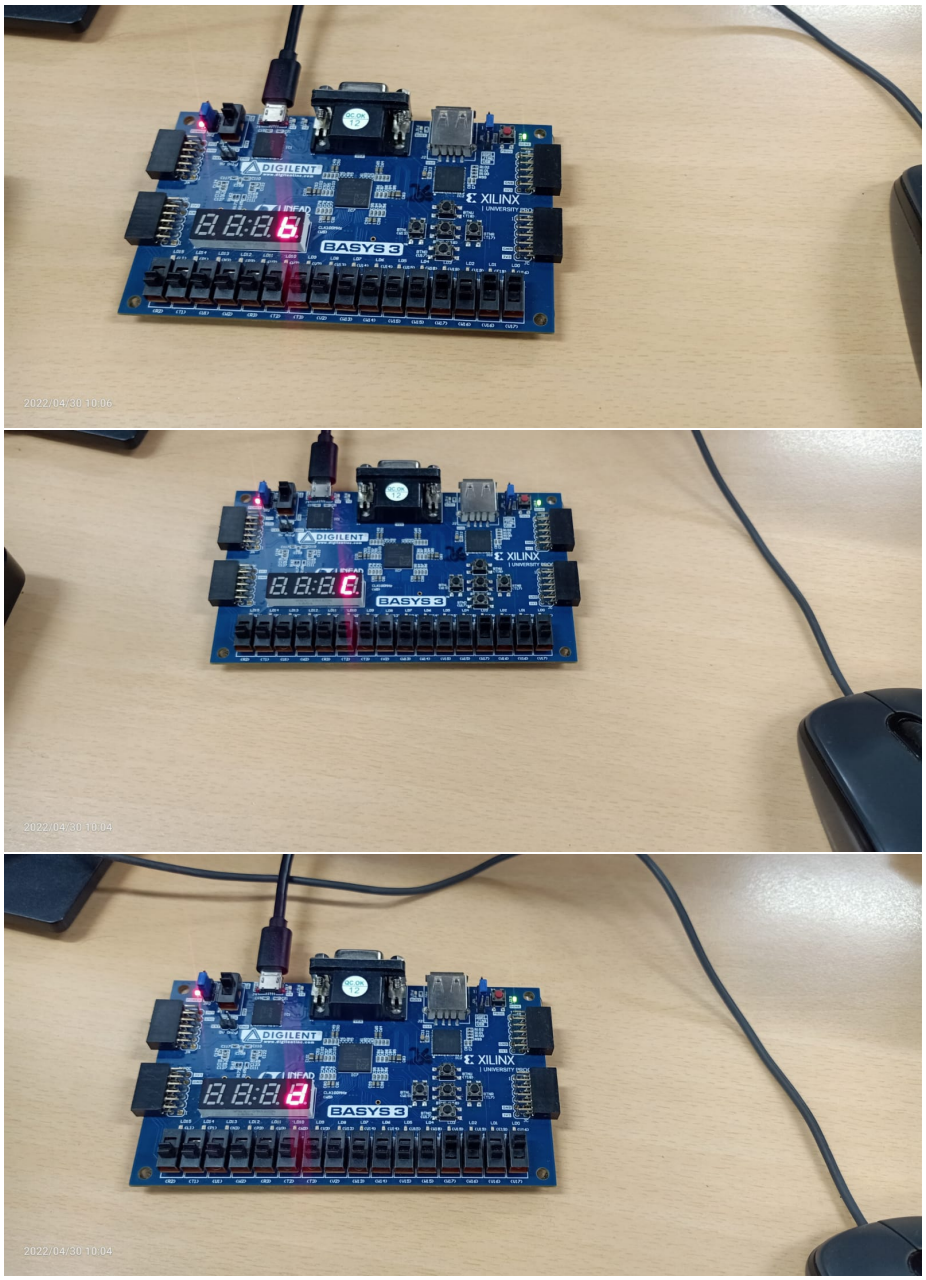
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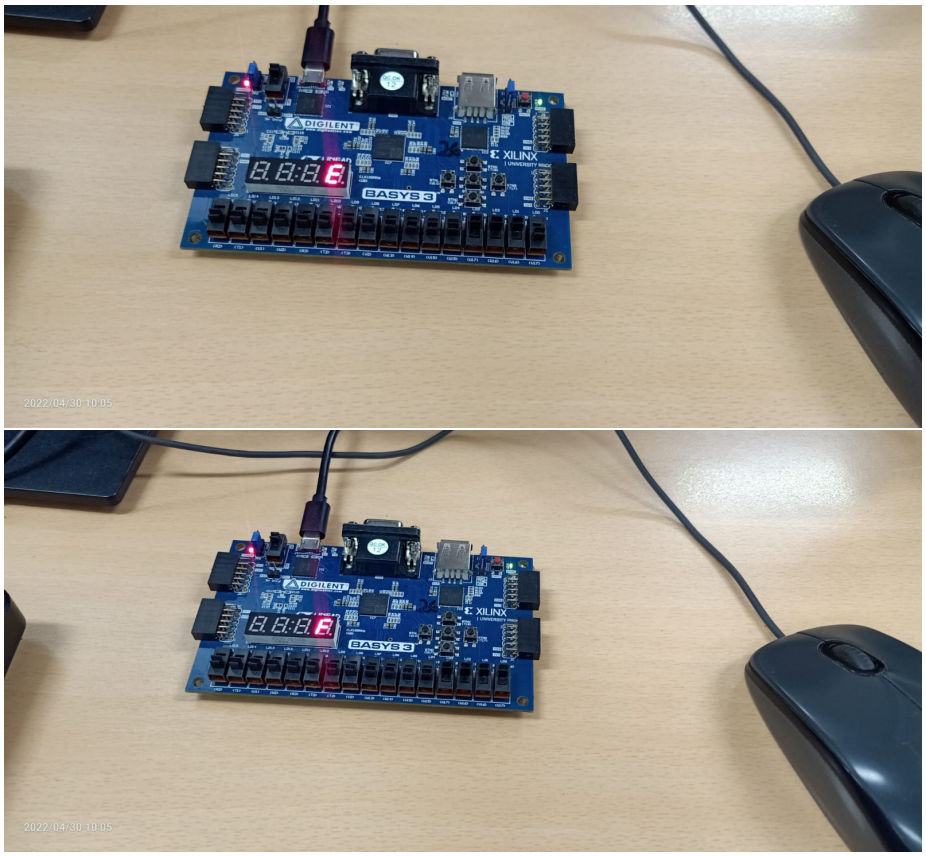
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