COL215
Assignment-6

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May 2022

1 Introduction

In lab we design a stopwatch and implement it on BASYS 3 board, using its 7-segment display and push buttons. Since the display has only 4 digits, assign these as follows -1 digit for minutes, two digits for seconds and one digit for tenths of a second. Use three push buttons as follows.

1. Start/Continue
2. Pause
3. Reset

For simulation and implementation of our VHDL code, we use viavdo software.

2 Steps Performed in this Assignment

1. We create an entity for our inputs and outputs (here we are using 3 push buttons as input and 4 7-segments for the output).
2. From previous Assignments, we use the 4 digit-seven segment display code.
3. We define a process over clock, with every rising edge of the clock, The design will be centered around an ensemble of four counters described below.
   (a) A modulo 10 counter to count tenths of a second
   (b) A modulo 10 counter to count unit digits of seconds
   (c) A modulo 6 counter to count tens of seconds
   (d) A modulo 10 counter to count minutes

The ensemble is driven by a 10 Hz timing reference. Provide for an enable input and a reset input. The enable input comes from a flip-flop/latch that is set to '1' when Start/Continue button is pressed and set to '0' when Pause button is pressed. Reset input comes from a push button. The counters can be synchronous or asynchronous. In asynchronous counters, various bits may not change simultaneously, but the time delays will not be perceptible to the eye.

4. In another process over clk input (anode selector) ans showing the minutes in leftmost segment and the next 2 segments shows the second and rightmost segment shows the milliseconds of the stop watch.

5. We make a process that controls the push buttons basically we handle the cases when push button is pressed is for stop reset and the start/continue and work according to the buttons.

6. We run simulations on our code and check the outputs.

7. Then we write the constraints file for our code.

8. After this we Synthesize and implement our project and generate a bitstream.

9. Finally, we download the bitstream in the FPGA board and check outputs that the stopwatch is working fine for all the anodes/7-segment and also ensure with the mobile stopwatch.

3 Resources Utilization

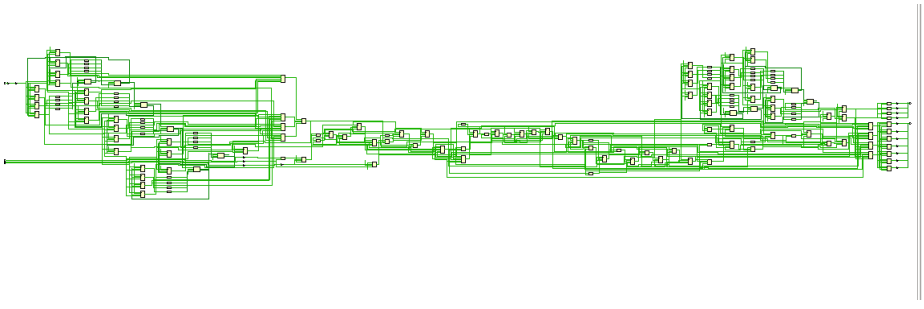
Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
a6_main	82	64	15	2

Primitives

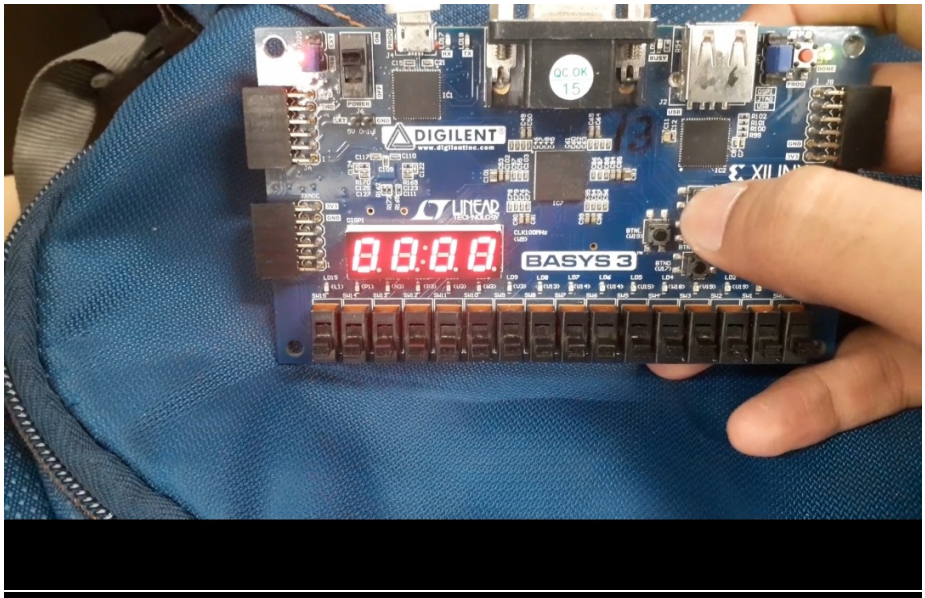
Ref Name	Used	Functional Category
FDRE	61	Flop & Latch
LUT1	48	LUT
LUT4	15	LUT
LUT6	12	LUT
LUT2	12	LUT
OBUF	11	IO
CARRY4	11	CarryLogic
LUT3	7	LUT
IBUF	4	IO
BUFG	2	Clock
LUT5	1	LUT
LDPE	1	Flop & Latch
LDCE	1	Flop & Latch
FDSE	1	Flop & Latch

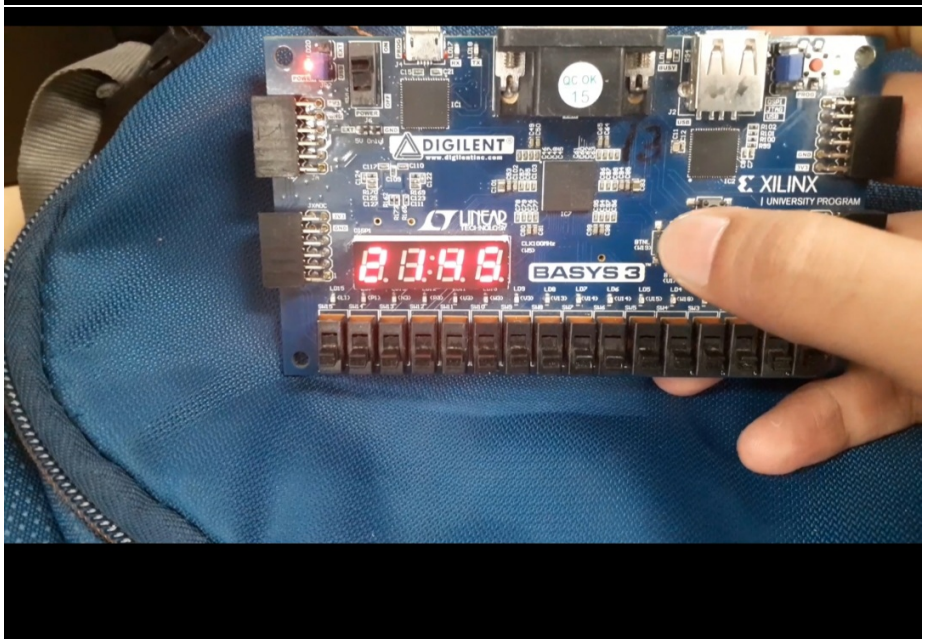
4 Digital Circuit of the Code

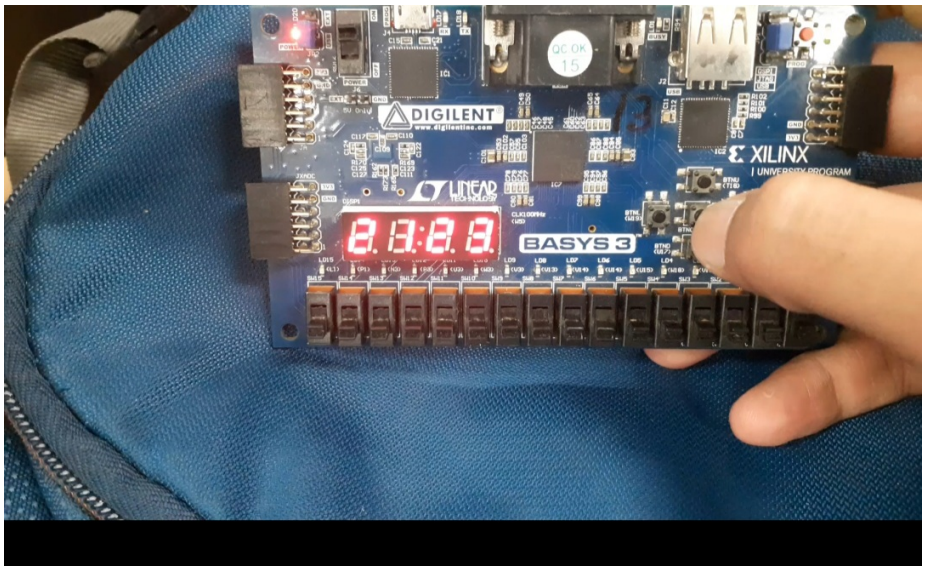


5 Simulation of the Code

6 FPGA OUTPUT






DIGILENT
XILINX
BASYS 3